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A pseudo 2-D surface potential model of a dual material double gate junctionless field effect transistor

Ashutosh Kumar Agrawal[1] · **P. N. V. R. Koutilya**[1] · **M. Jagadesh Kumar**[1]

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Abstract In this paper, we have developed a pseudo two-dimensional (2-D) analytical model for the surface potential of a dual-material double-gate junctionless field-effect transistor. We have incorporated the effects of depletion into the source and drain regions to model the surface potential for all three operating modes: (a) full depletion, (b) partial depletion, and (c) near flatband. The effects of the device parameters such as oxide thickness, silicon thickness, and impurity concentration on the surface potential is demonstrated through the model. The model is further extended to derive an expression for the threshold voltage which predicts the expected change with respect to variation in the device parameters. The accuracy of the proposed model is verified against 2-D numerical simulations.

Keywords 2-D modelling · Dual material double gate (DMDG) · Junctionless field-effect transistor (JLFET) · Poisson's equation · Surface potential · Threshold voltage

1 Introduction

Junctionless field effect transistors (JLFETs) have been studied as a promising alternative for MOSFETs in sub-100 nm regime. The junctionless FET, also known as a gated resistor has several advantages over the conventional MOSFET, like diminished short channel effects (SCEs), nearly ideal subthreshold slope (SS ∼60 mV/dec), high I_{ON}/I_{OFF} ratio, and low source/drain series resistance [1]. Besides, the absence of any metallurgical junctions in the device offers a simplified low thermal budget fabrication process. Analyzing and developing accurate models for JLFETs, hence, is important for circuit designs and simulations.

However, the subthreshold leakage current (diffusion current) for the JLFETs is considerably high and flows through the center of the channel due to low concentration of the depletion charge carriers. To turn OFF the device properly and to achieve a lower value of subthreshold leakage current, we need to use a gate material with a high work function (∼5.6 eV), which is technologically challenging. Instead, the electrostatic performance of the device can be significantly improved by incorporating a step in the surface potential profile using a Dual Material Gate (DMG). The DMG concept has been widely studied to demonstrate the simultaneous suppression of the SCEs and enhancement of trans-conductance, due to the introduction of a step function in the channel surface potential [2–11]. Recently, improvements in electrical characteristics have been demonstrated by using the DMG structure in planar JLFETs and junctionless nanowire transistors [12,13]. In addition, the DMG structure is compatible with the current CMOS fabrication technology [14,15]. Therefore, developing a pseudo two-dimensional (2-D) analytical surface potential model for a dual material double gate junctionless field effect transistor (DMDG JLFET) is of great interest. An accurate surface potential model is useful to develop the drain current model of DMDG JLFET.

In this paper, therefore we report an analytical model for the surface potential of a DMDG JLFET by solving the 2-D Poisson's equation. The model results are verified by comparing them with the 2-D simulated results from ATLAS [16]. Most of the models developed for DG JLFET did not account for depletion into the source and drain regions. In this paper, the depletion regions extending into source (d_S) and drain (d_D) are also considered [10,17].

✉ M. Jagadesh Kumar
mamidala@ee.iitd.ac.in

[1] Department of Electrical Engineering, Indian Institute of Technology Delhi, Hauz Khas, New Delhi 1100016, India

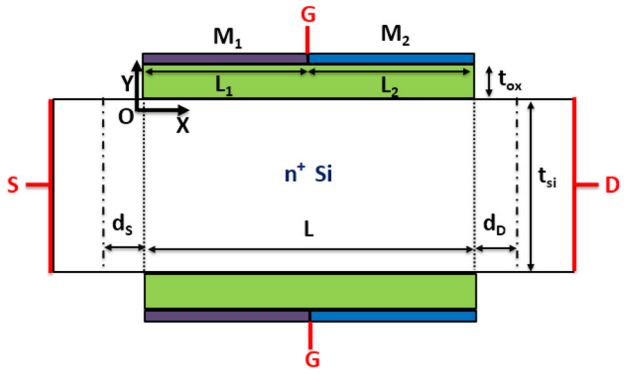

Fig. 1 Cross sectional view of an a dual material double gate junctionless field effect transistor (DMDG JLFET)

2 Two dimensional model for surface potential

A schematic cross sectional view of the DMDG JLFET is shown in Fig. 1. It is a junctionless device with uniform doping in the entire silicon channel. The gate is made up of two different metals laterally merged together, where, the work function of metal in gate1 (M_1) is greater than that of gate2 (M_2) i.e. $\phi_{M1} > \phi_{M2}$ for an n-doped structure and vice-versa for a p-doped structure. The 2-D Poisson's equation for the potential distribution in the channel can be written as:

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2} = \frac{qN_D}{\varepsilon_{si}}\left[e^{\left(\frac{\phi-V}{V_t}\right)}-1\right] \quad for\ 0\le x\le L; -t_{si}\le y\le 0 \tag{1}$$

where $\phi(x,y)$ is the potential at any point (x, y) in the channel, N_D is the channel doping concentration, ε_{si} is the dielectric constant of silicon, V is the quasi-Fermi potential, V_t is the thermal voltage, t_{si} is the channel thickness and L is the channel length.

The parabolic nature of potential across the channel has already been demonstrated [18,19]. Hence, the potential profile in the vertical direction, i.e., the y-dependence of $\phi(x,y)$ can be approximated by a simple parabolic function:

$$\phi(x,y)=\phi_s(x)+a_1(x)\,y+a_2(x)\,y^2;\ -t_{si}\le y\le 0 \tag{2}$$

where $\phi_s(x)$ is the surface potential and arbitrary coefficients $a_1(x)$ and $a_2(x)$ are functions of x only.

In the DMDG JLFET, we have two different gate metals with different work functions. Therefore, the flatband voltage for the two gates would be different. Since, the flat band voltages V_{FB1} and V_{FB2}, respectively, depend upon the work functions ϕ_{M1} and ϕ_{M2}, they can be written as

$$V_{FB1}=\phi_{M1}-\phi_{si}\ and\ V_{FB2}=\phi_{M2}-\phi_{si} \tag{3}$$

where ϕ_{si} is the silicon work function. In the DMDG JLFET structure, since the gate is divided into two parts (M_1 and M_2), the potential under the two gates can be written as

$$\phi_1(x,y)=\phi_{s1}(x)+a_{11}(x)\,y+a_{12}(x)\,y^2 \quad for\ 0\le x\le L_1; -t_{si}/2\le y\le 0 \tag{4}$$

$$\phi_2(x,y)=\phi_{s2}(x)+a_{21}(x)\,y+a_{22}(x)\,y^2 \quad for\ L_1\le x\le L_1+L_2; -\frac{t_{si}}{2}\le y\le 0 \tag{5}$$

3 Boundary conditions

The Poisson's equation under two gates can be solved using following boundary conditions:

(1) Electric flux at the gate-oxide interface is continuous for both metal gate s

$$\varepsilon_{Si}\frac{\phi_1(x,y=0)}{\partial y}=C_{ox}\left(V'_{GS1}-\phi_{s1}(x)\right)\ for\ M_1 \tag{6}$$

$$\varepsilon_{Si}\frac{\phi_2(x,y=0)}{\partial y}=C_{ox}\left(V'_{GS2}-\phi_{s2}(x)\right)\ for\ M_2 \tag{7}$$

where $V'_{GS1}=V_{GS}-V_{FB1}$ and $V'_{GS2}=V_{GS}-V_{FB2}$, $C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}$
ε_{ox} is the dielectric constant of the oxide and t_{ox} is the oxide thickness, V_{GS} is the gate to source bias voltage.

(2) Surface potential at the interface of the two dissimilar metals is continuous

$$\phi_{s_1}(L_1)=\phi_{s_2}(L_1) \tag{8}$$

(3) Electric field at the interface of the two dissimilar metals is continuous

$$\phi'_{s_1}(L_1)=\phi'_{s_2}(L_1) \tag{9}$$

(4) By accounting for the extra depletion into the source region, we can approximate the potential at the source end to be

$$\phi_{s_1}(x=0)=V-\frac{qN_dd_S^2}{2\varepsilon_{Si}} \tag{10}$$

where d_S is the extra depletion into the source region [17].

(5) By accounting for the extra depletion into the drain region, we can approximate the potential at the drain end to be

$$\phi_{s_2}(x=L_1+L_2)=V+V_{DS}-\frac{qN_dd_D^2}{2\varepsilon_{Si}} \tag{11}$$

where d_D is the extra depletion into the drain region, V_{DS} is the drain to source bias voltage [17].

(6) From the boundary condition (10), the electrical field at the source end should be continuous i.e.

$$\phi'_{S_1}(x=0) = -\frac{qN_d d_S}{\varepsilon_{Si}} \tag{12}$$

(7) From the boundary condition (11), the electrical field at the drain end should be continuous i.e.

$$\phi'_{S_2}(x=L_1+L_2) = \frac{qN_d d_D}{\varepsilon_{Si}} \tag{13}$$

4 Modes of operation

According to the applied gate voltage, the operation of the DMDG JLFET can be categorized into three modes: (i) full depletion, (ii) partial depletion, and (iii) near flatband. In this section, the general surface potential functions for all the three modes are discussed. This approach helps in arriving at the final surface potential model in the DMDG JLFET for different modes of operation.

4.1 Full depletion model ($V_G < V_{th}$)

When the applied gate voltage (V_G) is less than the threshold voltage (V_{th}), the channel is completely depleted. Since, the concentration of mobile charges is almost negligible in the channel, the exponential term can be neglected from the Poisson's equation and can be simplified as

$$\frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = \frac{-qN_D}{\varepsilon_{si}}; -t_{si}/2 \le y \le 0 \tag{14}$$

Since, the device is a symmetric structure, the electric field at the center of the device is zero i.e.

$$\frac{\phi(x, y=-t_{si}/2)}{\partial y} = 0 \tag{15}$$

The constants $a_{i1}(x)$ *and* $a_{i2}(x)$ are deduced from the boundary conditions (6, 7) and (15). Substituting their values in (4) and (5) and then in (14), we obtain

$$\phi''_{s_i} - \alpha\phi_{s_i} = \beta_i \tag{16}$$

where $\alpha = \frac{2C_{ox}}{t_{si}\in_{si}}$ *and* $\beta_i = -\left[\frac{qN_D}{\varepsilon_{si}} + \alpha\left(V_G - \phi_{M_i} + \phi_{si}\right)\right]$
(β_i corresponds to gate 'i')

4.2 Partial depletion ($V_{th} < V_G < V_{FB}$)

When the applied gate voltage is between the threshold voltage and the flatband voltage, the channel is partially depleted,

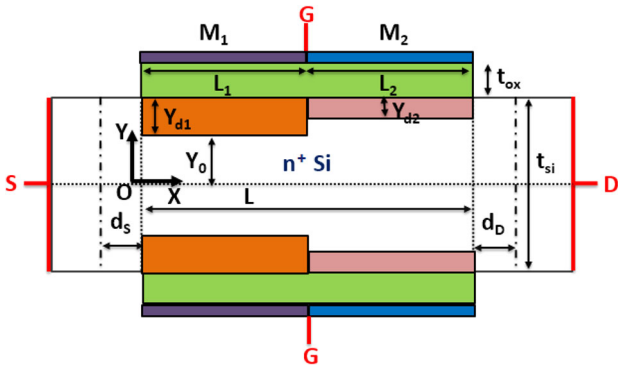

Fig. 2 DMDG JLFET illustrating partial mode under both gate1 and gate2

leaving a neutral region at the center of the structure. In the depletion region, therefore, the Poisson's equation can be simplified as

$$\frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = \frac{-qN_D}{\varepsilon_{si}}; -y_d \le y \le 0 \tag{17}$$

To model the surface potential function in the partial depletion, we need to calculate the depletion thickness (y_d) of the channel (refer to Fig. 2). Assuming uniform y_d in the channel, it is calculated through one dimensional (1-D) model of the surface potential in the depletion region. Assuming the origin to be at the center of the device, 1-D model is developed given as

$$\phi(x,y) = \frac{-qN_D}{2\varepsilon_{si}}(|y| - y_0)^2 - E_0(|y| - y_0) + V - V_t; \quad y_0 \le |y| \le t_{si}/2 \tag{18}$$

where y_0 is the point from the origin where the depletion region starts, E_0 is the electric field at y = y_0.

Since, the potential profile across the channel is parabolic in nature, the electric field can be approximated as E=Ky in the neutral region ($0 \le |y| \le y_0$), where K is a constant. We obtain a concise expression for E_0 by the finite difference method using the potential relation $\phi(x, y_0) = V - V_t$ i.e.

$$\frac{\phi(x, y=y_0)}{\partial y} = Eo = \frac{-8V_t y_d}{t_{Si}^2} \tag{19}$$

$$y_d = \frac{t_{si}}{2} - y_0 \tag{20}$$

Using Eqs. (19) and (20) in (18), then using Eq. (6) or (7), the depletion thickness y_d can be calculated as

$$y_d = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \tag{21}$$

where $b = \frac{qN_d}{C_{ox}} + \frac{8\varepsilon_{si}V_t}{C_{ox}*t_{Si}^2}$, $a = \frac{qN_d}{2\varepsilon_{si}} + \frac{8V_t}{t_{Si}^2}$, c $= V_g - V_{FB_2} -$ V$+V_t$

Also, y_d being the magnitude of depletion thickness, it remains unchanged with respect to the change in the origin.

The potential in the neutral region follows a simple parabolic potential approximation where the potential at the center of the device is approximated to be V, i.e.

$$\phi\,(x, y = -t_{si}/2) = V \tag{22}$$

The constants $a_{i1}\,(x)\ and\ a_{i2}\,(x)$ are deduced from the boundary conditions (6, 7) and (19). Substituting their values in (4) and (5) and then in (17), we obtain,

$$\phi''_{s_i} - \alpha\phi_{s_i} = \beta_i \tag{23}$$

where $\alpha = \frac{C_{ox}}{y_d\varepsilon_{si}}\ and\ \beta_i = -\left[\frac{qN_D}{\varepsilon_{si}} + \alpha\left(V_G - \phi_{M_i} + \phi_{si}\right)\right]$
(β_i corresponds to gate 'i')

4.3 Near flatband ($|V_G \sim V_{FB}| \leq V_t$)

Around the flatband voltage, the carrier concentration in the entire channel is approximately equal to $N_D(\sim 10^{19}/cm^3)$. On further increasing the gate voltage, negative charges accumulate at the surface changing the curvature of the band diagram [18]. Using Taylor' series, the Poisson's equation can be approximated as

$$\frac{\partial^2\phi\,(x, y)}{\partial x^2} + \frac{\partial^2\phi\,(x, y)}{\partial y^2} = \frac{qN_D}{\varepsilon_{si}}\left(\frac{\phi - V}{V_t}\right);$$
$$-t_{si}/2 \leq y \leq 0 \tag{24}$$

The constants $a_{i1}\,(x)\,and a_{i2}\,(x)$ are deduced from the boundary conditions (6, 7) and (15). Substituting their values in (4) and (5) and then in (24), we obtain

$$\phi''_{s_i} - \alpha\phi_{s_i} = \beta_i \tag{25}$$

where

$$\alpha = \frac{2C_{ox}}{t_{si}\varepsilon_{si}} + \frac{qN_D}{\varepsilon_{si}V_t}\ and$$
$$\beta_i = -\left[\frac{qN_D}{\varepsilon_{si}V_t} + \alpha\left(V_G - \phi_{M_i} + \phi_{si}\right)\right]$$

(β_i corresponds to gate 'i')

5 Combination of operating modes

Since $\phi_{M1} > \phi_{M2}$, the threshold and the flatband voltages for gate1 are larger than that of gate2 ($V_{th1} > V_{th2}\&V_{FB1} > V_{FB2}$). Therefore, on applying a gate voltage, the channels under the two gate regions will be in different operating modes. Hence, we need to model the surface potential for different combinations of the operating modes. The surface potential model for a particular combination of operating modes is developed from the previously obtained general surface potential model depending upon the operating mode, exhibited under the respective gate. In addition, on applying a gate voltage, the depletion thicknesses(y_{d1}, y_{d2}) under the two gates will be different.

5.1 Full depletion (gate1) and partial depletion (gate2)

When $V_G < V_{th1}$ (threshold voltage of gate1) and $V_{th2} < V_G < V_{FB2}$, the channel under gate1 is fully depleted and the channel under gate2 is partially depleted. Using equations (16) and (23) for gate1 and gate2 respectively, the surface potential functions can be written as

$$\phi_{s_1}\,(x) = A_1e^{\lambda_1 x} + B_1e^{-\lambda_1 x} - \frac{\beta_1}{\alpha};\ 0 \leq x \leq L_1 \tag{26}$$

$$\phi_{s_2}\,(x) = A_2e^{\lambda_2(x-L_1)} + B_2e^{-\lambda_2(x-L_1)} - \frac{\beta_2}{\alpha};\ 0 \leq x \leq L_2 \tag{27}$$

where A_1, A_2, B_1, and B_2 are deduced using the boundary conditions (8–13) as shown below in (33).

5.2 Partial depletion (gate1) and partial depletion (gate2)

When $V_G > V_{th1}$ (threshold voltage of gate1) and $V_{th2} < V_G < V_{FB2}$, the channel under both the gates is partially depleted. This results in the formation of depletion regions of thickness y_{d1} and y_{d2} under gate1 and gate2, respectively. Using equation (23) for both the gates, the surface potential functions can be written as

$$\phi_{s_1}\,(x) = A_1e^{\lambda_1 x} + B_1e^{-\lambda_1 x} - \frac{\beta_1}{\alpha};\ 0 \leq x \leq L_1 \tag{28}$$

$$\phi_{s_2}\,(x) = A_2e^{\lambda_2(x-L_1)} + B_2e^{-\lambda_2(x-L_1)} - \frac{\beta_2}{\alpha};\ 0 \leq x \leq L_2 \tag{29}$$

where A_1, A_2, B_1, and B_2 are deduced using the boundary conditions (8–13) as shown below in (33).

5.3 Partial depletion (gate1) and near flatband (gate2)

When $V_{th1} < V_G < V_{FB1}$ and $V_G > V_{FB2}$ channel under gate1 is partially depleted with a depletion thickness (y_{d1}) and the channel under gate2 is in near flat band mode. In near flat band mode, there is no depletion in the channel. Hence, the depletion width into the drain region is zero ($d_D = 0$).

Using Eqs. (23) and (25) for gate1 and gate2 respectively, the surface potential functions can be written as

$$\phi_{s_1}(x) = A_1 e^{\lambda_1 x} + B_1 e^{-\lambda_1 x} - \frac{\beta_1}{\alpha};\ 0 \le x \le L_1 \tag{30}$$

$$\phi_{s_2}(x) = A_2 e^{\lambda_2 (x-L_1)} + B_2 e^{-\lambda_2 (x-L_1)} - \frac{\beta_2}{\alpha};\ 0 \le x \le L_2 \tag{31}$$

where A_1, A_2, B_1, and B_2 are deduced using the boundary conditions (8–12) as shown below in (33).

5.4 Threshold voltage

At threshold, the channel is completely depleted. Therefore, on substituting $y_d = -t_{si}/2$ in equation (21) and solving for the gate voltage, we get the threshold voltage as

$$V_{th} = V_{FB1} - \frac{qN_D}{8\varepsilon_{si}} t_{si}^2 - \frac{qN_D}{2\varepsilon_{ox}} t_{si} t_{ox} + V - 3V_t - \frac{4C_{si}}{C_{ox}} V_t \tag{32}$$

In the case of DMG structure, due to the coexistence of metal gates M_1 and M_2, with different work functions, the threshold voltage of DMDG JLFET is solely determined by the metal gate with a higher work function i.e. ϕ_{M1} [3].

$$d_S = \frac{-b_S + \sqrt{b_S^2 - 4a_S c_S}}{2a_S} \text{ and } d_D = \frac{-b_D + \sqrt{b_D^2 - 4a_D c_D}}{2a_D}$$

$$a_S = \frac{qN_d}{2\varepsilon_{si}},\ b_S = \frac{qN_d}{\varepsilon_{si}\lambda_1},\ c_S = -\frac{\beta_1}{\alpha_1} - V \text{ and}$$

$$a_D = \frac{qN_d}{2\varepsilon_{si}},\ b_D = \frac{qN_d}{\varepsilon_{si}\lambda_2},\ c_D = -\frac{\beta_2}{\alpha_2} - V - V_d$$

$$\lambda_i = \sqrt{\alpha_i};\ B_1 = 0.5\left(\frac{\beta_1}{\alpha_1} + V - \frac{qN_d}{2\varepsilon_{si}} d_S^2 + \frac{qN_d}{\varepsilon_{si}\lambda_1} d_S\right)$$

$$A_2 = \begin{cases} 0.5\left(\frac{\beta_2}{\alpha_2} + V + V_d - \frac{qN_d}{2\varepsilon_{si}} d_D^2 + \frac{qN_d}{\varepsilon_{si}\lambda_2} d_D\right) e^{-\lambda_2 L_2} \\ \quad Full\ and\ Partial\ depletion\ modes \\ \frac{\left[\left(V + V_d + \frac{\beta_2}{\alpha_2}\right)(\lambda_1+\lambda_2) e^{(\lambda_2 L_2)} + \left(\frac{\beta_1}{\alpha_1} - \frac{\beta_2}{\alpha_2}\right)\lambda_1 - 2\lambda_1 B_1 e^{-\lambda_1 L_1}\right]}{\lambda_1 - \lambda_2 + (\lambda_1+\lambda_2) e^{(2\lambda_2 L_2)}} \\ \quad Near\ flatband\ mode \end{cases}$$

$$A_1 = \frac{\left[2A_2 - \left(1 - \frac{\lambda_1}{\lambda_2}\right) B_1 e^{-\lambda_1 L_1} + \frac{\beta_1}{\alpha_1} - \frac{\beta_2}{\alpha_2}\right] e^{-\lambda_1 L_1}}{1 + \frac{\lambda_1}{\lambda_2}}$$

$$B_2 = \left[\left(1 - \frac{\lambda_1}{\lambda_2}\right) A_1 e^{\lambda_1 L_1} + \left(1 + \frac{\lambda_1}{\lambda_2}\right) B_1 e^{-\lambda_1 L_1} - \frac{\beta_1}{\alpha_1} + \frac{\beta_2}{\alpha_2}\right] * 0.5 \tag{33}$$

In the above equations, values of α_i, β_i, λ_i are used from the Sect. 4 depending upon the operating mode, exhibited by the respective gate.

6 Model verification and discussion

To verify the proposed analytical model, the 2-D device simulator ATLAS is used to simulate the potential distribution within the silicon channel [16]. A DMDG JLFET structure is implemented in ATLAS, having a uniformly n-doped ($N_D \sim 10^{19}/cm^3$) source, drain and channel regions. The typical values of the work functions of gate metals M1 and M2 are chosen to be 5.2 and 4.7 eV, respectively. The Shockley–Read-Hall recombination model and the Fermi–Dirac carrier statistics are used in the simulation. The device channel length is 100 nm and source/drain lengths are 10 nm each to avoid parasitic resistance effects. The other device parameters used are; channel thickness (t_{si}) = 10 nm, $L_1 = L_2$ = 50 nm, gate oxide thickness (t_{ox}) = 2 nm, and $V_S = V_D = 0$. The threshold voltages for the two gates, calculated from (32), are $V_{th1} = 0.23$ V, $V_{th2} = -0.27$ V. Figure 3 shows the surface potential variation with respect to different val-

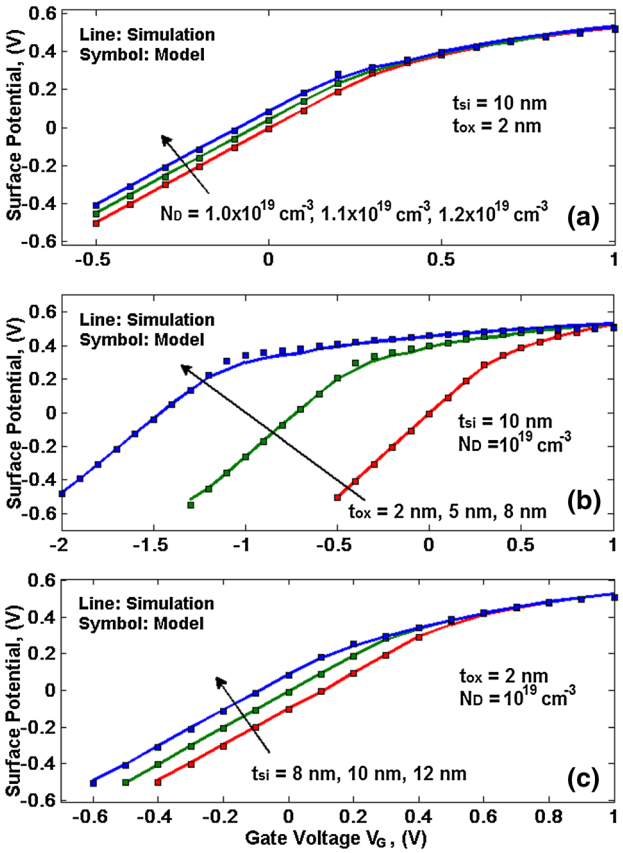

Fig. 3 The surface potential of DMDG JLFET under gate1 versus gate voltage for different values of **a** impurity concentration, **b** gate oxide thickness, and **c** silicon film thickness

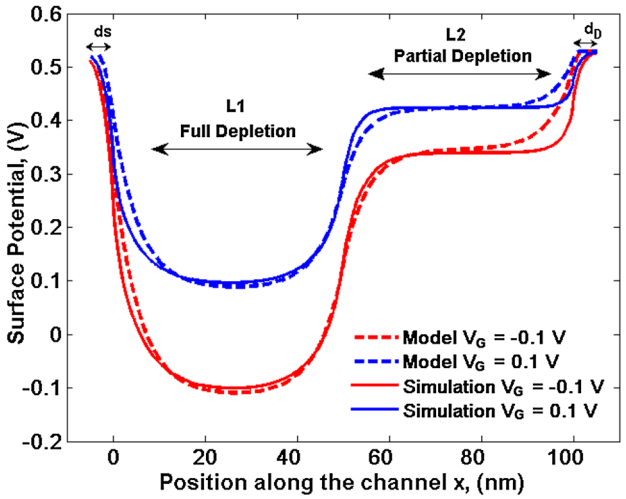

Fig. 4 The surface potentials versus position along the channel for full depletion under gate1 and partial depletion under gate2 for $V_G = -0.1$ and 0.1 V

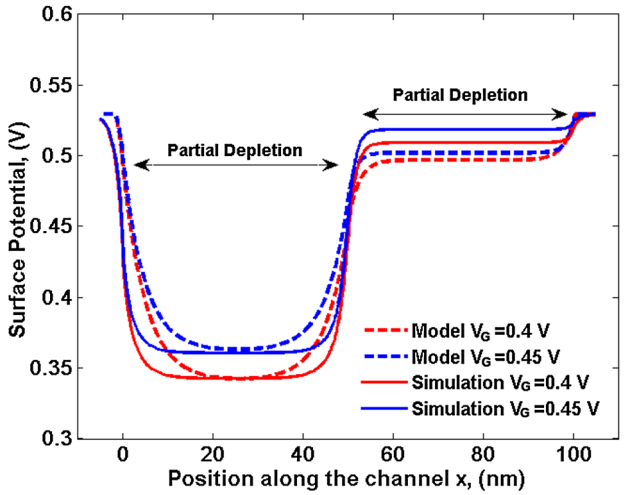

Fig. 5 The surface potentials versus position along the channel for partial depletion under both gate1 and gate2 for $V_G = 0.4$ and 0.45 V

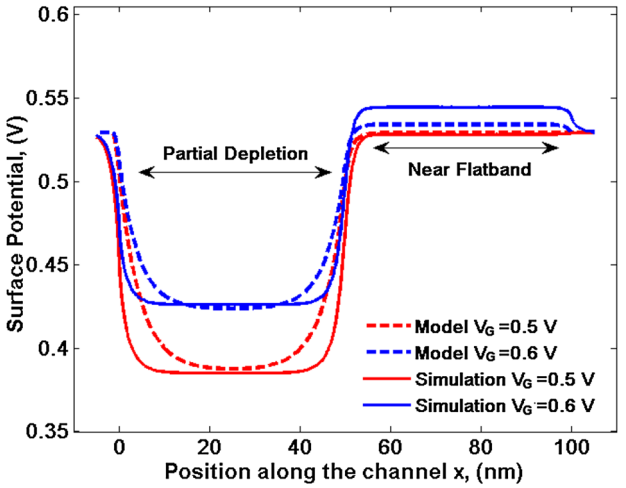

Fig. 6 The surface potential versus position along the channel for partial depletion under gate1 and near flatband ($V_G = 0.5$ V) / accumulation ($V_G = 0.6$ V) under gate2

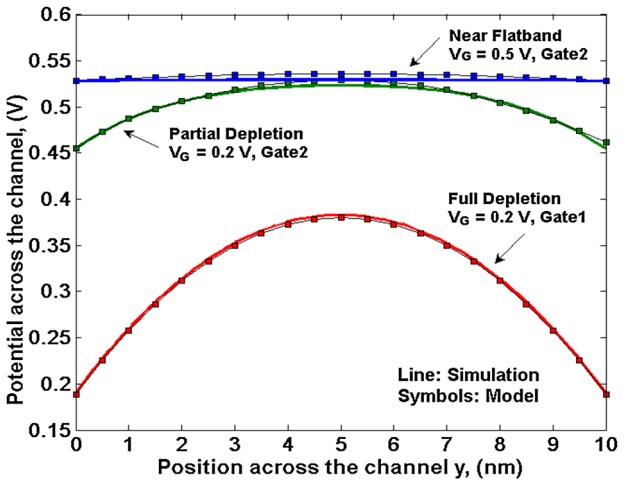

Fig. 7 Potential distribution versus position across the channel for **a** full depletion, **b** partial depletion, **c** near flatband condition

ues of (a) impurity concentration, (b) gate oxide thickness and (c) silicon film thickness. Irrespective of which one of these parameters is varied, the surface potential converges to the quasi-Fermi potential (∼0.5294 V) as the gate voltage approaches the flatband voltage. The reason for this convergence is that the electric field and the space charge concentration would be zero when the device is in the near flatband mode. In addition, due to the absence of the depletion region the impact of oxide or silicon channel capacitance reduces in near flat band condition. We observe from Fig. 3 that the model shows good agreement with the simulation results. In Fig. 4, the surface potential along the channel is shown for $V_G = -0.1$ and 0.1 V. At these gate voltages, the channel under gate1 is fully depleted and the channel under gate2 is partially depleted. In addition, it is evident from the figure that the proposed analytical model accounts for the depletion into the source and drain region and the model values are in good agreement with the simulation results. Similarly, Fig. 5 shows the surface potential along the channel for $V_G = 0.4$ and 0.45 V.

At these gate voltages, the channel under both gate1 and gate2 is partially depleted. We observe that the error between the model and the simulation results is negligible (≤2 %). Even this small error is due to the fact that the electric field approximation (18) used in the partial depletion model does not hold good for the gate voltages around flatband. Figure 6 compares the surface potentials along the channel for $V_G = 0.5$ and 0.6 V from our model with simulations. At these gate voltages, the channel under gate1 is partially depleted and the channel under gate 2 is in near flat band condition. The channel under the gate2 is entirely neutral due to

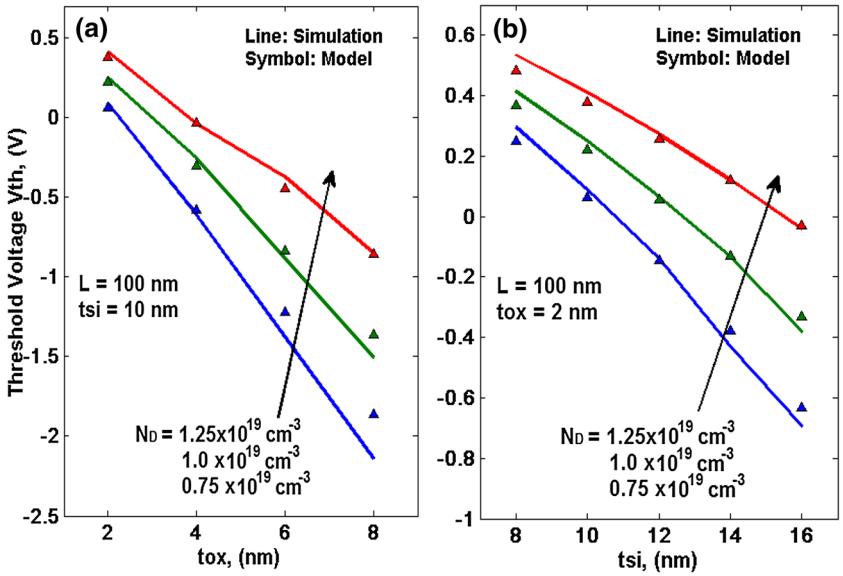

Fig. 8 Threshold voltage of DMDG JLFET for various **a** oxide thickness and **b** silicon thickness as a parameter of impurity concentration for $V_D = 1.0\,V$

absence of any space charges. Therefore, the surface potential plot is completely flat and in conjunction with the quasi-Fermi potential for gate2. Therefore, at $V_G = 0.5\,V$, ϕ_{s_2} is equal to V (~0.5294 V), as is expected. When $V_G = 0.6\,V$, the channel under gate2 enters the accumulation regime. The model results match well with the simulation results even when the gate voltage exceeds the flatband voltage of the channel under gate2. In Fig. 7, the potential distributions across the channel from our model and simulations are compared for all the operating modes.

In Fig. 8, the threshold voltage calculated from the analytical model (32) for different impurity concentrations is compared with those obtained from 2-D simulation, extracted from the commonly used maximum transconductance method [3], for different values of gate oxide thickness and silicon film thickness. We observe that for a given channel doping, the threshold voltage decreases with an increase in either the gate oxide thickness or the silicon film thickness. The proposed analytical model accurately predicts the potential distribution for the entire silicon channel. The model is continuous and is valid for all the operating modes, making it suitable to develop the drain current model of a DMG JLFET.

7 Conclusions

In this paper, we have developed a pseudo 2-D analytical model for the surface potential of a DMDG JLFET. This model uses a parabolic approximation to find the surface potential under the two metal gates. The extra depletion extending into the source (d_S) and the drain regions (d_D) is accounted for a better accuracy of the model. In the partial depletion mode, a model for the channel depletion thickness (y_d) is also developed and is further used to model both the surface potential and the threshold voltage. The model accurately predicts the surface potentials for all the different combination of operating modes exhibited under the two metal gates. The dependence of the surface potential and threshold voltage on the device parameters such as doping concentration, gate oxide and silicon film thicknesses is demonstrated. The accuracy of the model is validated against 2-D numerical simulations.

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