J Comput Electron (2015) 14:537–542
DOI 10.1007/s10825-015-0685-1

Dual metal-double gate tunnel field effect transistor with mono/hetero dielectric gate material

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Published online: 18 March 2015
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Abstract In this paper, dual metal-double gate tunnel field effect transistor (DMG-DGTFET) is discussed for mono & hetero dielectric gate material. The hetero dielectric that we have used at the gate is a combination of SiO_2 and HfO_2. The DMG technique is used to optimize the performance of DGTFET along with the mono/hetero dielectric gate material. The results obtained from the simulation are discussed using energy band diagram, tunneling barrier width and compared with hetero & mono dielectric gate. With the application of hetero dielectric to the DMG-DGTFET, the advantages of both the techniques combine and the results shows that higher I_{ON}/I_{OFF} ratio (2×10^9) compared to the mono dielectric case (2.5×10^8). The average subthreshold slope also improves from 58 mV/decade in mono dielectric to 48 mV/decade in hetero dielectric DMG-DGTEFT. All the simulations are done in Synopsys TCAD for a channel length of 25 nm using the non-local tunneling model.

Keywords Dual metal gate (DMG) · Single metal gate (SMG) · Double gate (DGTFET) · Band-to-band tunneling (BTBT)

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1 Introduction

The continued scaling of the transistors and the increase in the transistor density, has led to an immense increase in the power density on chip. Supply voltage scaling reduces the dynamic power consumption which is desirable for power constrained application, but to achieve the same ON-current, threshold voltage V_{th} has to be scaled proportionately as V_{DD} reduces. The reduction of V_{th} causes an exponential increase of OFF-current and the static leakage power. The exponential increase of OFF-current is due to threshold swing limit of 60 mV/decade, due to the Boltzmann distribution of carriers at room temperature. Therefore it becomes essential to explore other new devices structure, which can operate at low voltage and consumes less power [1,2], and in this regard Tunnel FET appears to be the most promising device which is emerging for low power applications. Tunnel FET can be operated at much lower drain voltage [3,4] and is having excellent subthreshold characteristics [5,6] compared to MOSFET [7]. The difference in the characteristics of MOSFET and TFET is attributed to the operational mechanism difference. In Tunnel FET majority current flows because of BTBT [8] between the source/body junctions while in MOSFET it is due to the drift diffusion. But the TFET has its disadvantages also and one of the major disadvantages is its ON-current, which is much lower than conventional MOSFET as required by ITRS [9]. Another drawback of TFET's is it's ambipolar conduction for negative V_G values. To make the TFET a mainstream device, it becomes essential to increase its ON-current and reduce its ambipolar conduction.

The current in TFET is proportional to the BTBT tunneling probability which is calculated by using Wentzel–Krammers–Brillouin (WKB) approximation and Kane dispersion relationship and is given by

$$I_{ON} \propto T_{WKB} \propto exp\left(-\left(\lambda_{dop}+\lambda_{ch}\right)\frac{4\sqrt{2m^*}}{3h\left(\Delta\phi+E_g\right)}E_g^{3/2}\right) \quad (1)$$

where m^* is the effective mass and E_g the energy band gap, is the screening length of the electric potential,λ_{dop} refects the steepness of the doping profile and λ_{ch} is determined by the device structure. λShould be minimized to achieve good electrostatic control.$\Delta\phi$ denotes the energy overlap of valence band and conduction band.

Equation (1) suggests that the tunneling probability is a direct function of band gap of the material and thus by using the material with lower band gap (Ge, $Si_{1-x}Ge_x$) [10,11] at the source, ON-current can be increases significantly. Another technique uses high-k dielectric [12] at the gate which increases the ON state current significantly, because the use of high-k dielectric at the gate improves the coupling of the gate to the source/body junction, which results in the increase of ON-current. Double Gate TFET with high-k dielectric [13] also increases the ON-current significantly. DMG-DGTFET can also be used to optimize the ON state and OFF state current simultaneously in TFET [14]. The ambipolar conduction can be reduced by using hetero dielectric gate, short gate TFET's or gate drain underlap [15,16], asymmetric source/drain doping etc.

The rest of the paper is organized as follows: Sect. 2 explains the structure of DMG-DGTFET [17,18] with hetero-dielectric gate [19,20] and simulation model used. Section 3 shows the results obtained by the simulation of SMG-DGTFET with hetero dielectrics (combination of silicon dioxide and hafnium oxide). Section 4 involves the detailed study of DMG-DGTFETS with hetero /mono dielectric gate along with the simulation results. Section 5 has comparison of results along with the table. In the last section conclusion has been drawn based on the results that we got from the simulation.

2 Schematic of DMG-DGTFET with hetero dielectric gate material and simulation model

The DMG-DGTFET based on hetero dielectric material consists of gate with two different metals. The metal gate which is near to the drain is called auxiliary gate, whose work function variation mainly controls the OFF state current. The metal gate near to the source side is called tunnel gate, and it controls the tunneling between body/source junctions. Hetero dielectric material consists of a combination of different dielectric (Fig. 1).

The Fabrication of DMG-DGTFET, based on hetero dielectric gate can be done by the technique already available [21,22]. The dielectric below the tunnel gate is having a high dielectric constant, since it improves the ON-current with more electrostatic coupling between the gates and tunneling junction.

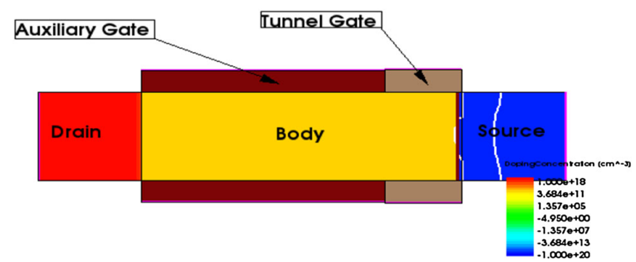

Fig. 1 The schematic cross sectional view of DMG-DGTFET with hetero dielectric gate material with showing the doping profile in the device

The doping profile is assumed to be constant in the drain, source and body region [23,24]. All the simulations are done using Synopsys TCAD, using the Non-Local tunneling model [25,26] for the calculation of BTBT tunneling current. The values of the Non-Local tunneling model are calibrated to the practical results [27]. Phonon assisted tunneling is used in the model. The gate tunneling current is simulated using Direct tunneling model and the traps are considered as fixed charge with concentration of 1e+10 cm^{-3}. The mobility at the surface is degraded because of the use of high-k dielectric at the gate and to include high-k degradation effect Enormal model is used with the default parameter values [28,29]. Quantum effects are not considered in the simulation due to the lack of availability of quantum models [30], which are coupled with the non local BTBT tunneling model. However it is to be noted including quantum effects in the simulation will lead to a V_T shift in drain current [31], because of charge centroid shift away from the surface effective oxide thickness increases, which degrades the current and also due to slight increase in band gap, because of quantization of energy states at the surface BTBT current decreases. A very fine mesh is used at the surface to simulate the structure.

The following parameter value have been used throughout this work drain doping 1e+18 cm^{-3} (Arsenic), source doping 1e+20 cm^{-3}(Boron), body is doped slightly with arsenic concentration of 1e+16 cm^{-3}.The thickness of the gate dielectric material is 2 nm. Hetero dielectric that we have used in this study is composed of silicon dioxide SiO_2 and hafnium oxide HfO_2. The gate length that we used throughout this work is 25 nm.The length of auxiliary gate is L_{aux} 18 nm and that of tunnel gate is $L_{tun} = 7$ nm. The silicon body thickness t_{si} is 8 nm.The analysis of DMG-DGTFETS has been done for $V_{DD} = 1.0$.

3 SMG-DGTFET based on hetero dielectric gate material

The DGTFET based on hetero dielectric material is simulated and the results are shown in Fig. 2. The analysis is carried out

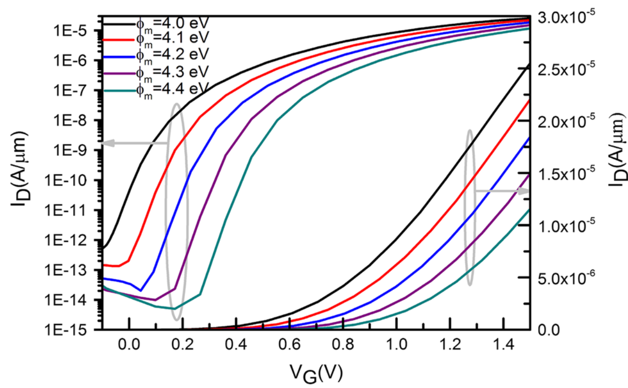

Fig. 2 SMG-DGTFET(L $= 25\,$nm, $t_{ox} = 2\,$nm) based on $SiO_2 + HfO_2$ hetero gate dielectric for different values of ϕ_m

for SMG-DGTFET based on SiO_2 and HfO_2 hetero dielectric to find the optimum value of the work function of the metal.

From Fig. 2 it can be seen that the best possible value of I_{ON}/I_{OFF} is achieved at $\phi_m = 4.3\,$eV. The purpose of using hetero dielectric is to optimise the OFF-current as compared to mono dielectric. Since tunneling occurs at the source/body junction, which is controlled by the dielectric at the source side, by using a material with high-K at the source side, results in a significant increase in the ON current. The dielectric on the drain side affects only the OFF-current. Important thing to notice here is that by changing the Φm in the SMG-DGTFET based on hetero dielectric gate changes the transfer characteristics significantly, but the change is that it just shifts the transfer characteristics parallel to the X-axis as a result average subthreshold slope doesn't improves.

4 DMG-DGTFET based on hetero dielectric gate material

In this section, DMG-DGTFET based on hetero dielectric gate material is analyzed. The analysis is carried out in the same way as it is done for DMG-DGTFET [32]. The results obtained are shown below in Fig. 3. The dual metal at the gate in DMG-DGTFET, along with different dielectrics provide additional flexibility to control different section of the transfer characteristics, thus improving the TFET performance.

At OFF state, as $\phi_{aux.}$ increases the OFF state current first decreases and then increases as shown in Fig. 3c. The OFF state current is composed of reverse leakage current plus the BTBT current, as ϕ_{aux} increases up to 4.4 eV reverse leakage current will dominate, since there is no tunneling path; but with further increase in ϕ_{aux} tunneling path will be formed at the drain end as shown above in Fig. 3a which increases the OFF state current. At ON state, increase in $\phi_{aux.}$ does not bring any significant change in the tunnel barrier width as shown in Fig. 3b.

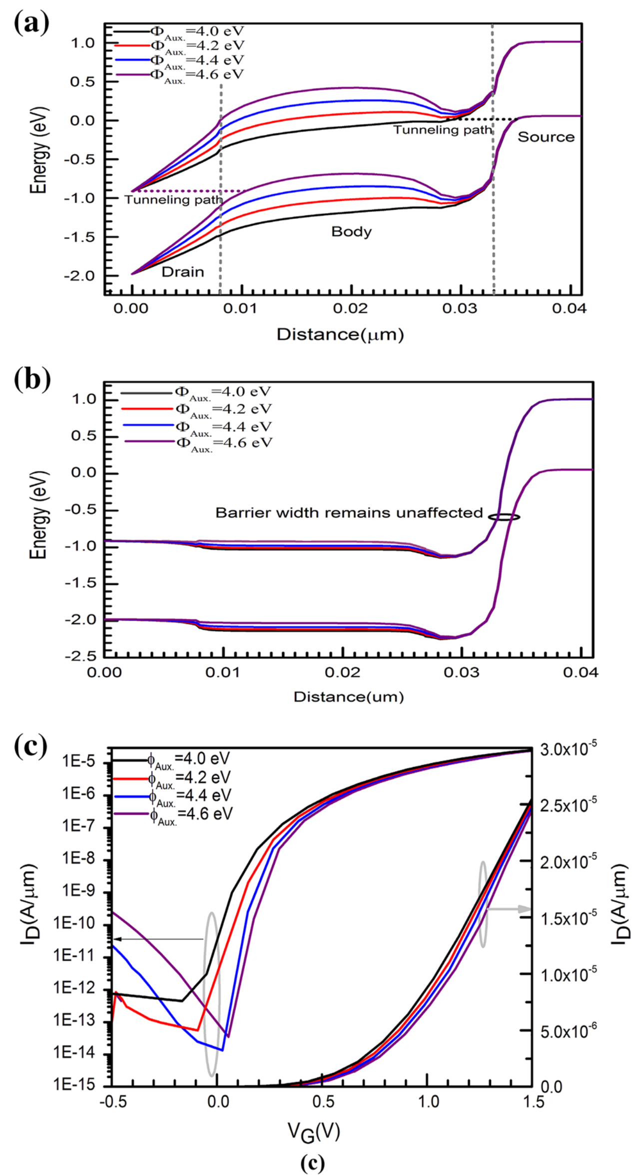

Fig. 3 For DMG-DGTFET based on hetero dielectric gate material ($\phi_{tun.} = 4.0\,$eV, $L_{tun} = 7$ nm $L_{aux} = 18\,$nm). Energy band diagram along a *horizontal cut line* near to the surface is shown at **a** OFF state ($V_{gs} = 0\,$V and $V_{ds} = 1$) V. **b** ON-state ($V_{gs} = 1.5$ V, $V_{ds} = 1\,$V. **c** Transfer characteristics at $V_{DS} = 1.0\,$V shown on both semi log and linear scale

The ambipolar current increases for negative increase in V_G values as shown in Fig. 3c. As ϕ_{aux} increases for constant negative V_G, bands are pulled upwards, as a result tunneling path is formed at the drain end and barrier width reduces, BTBT occurs thus the current increases. The gate current under both the auxiliary and tunnel gate decreases with increase in ϕ_{aux} for constant $\phi_{tun} = 4.0\,$eV. For $\phi_{aux} = 4.4\,$eV and $\phi_{tun} = 4.0\,$eV, the maximum value of gate current under both auxiliary and tunnel gate is limited to 1e−13 A/um. .

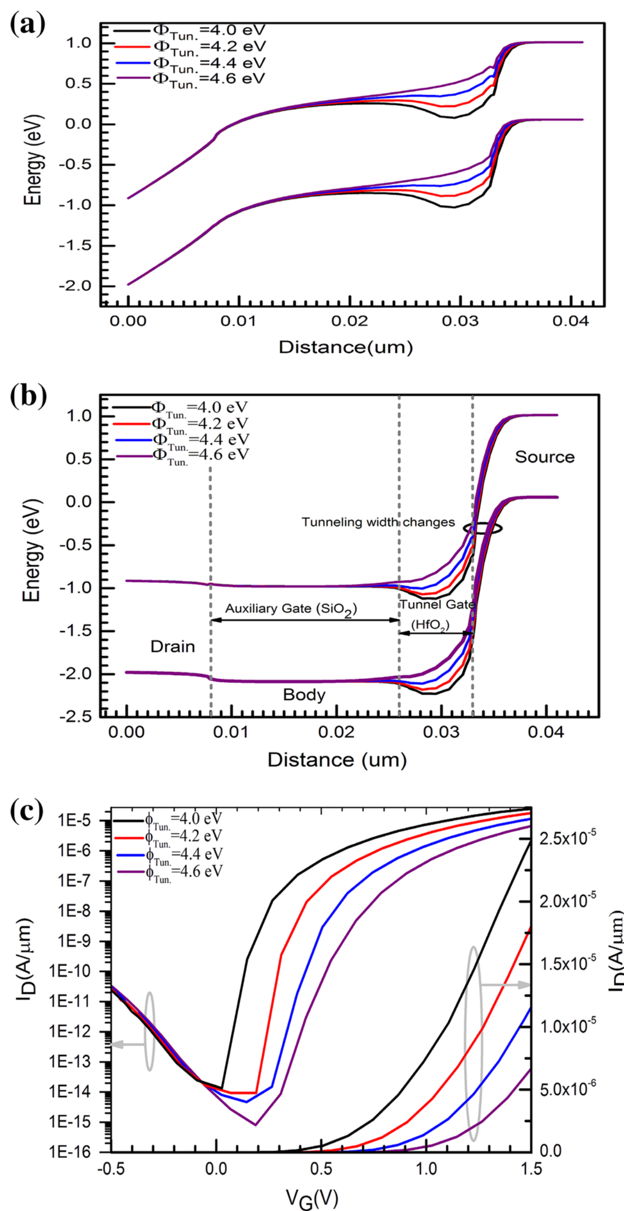

Fig. 4 For DMG-DGTFET based on hetero dielectric gate material ($\phi_{aux} = 4.4$ eV, $L_{tunn.} = 7$ nm, $L_{aux} = 18$ nm). Energy band diagram along a *horizontal cut line* near to the surface is shown at **a** OFF state ($V_{gs} = 0$ V and $V_{DS} = 1$V). **b** ON state ($V_{gs} = 1.5$V, $V_{ds} = 1$V). **c** Transfer characteristics shown on both semi log and linear scale at $V_{ds} = 1.0$ V

From the ϕ_{tun} results, it can be concluded that at ON state, as the tunnel gate work function increases the current starts to decrease, as shown below in Fig. 4c, because of increased tunnel barrier width at the source/body junction, Fig. 4b. At OFF state tunnel gate work function doesn't bring any significant change in tunnel barrier width as shown in Fig. 4a.

The ambipolar conduction is not affected by ϕ_{tun}, this is because of the fact that ϕ_{tun} doesn't bring significant changes in the energy band at the drain end, thus current remains unaffected by ϕ_{tun} for negative V_G. The gate current under

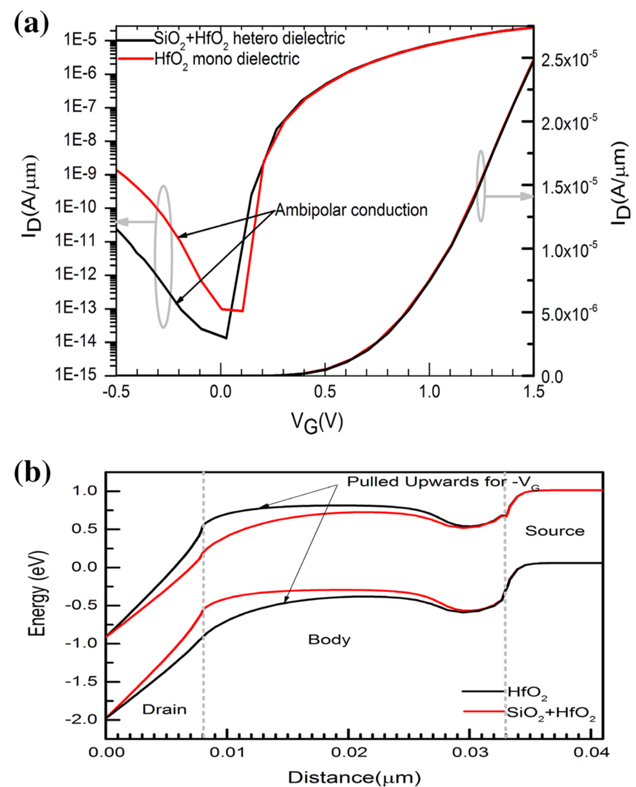

Fig. 5 Transfer characteristics for mono & hetero dielectric DMG-DGTFET ($\phi_{aux} = 4.4$ eV, $\phi_{tunn} = 4.0$ eV) at $V_{ds} = 1.0$ V **b** Energy band diagram along a *horizontal cut line* near to the surface shown at ($V_{gs} = -0.5$V and $V_{DS} = 1$V)

both the gate decreases with increase in ϕ_{tun} for constant $\phi_{aux} = 4.4$ eV. The maximum gate current under both the gate is limited to 1e−13 A/um for constant $\phi_{tun.} = 4.0$ eV and $\phi_{aux} = 4.4$ eV.

The best possible value for the auxiliary gate work function (ϕ_{aux}) is 4.4 eV and for tunnel gate (ϕ_{tun}) it is 4.0 eV.The metals which can be used at gates to obtain the desired ϕ_{aux} (4.4 eV) are (e.g., W, Ta, and Mo) and ϕ_{tun} (4.0 eV) are (e.g., Mo, Ni–Ti, and Sc) [33,34].

The results obtained for DMG-DGTFET based on SiO_2+HfO_2 hetero dielectric and HfO_2 mono dielectric gate are compared and shown above in Fig. 5. The hetero dielectric at the gate gives better performance as compared to mono dielectric in DMG-DGTFET. The value achieved for I_{ON}/I_{OFF} is 2.5×10^8 in the mono dielectric, while it is 2×10^9 for hetero dielectric gate DMG-DGTFET. Also the ambipolar conduction in mono dielectric is more as compared to hetero dielectric this can be explained as follows: for mono dielectric the voltage drop would be minimum in HfO_2 more in silicon, as a result the band are pulled more upward as compared to $SiO_2 + HfO_2$ hetero dielectric as shown in Fig. 5b.

The average subthreshold slope, which can be used as a performance parameter in comparison of semiconductor

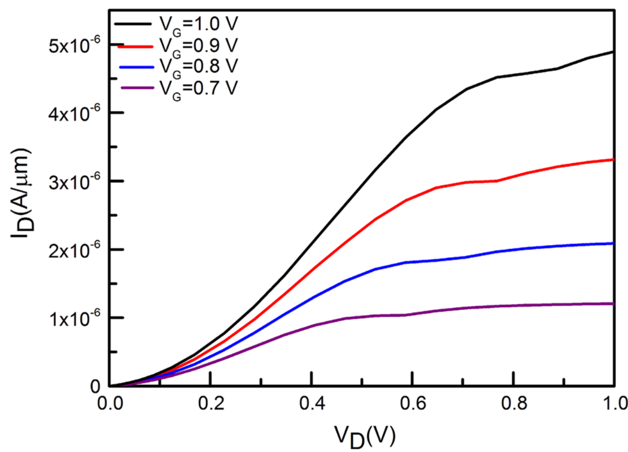

Fig. 6 Transfer characteristics with respect to drain voltage for different gate voltage for DMG-DGTFET based on hetero dielectric material gate ($\phi_{aux} = 4.4$ eV, $\phi_{tunn.} = 4.0$ eV, $L_{aux.} = 18$ nm, $L_{tunn.} = 7$ nm)

devices and is defined as:

$$SS_{AVG} = \frac{V_T - V_{OFF}}{log(I_{vt}) - log(I_{VOFF})} \quad (2)$$

where , V_T is the threshold voltage, V_{OFF} is the gate voltage from which the drain current starts to take off [35], I_{Vt} is the drain current at $V_{gs} = V_t$, and I_{VOff} is the drain current of the device at $V_{gs} = V_{OFF}$. The SS_{AVG} shows a significant improvement from 57 mV/decade in mono dielectric gate to 48 mV/decade in the hetero dielectric DMG-DGTFET.

In this section, transfer characteristic with respect to drain voltage are simulated and analyzed for different value of gate voltage. The saturation voltage in the output characteristics are evaluated as the value of drain voltage for which the drain current reaches 95% of its final value. For DMG-DGTFET based on hetero dielectric gate material the value of V_{dsat} comes out to be 0.85, 0.81, 0.76, and 0.70 for the following gate voltages 1, 0.9, 0.8 and 0.7 respectively. For mono dielectric, the value of V_{dsat} is similar to the hetero dielectric case as the value of I_{on} is similar for both the cases (Fig. 6).

The band-to-band generation is also simulated for different values of gate voltage and is shown in Fig. 7. The band-to-band generation rate is simulated by using Kane dispersion relationship and WKB approximation [36]. WKB approximation assumes the barrier to be slowly varying with distance, so that the solution of Schrodinger equation is exponential only, with amplitude and phase that varies slowly compared to de Broglie wavelength. Tunneling probability is calculated using WKB approximation, which is then reflected into kane dispersion relationship to give the BTBT generation rate. With Kane's equation, the peak electron generation rate ($G_{tun.max}$) by BTBT is found to be.

$$G_{tun \cdot max} = A\frac{E_G^{3/2}}{q^2} \cdot \frac{1}{W_{t \cdot min}^2} \exp\left[-\frac{-q \cdot W_{t \cdot min}}{B \cdot E_G^{1/2}}\right] \quad (3)$$

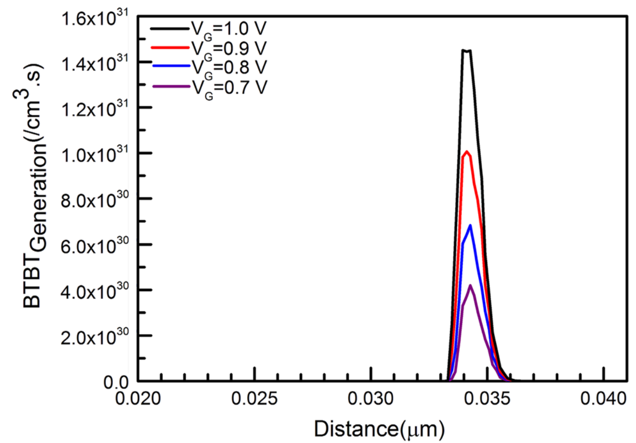

Fig. 7 Band-to-band generation rate for DMG-DGTFET based on hetero gate dielectric ($V_{gs} = 1.0, 0.9, 0.8$ and 0.7, $\phi_{aux} = 4.4$ eV, $\phi_{tun.} = 4.0$ eV) for $V_{DS} = 1.0$ V

Table 1 Comparison of various parameters for DMG (ϕ_{aux} = 4.4 eV, $\phi_{tunn.}$ = 4.0 eV) technique for mono and hetero dielectric. Mono dielectric = HfO_2, Hetero dielectric = $SiO_2 + HfO_2$

Technique	I_{on} (A/um)	I_{off} (A/um)	I_{on}/I_{off}	SS_{avg} (mV/decade)
DMG mono dielectric	2.48e−5	9.8e−14	2.5e+8	58
DMG hetero dielectric	2.48e−5	1.2e−14	2.0e+9	48

where, $w_{t \cdot min}$ is the tunneling barrier width.

As the value of V_G increases minimum barrier width reduces at the junction, which increases the BTBT generation rate as shown above.

5 Results

The comparison of DMG-DGTFET with mono and hetero dielectric gate is shown in Table 1. We have not compared the SMG with DMG because the bias points of both the techniques are not same. It is evident from the results that using hetero dielectric with DMG technique results in further improvement of the I_{ON}/I_{OFF} ratio and SS_{avg} because of the reasons explained earlier.

6 Conclusion

The DMG technique, when applied to DGTFET results in individual control for the different section of the transfer characteristics by adjusting the work function of the metal, and results in improvement of the I_{ON}/I_{OFF} ratio and average subthreshold slope, and by the use of different dielectrics under the gates (Hetero Dielectric) the performance can be

improved further as it can be seen from the results. The use of high-k dielectrics results in the degradation of the mobility at the interface due to columbic scattering, degradation can be improved by using Retro grade kind of doping profile, where the doping is kept low at the surface and high in the body. Thus we can see that DMG along with hetero dielectric provides a very powerful technique to boosts the performance of DMG-DGTFET.

Fabrication difficulty are there to fabricate DMG-DGTFET based on hetero dielectric gate The use of hetero dielectric at the gate along with DMG technique adds complexity to the device fabrication and fabrication becomes more challenging as the device dimension scale down.

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