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A full-range dual material gate tunnel field effect transistor drain current model considering both source and drain depletion region band-to-band tunneling

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Abstract In this paper, a 2-D analytical model for the drain current of a dual material gate tunneling field-effect transistor is developed incorporating the effects of source and drain depletion regions. The model can forecast the effects of drain voltage, gate work function, oxide thickness, and silicon film thickness. The proposed model gives analytical expressions for the surface potential, electric field and the band to band generation rate which is numerically integrated to give the drain current. More importantly, our model accurately predicts the ambipolar current and the effects of drain voltage in the saturation region. A semi-empirical approach is used to model the transition from the linear to the saturation region, leading to an infinitely differentiable characteristics. The model is shown to be scalable down to a gate length of 50 nm. The model validation is carried out by a comparison with 2-D numerical simulations.

Keywords Analytical modeling · Band to band tunneling · Poisson equation · Ambipolar current · Dual material gate (DMG) · Tunneling field-effect transistor (TFET)

1 Introduction

Tunneling field-effect transistors (TFETs) have been extensively studied as an attractive alternative to conventional MOSFETs in ultralow power applications [1–9]. They have been shown to exhibit subthreshold swing (SS) below 60 mV/decade, low OFF-state leakage currents, and diminished short-channel effects (SCEs). However, TFETs also have problems related to ON-state current lower than ITRS requirements [3–8] and DIBL effects [10]; a Dual Material Gate (DMG) TFET had been proposed to address these [11]. The application of DMG is one of the several methods [3,12,13] that are being studied to increase the ON-state current of TFETs. Of these methods, the DMG TFET has the advantage of compatibility with the current CMOS fabrication technology. The DMG structures have been shown to give enhanced ON-state current [11,14]. Therefore, modeling the drain current of the DMG TFET is of great interest. A DMG TFET (see Fig. 1) has a gate made of two different metals, both connected to the same terminal and having the same voltage. The tunneling gate has a lower work function than the auxiliary gate for an n-channel TFET (vice-versa for a p-channel TFET). This leads to a higher ON-state current, lower OFF-state current, and better SS than a conventional TFET [11,14]. The fabrication of a DMGTFET using a self-aligned symmetric spacer process [15] has been extensively studied [16–18].

While a number of analytical models have been proposed for the SMGTFET [19–25], most of the studies on a DMGTFET have used TCAD numerical simulations. In the previous models on DMG TFET [26,27], a single tunneling length was used and therefore, they were not accurate in the subthreshold region. Moreover, as these models did not consider the band to band tunneling simultaneously in the source and the drain depletion regions, they were not able to predict the ambipolar current.

Therefore, this paper develops a 2-D model for the DC drain current of a DMG TFET considering the source and drain depletion regions band to band tunneling. The proposed model is able to predict the drain current accurately in the subthreshold region, the ON-state (strong inversion), and the OFF-state including the ambipolar current. The model results are verified by a comparison with 2-D numerical simulations [28].

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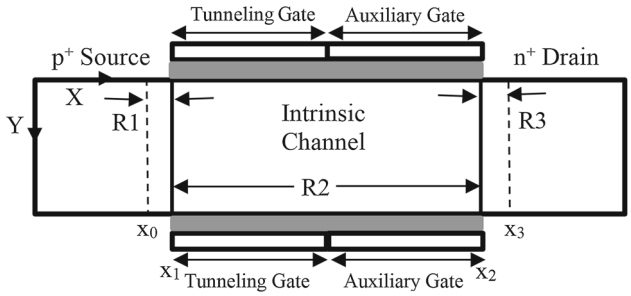

Fig. 1 Schematic of the n-channel DMG DG TFET being modeled.

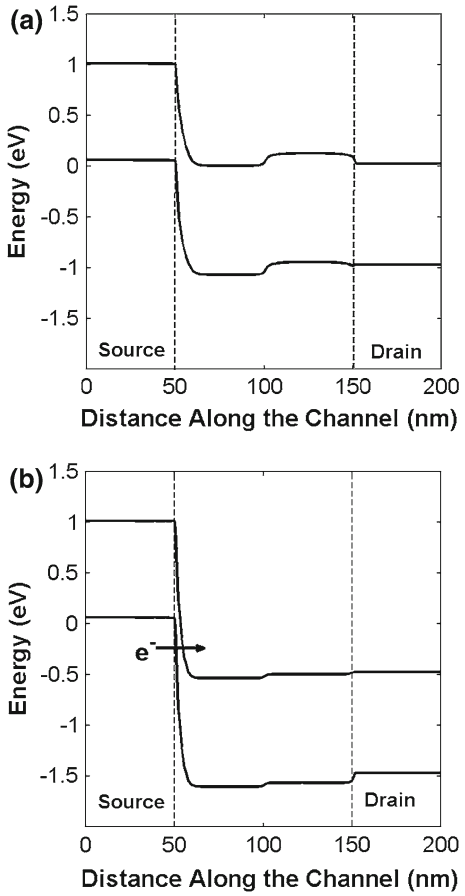

Fig. 2 Band diagrams for the DG DMG TFET in the **a** OFF-state ($V_{DS} = 0\,V$, $V_{GS} = 0\,V$) and the **b** ON-state ($V_{DS} = 0.5\,V$, $V_{GS} = 1.0\,V$).

2 Model derivation

The model is derived for a double gate DMG n-channel TFET (Fig. 1). The corresponding band diagrams for the DG DMG TFET in the (a) OFF-state ($V_{DS} = 0\,V$, $V_{GS} = 0\,V$) and the (b) ON-state ($V_{DS} = 0.5\,V$, $V_{GS} = 1.0\,V$) are shown in Fig. 2. Tunneling occurs when the energy barrier separating the valence band of the source and the conduction band of the channel is sufficiently thin. The entire device is divided into separate regions as follows. R1 is the source depletion region and R3 is the drain depletion region. R2 is the channel, which is further sub-divided into R2t, the region under the tunneling gate, and R2a, the region under the auxiliary gate. The device parameters are: channel length (L_2) = 100 nm, silicon film thickness (t_{Si}) = 10 nm, oxide thickness (t_{ox}) = 2 nm, p-type source doping (N_1) = 10^{20} cm^{-3}, n-type channel doping (N_2) = 10^{17} cm^{-3}, n-type drain doping (N_3) = 10^{19} cm^{-3}, the tunneling gate work function (Φ_t) = 4.0 eV, and the auxiliary gate work function (Φ_a) = 4.4 eV. The length of the tunneling gate (L_{2t}) and the auxiliary gate (L_{2a}) is taken to be 50 nm each in the initial calculations; results for the case of tunneling gate length of 20 nm and auxiliary gate length of 30 nm are also shown. The electron affinity (χ_{Si}) = 4.17 eV and silicon bandgap (E_G) = 1.1 eV are taken from the default values used in ATLAS [28].

First, the 2-D Poisson's equation is solved to obtain a general solution. This solution, the values of the source and drain depletion region lengths, and the appropriate boundary conditions are used to calculate the potential and the electric field throughout the device. The electric field is then substituted into Kane's model [29] to extract the drain current. In the derivations that follow, all potentials are referenced with respect to the substrate.

2.1 2-D Poisson's equation

As shown in [25], the mobile charges have negligible effect on the electrostatics of the device as it undergoes a transition from the OFF-state to the ON-state. Since this is the regime that is of primary interest, the Poisson's equation can be written as

$$\frac{\partial^2\psi(x,y)}{\partial x^2} + \frac{\partial^2\psi(x,y)}{\partial y^2} = -\frac{qN}{\varepsilon_{Si}} \tag{1}$$

where $\psi(x, y)$ is the electrostatic potential in the region of consideration, N is the doping, q is the electronic charge, and ϵ_{Si} is the dielectric constant for silicon.

The potential along Y-direction can be approximated by the second-order polynomial [30]:

$$\psi(x,y) = c_0(x) + c_1(x)y + c_2(x)y^2. \tag{2}$$

To evaluate $c_0(x)$, $c_1(x)$, and $c_2(x)$, four boundary conditions in Y-direction must be imposed. Due to the continuity of potential at the front and back side body-oxide interfaces, respectively, we have two boundary conditions:

$$\psi_i(x,0) = \psi_s(x) \tag{3a}$$

$$\psi_i(x,t_{Si}) = \psi_b(x) = \psi_s(x). \tag{3b}$$

And due to the continuity of the vertical electric displacement at the front and back side body-oxide interfaces, respectively, we can write two more boundary conditions:

$$D_y(x,0) = -\varepsilon_{Si} c_1(x) = -\varepsilon_{ox}\frac{\psi_s(x)-\psi_g}{t_{ox}} \tag{3c}$$

$$D_y(x,t_{Si}) = -\varepsilon_{Si}(c_1(x)+2c_2(x)y) = -\varepsilon_{ox}\frac{\psi_g-\psi_s(x)}{t_{ox}} \tag{3d}$$

where $\psi_s(x)$ = the front side surface potential (at $y = 0$), $\psi_b(x)$ = the back side surface potential (at $y = t_{Si}$), electric displacement $D_y = \epsilon_{Si} E_y$, and E_y = the electric field in Y-direction. The gate potential is different for both the gates; the tunneling gate potential $\psi_{g2t} = V_g - \Phi_t + \chi_{Si} + E_G/2$, and the auxiliary gate potential $\psi_{g2a} = V_g - \Phi_a + \chi_{Si} + E_G/2$. From the symmetry of the device, we can write $\psi_s(x) = \psi_b(x)$.

The eqs. (3a)–(3d) can be solved to give the functions $c_0(x)$, $c_1(x)$, and $c_2(x)$ in terms of the front side surface potential $\psi_s(x)$ as

$$\begin{aligned} c_0(x) &= \psi_s(x) \\ c_1(x) &= \eta\frac{\psi_s(x)-\psi_g}{t_{Si}} \\ c_2(x) &= \eta\frac{\psi_g-\psi_s(x)}{t_{Si}^2} \end{aligned} \tag{4}$$

where η is the capacitance ratio of gate oxide and silicon film, i.e. $\eta = C_{ox}/C_{Si}$. The gate oxide capacitance is $C_{ox} = \epsilon_{ox}/t_{ox}$ for the intrinsic channel region R2. Conformal mapping techniques are used to take into account the fringing field effect of the gate in the depletion regions R1 and R3 [31–33], thereby giving the oxide capacitance as $C_{ox} = 2/\pi \times \epsilon_{ox}/t_{ox}$. The silicon film capacitance $C_{Si} = \epsilon_{Si}/t_{Si}$. From (4), $c_0(x)$, $c_1(x)$, and $c_2(x)$ can be substituted into (2). The resultant expression when substituted into the 2-D Poisson's eq. (1) leads to a 1-D differential equation in $\psi_s(x)$:

$$\frac{\partial^2\psi_s(x)}{\partial x^2} - k^2\psi_s(x) = -k^2\psi_c \tag{5}$$

where

$$\begin{aligned} k &= \sqrt{2\eta/t_{Si}^2} \\ \psi_c &= \psi_g - \frac{qN}{k^2\varepsilon_{Si}} \end{aligned} \tag{6}$$

where $1/k$ is the decay length or characteristic length for the surface potential $\psi_s(x)$ in each region, and has different values in the source (R1), the channel (R2), and the drain (R3) regions. The parameter ψ_c has different values in all the four regions, i.e. the source (R1), the tunneling gate (R2t), the auxiliary gate (R2a), and the drain (R3) regions.

Equation (5) is solved individually for each region (R1, R2a, R2t, and R3). The solution for the i^{th} region (i=1, 2t, 2a and 3) is

$$\psi_{s,i}(x) = a_i e^{-k_i(x-x_{i-1})} + b_i e^{k_i(x-x_{i-1})} + \psi_{ci} \tag{7}$$

where k_i and ψ_{ci} are the parameters defined in (6) for the i^{th} region. To get the complete solution for the surface potential throughout the device, a_i and b_i need to be solved for.

The surface potential $\psi_s(x)$ from (7) is used to find the variation of potential in the Y-direction. This can be done by substituting the surface potential $\psi_s(x)$ from (7) into (4), and further substituting the expressions thus obtained for $c_0(x)$, $c_1(x)$, and $c_2(x)$ into (2). The negative of the partial derivatives of the potential with respect to x and y would give the electric fields in the x and y direction respectively.

$$E_{x,i}(x,y) = k_i(a_i e^{-k_i(x-x_i)} - b_i e^{k_i(x-x_i)})(1+\eta y/t_{Si} - \eta y^2/t_{Si}^2) \tag{8a}$$

$$E_{y,i}(x,y) = -c_1(x) - 2c_2(x)y. \tag{8b}$$

2.2 Pinning the channel potential

From analytical models that incorporate the effects of drain voltage on the surface potential [14–19], as well as from simulations, it is observed that an inversion charge layer forms in the channel at large positive and negative gate voltages. This inversion charge leads to the 'pinning' of the channel potential in both the cases. For an n-channel TFET, the channel potential $\psi_{channel}$ is observed to vary as:

$$\Psi_{source} + \Phi_{bi,source} \le \psi_{channel} \le \Psi_{drain} + \Phi_{bi,drain}. \tag{9}$$

where Ψ_{source} is the source potential and Ψ_{drain} is the drain potential. Φ_{bi} is the built-in potential across the respective junction, and can be given as [36]:

$$\Phi_{bi,drain} = \frac{kT}{q}\ln\frac{n_{channel}}{n_{drain}} \tag{10a}$$

$$\Phi_{bi,source} = \frac{kT}{q}\ln\frac{n_{channel}}{n_{source}} = -\frac{kT}{q}\ln\frac{p_{channel}}{p_{source}} \tag{10b}$$

where $n_{channel}$ is the electron concentration of the inversion layer formed in the channel when drain side pinning occurs (i.e. when $\psi_{channel} \ge \Psi_{drain}$), and is observed in simulations to be 10^{21} cm^{-3}; n_{drain} is the electron concentration in the drain. Similarly, $p_{channel}$ is the hole concentration of the inversion layer formed in the channel when source side pinning occurs (i.e. when $\psi_{channel} \le \Psi_{source}$), and is observed in simulations to be 10^{21} cm^{-3}; p_{source} is the hole concentration in the source.

In the channel regions, R2t and R2a, the term $\psi_{ci}|_{i=2t,2a}$ in (7) is the potential solely due to the biasing of the gates. To appropriately capture the behavior of the channel potential as described in (9), a semi-empirical parameter called the "effective gate potential" $\psi_{gi,eff}$ (i=2t, 2a) is introduced. This parameter varies such that when $\Psi_{source} + \Phi_{bi,source} \le \psi_{gi} \le \Psi_{drain} + \Phi_{bi,drain}$, we have

$$\psi_{gi,eff} = \psi_{gi} \tag{11a}$$

when $\psi_{gi} \geq \Psi_{drain} + \Phi_{bi,drain}$,

$$\psi_{gi,eff} = \Psi_{drain} + \Phi_{bi,drain} \tag{11b}$$

and when $\psi_{gi} \leq \Psi_{source} + \Phi_{bi,source}$

$$\psi_{gi,eff} = \Psi_{source} + \Phi_{bi,source} \tag{11c}$$

The parameter $\psi_{gi,eff}$ so defined is used in place of the gate potential ψ_{gi} for calculating the potential and the electric field in the device.

To model the transitions from (11a) to (11c), a semi-empirical approach is adopted by using the following smoothing function [34,35]:

$$\psi_{gi,eff} = \psi_{gi} - \varphi_{t1} \ln\left(1 + e^{\frac{\psi_{gi} - \Psi_{drain} - \Phi_{bi,drain}}{\varphi_{t1}}}\right) + \varphi_{t2} \ln\left(1 + e^{\frac{\Psi_{source} + \Phi_{bi,source} - \psi_{gi}}{\varphi_{t2}}}\right) \tag{12}$$

where ϕ_{t1} and ϕ_{t2} are empirical smoothing parameters whose values can be obtained by fitting the simulated and the modeled transfer characteristics. The smoothing parameters must be recalibrated if different doping levels are simulated; they remain constant across variations in gate work-functions and gate lengths. Since most circuit simulators use only a single device structure with fixed parameters and at most vary the size of the device, this should not limit the applicability of the model. The above function ensures the continuity and infinite differentiability of the potential, leading to the continuity and infinite differentiability of all the obtained characteristics.

2.3 Length of depletion regions

To obtain accurate values of the source and drain depletion region lengths, certain boundary conditions need to be imposed. From the continuity of electric field and potential, respectively, at the end of the source depletion region (i.e. $x = x_0$):

$$E_x(x_0, y) = 0 \tag{13a}$$

$$\psi_{s1}(x_0) = \Psi_{source}. \tag{13b}$$

Similarly, from the continuity of electric field and potential, respectively, at the end of the drain depletion region (i.e. $x = x_1$):

$$E_x(x_3, y) = 0 \tag{13c}$$

$$\psi_{s1}(x_3) = \Psi_{drain}. \tag{13d}$$

Since the set of equations (13) are transcendental in nature, solving them is analytically complex and computationally cumbersome.

The source-channel (under the tunneling gate) and channel (under the auxiliary gate)-drain junctions are, therefore, approximated as diodes so that the depletion region length can be modeled using the junction potential [36]. The junction potential is taken to be the difference between the source (or drain) potential and ψ_{c2t} (or ψ_{c2a}) which is the potential in the silicon body solely due to the gate voltage. This would give the depletion region lengths as:

$$L_1 = \sqrt{((2\varepsilon_{Si}\,|\psi_{c2} - \Psi_{source}| \times |N_2|)/([q\,|N_1| \times (|N_1| + |N_2|)]))} \tag{14a}$$

$$L_3 = \sqrt{((2\varepsilon_{Si}\,|\Psi_{drain} - \psi_{c2}| \times |N_2|)/([q\,|N_3| \times (|N_1| + |N_3|)]))} \tag{14b}$$

where L_1 and L_3 are the lengths of the source depletion region (R1) and the drain depletion region (R3), respectively. It should be noted that in (14), the values of ψ_{c2t} and ψ_{c2a} are calculated using $\psi_{g2t,eff}$ and $\psi_{g2a,eff}$, respectively.

2.4 Solution for surface potential

To obtain the coefficients a_i and b_i in (7), the following horizontal boundary conditions need to be imposed. Equations (15a) and (15b) specify the continuity and differentiability, respectively, of the surface potential across the three horizontal interfaces. The interfaces under consideration are: (a) the source-channel (under the tunneling gate) interface for $i = 1$, $j = 2t$; (b) the interface between the channel under the tunneling gate and the channel under the auxiliary gate for $i = 2t$, $j = 2a$; and (c) the interface between the channel under the auxiliary gate and the drain for $i = 2a$, $j = 3$.

$$\psi_{s,i}(x_i) = \psi_{s,j}(x_i) \tag{15a}$$

$$\psi'_{s,i}(x_i) = \psi'_{s,j}(x_i). \tag{15b}$$

Also, as the surface potential in the source and the drain depletion regions drop to the source potential (Ψ_{source}) at $x = x_0$ and the drain potential (Ψ_{drain}) at $x = x_3$, respectively, we must have:

$$\psi_{s1}(x_0) = \Psi_{source} = V_{source} - \frac{kT}{q} \ln|N_1/n_i| \tag{15c}$$

$$\psi_{s3}(x_3) = \Psi_{drain} = V_{drain} + \frac{kT}{q} \ln|N_3/n_i| \tag{15d}$$

where V_{source} is the source voltage and V_{drain} is the drain voltage.

The terms a_{i+1} and b_{i+1} can be written in terms of a_i and b_i by substituting $\psi_{s,i}$ from (7) into (15a) and (15b) and rearranging the resultant equations:

$$2b_{i+1} = \left(1 - \frac{k_i}{k_{i+1}}\right) e^{-k_i L_i} a_i + \left(1 + \frac{k_i}{k_{i+1}}\right) e^{k_i L_i} b_i + (\psi_{ci} - \psi_{ci+1}) \quad (16a)$$

$$2a_{i+1} = \left(1 + \frac{k_i}{k_{i+1}}\right) e^{-k_i L_i} a_i + \left(1 - \frac{k_i}{k_{i+1}}\right) e^{k_i L_i} b_i + (\psi_{ci} - \psi_{ci+1}) . \quad (16b)$$

The values for a_1 and b_1 are given in the "appendix", and the other coefficients can be found by substituting those values in (16).

2.5 Drain current

The band-to-band generation rate G_{btb} is numerically integrated throughout the device to give the drain current:

$$I_D = q \int G_{btb} dV . \quad (17)$$

G_{btb} is given by Kane's Model [29] as:

$$G_{btb} = A \frac{|E^{2.5}|}{\sqrt{E_G}} \exp\left[-B \frac{E_G^{3/2}}{|E|}\right] . \quad (18)$$

where E_G is the silicon bandgap and $|E| = \sqrt{E_x^2 + E_y^2}$ is the magnitude of the electric field at a given point. The electric fields E_x and E_y are given by (8a) and (8b) respectively.

3 Model validation

The accuracy of the proposed model is verified by comparing the results with 2D numerical simulations. The device structure shown in Fig. 1 is simulated using Silvaco ATLAS [28]. The models used in our simulations are: concentration dependent mobility, electric field dependent mobility, SRH recombination, auger recombination, band gap narrowing, Fermi-Dirac carrier statistics, and Kane's band to band tunneling, and have been calibrated as described in [27].

The surface potential given by the model and the simulations are compared in Fig. 3 for different values of applied gate and drain voltages, V_{GS} and V_{DS}, respectively. The model results are in good agreement with the simulation results. In Fig. 4, the electric field along the surface from the model and simulations is compared, and we observe that the results match well. Fig. 5 shows the I_D–V_{GS} curves given by the model and the simulations for $V_{DS} = 0.5$ V. It can be seen that the model accurately predicts the drain current in the positive as well as the negative ranges of the gate voltage, both on the logarithmic and linear scale. This is due to the incorporation of the effect of the drain side tunneling, thus leading to the prediction of the ambipolar current. Also, as numerical integration of the band-to-band generation rate

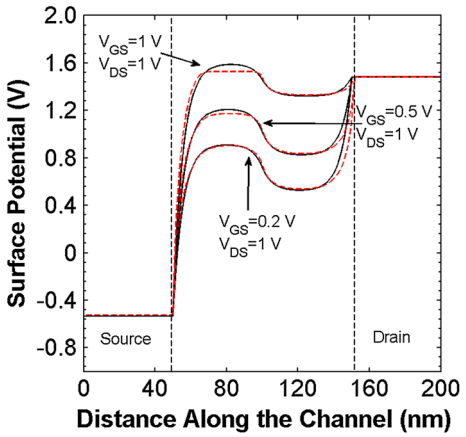

Fig. 3 Surface potential along the channel given by our model (*solid lines*) and TCAD simulations (*dashed lines*) for three biasing conditions.

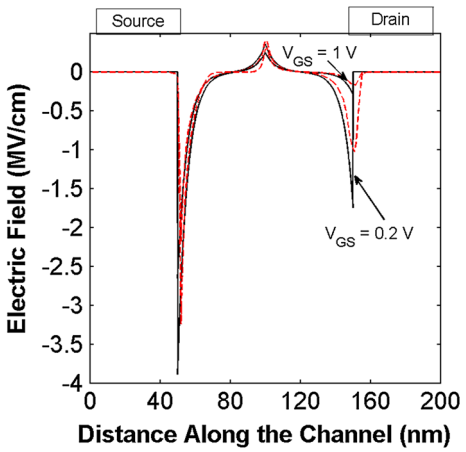

Fig. 4 Electric field (x-direction) at the surface along the channel given by our model (*solid lines*) and TCAD simulations (*dashed lines*) for two gate biasing conditions at $V_{DS} = 1$ V.

has been carried out over the entire device structure rather than using a single tunneling length, the model is able to accurately predict the subthreshold characteristics.

In Fig. 6, the surface potentials from our model and TCAD simulations are compared for devices with a fixed total gate length of 100 nm and varying tunneling gate lengths. In Fig. 7, the I_D–V_{GS} characteristics of a TFET with a total gate length of 50 nm and a tunneling gate length of 20 nm are shown. The results shown in Figs. 6 and 7 demonstrate that the proposed model is scalable down to a tunneling gate length of 20 nm and a total gate length of 50 nm.

The transfer characteristics of SMG TFET and DMG TFET are compared in Fig. 8. As can be observed in the figure, an SMG TFET with a gate of lower work function (Fig. 8, curve a) will have a higher ON-state current, but suffers from a low SS due to high OFF-state current. An SMG TFET with a gate of higher work function (Fig. 8, curve b)

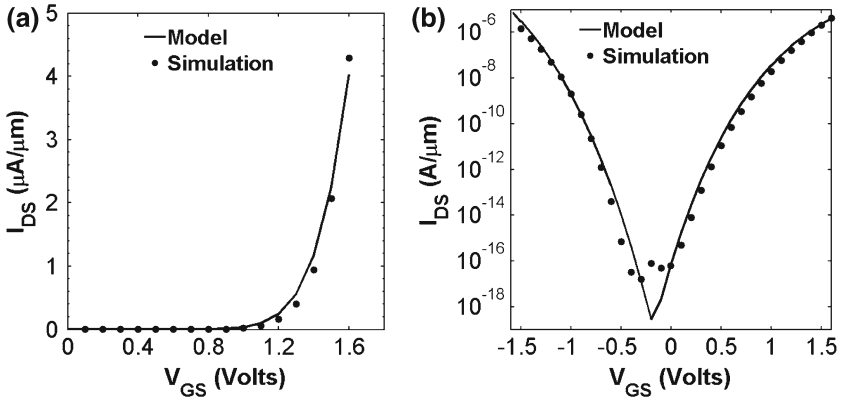

Fig. 5 $I_D - V_{GS}$ given by our model (*solid lines*) and TCAD simulations (*dots*) at $V_{DS} = 0.5$ V on **a** a linear scale, and **b** a logarithmic scale

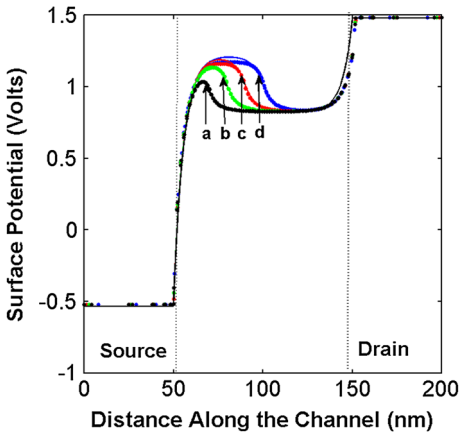

Fig. 6 Surface potential along the channel given by our model (*solid lines*) and TCAD simulations (*dots*) for $V_{DS} = 1.0$ V and $V_{GS} = 0.5$ V for gate length 100 nm, and different tunneling gate lengths: **a** 20 nm, **b** 30 nm, **c** 40 nm, and **d** 50 nm.

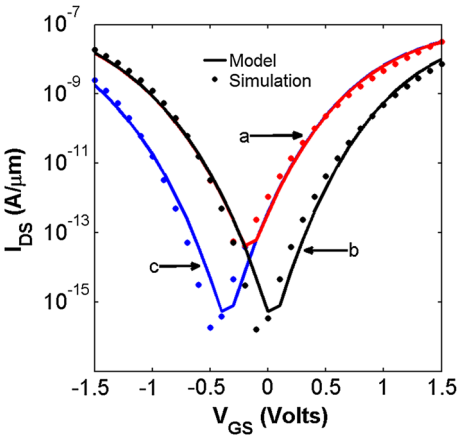

Fig. 8 Comparison of transfer characteristics obtained by our model and TCAD simulations for **a** an SMG TFET (*red*) with a gate of 50 nm length and 4.0 eV work function, **b** an SMG TFET (*black*) with a gate of 50 nm length and 4.4 eV work function, and **c** a DMG TFET (*blue*) with a tunneling gate having 25 nm length and 4.0 eV work function, and an auxiliary gate having 25 nm length and 4.4 eV work function.

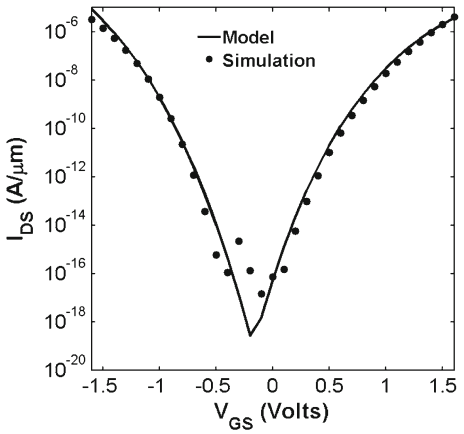

Fig. 7 $I_D - V_{GS}$ given by our model (*solid lines*) and TCAD simulations (*dots*) at $V_{DS} = 0.5$ V for a channel length of 50 nm having a tunneling gate length of 20 nm and an auxiliary gate length of 30 nm.

will have a lower OFF-state current, and thus a better SS, but its ON-state current is also low. A DMG TFET (Fig. 8, curve c) is able to combine the characteristics of both these devices, exhibiting a high ON-state current, a low OFF-state current, and a high SS. Our model can, therefore, be used to vary the gate work functions and achieve the optimal combination of ON-state current and SS as dictated by the design requirements.

4 Conclusion

In this work, a model is developed for the surface potential, electric field, and the drain current of a DMG double gate TFET that includes the effects of the source and the drain depletion regions. The variation in the channel potential with gate and drain biases is accurately captured by a semi-empirical approach that gives an infinitely differentiable transfer characteristics. This is needed for circuit design and simulation. The ambipolar current is accurately predicted by our model due to the incorporation of both the source and the drain side depletion region tunneling. The accuracy of the model is validated against calibrated 2-D numerical simulations. The model is accurate in both the

subthreshold and the ON-state (strong inversion) regions of operation.

Appendix

The coefficients a_1 and b_1 for the source depletion region (R1) are found by applying the boundary conditions as given in (16) and solving the resultant six linear equations in the six variables a_i and b_i:

$$
\begin{aligned}
a_1 &= e^{-k_2L_2-k_3L_3} \\
&\times \begin{pmatrix}
e^{k_1L_1}\left(\Psi_{source}-\psi_{c1}\right)\begin{pmatrix}\Delta k_{23}(\Delta k_{12}e^{2k_3L_3}-\Sigma k_{12}e^{2k_2L_2}) \\ +\Sigma k_{23}(\Sigma k_{12}e^{2k_2L_2+2k_3L_3}-\Delta k_{12})\end{pmatrix} \\
+k_2\Delta\psi_{1,2t}\begin{pmatrix}\Delta k_{32}(e^{2k_2L_2}+e^{2k_3L_3}) \\ +\Sigma k_{32}(1+e^{2k_2L_2+2k_3L_3}\end{pmatrix} \\
+k_2e^{k_2L_{2t}}\Delta\psi_{2a,2t}\begin{pmatrix}\Delta k_{23}(e^{2k_2L_{2a}}+e^{2k_3L_3}) \\ -\Sigma k_{23}(1+e^{2k_2L_{2a}+2k_3L_3})\end{pmatrix} \\
+2k_2k_3e^{k_2L_2}\Delta\psi_{2a,3}(1+e^{2k_3L_3})+4(\Psi_{drain}-\psi_{c3})e^{k_2L_2+2k_3L_3}
\end{pmatrix} \\
b_1 &= \Psi_{source}-\psi_{c1}-a_1. \qquad (19)
\end{aligned}
$$

Here additional symbols $\Delta\psi_{i,j}$, Δk_{ij} and Σk_{ij} have been defined for compact representation of the coefficients a_1 and b_1:

$$
\begin{aligned}
\Delta\psi_{i,j} &= \psi_{ci}-\psi_{cj} \\
\Delta k_{ij} &= k_i-k_j \\
\Sigma k_{ij} &= k_i+k_j \qquad (20)
\end{aligned}
$$

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