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A compact modelling of double-walled gate wrap around carbon nanotube array field effect transistors

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Abstract The effects of multi-walled CNTs and array of channels are combined to form Double-walled Gate Wrap Around Carbon Nano Tube array Field Effect Transistor (DWGWA CNTFET). Numerical model is proposed for the device to study its performance. Screening and imaging effects of adjacent and inter walls in array of channels are included for calculating the drive capacitance, subsequently the drive current. This model suits for a wide range of chiralities and diameters. The change in drive capacitance of double-walled and single-walled device with respect to various drain and gate voltage for different values of number of channels, diameters are studied. The number of channels, CNTs diameters, chiralities of the tubes, source/drain length are varied and the corresponding responses of drive current, cut off frequency, signal delay time for both double and single walled devices are compared. In all cases, DWGWA CNTFET excels in its performance over Single-walled Gate Wrap Around Carbon Nano Tube array Field Effect Transistor (SWGWA CNTFET).The model of the proposed device can be utilized for designing the Nano devices with high power and high speed capability.

Keywords Screening effects · Chirality · Gate wrap around transistor · Multi walled CNT · High gate dielectric · Cut-off frequency · Delay time

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1 Introduction

Carbon nanotube is most expected potential challenger which will replace Si in near future with high electrical performance. With ballistic transport, larger drive current flow is found in CNTFET compared to its Si counterpart and excels in its output. The strengths of CNT are explored highly in the past decade. It will occupy a greater space in electronic world with its unique physical, electrical, chemical and mechanical features. CNTFET hold ballistic transport with high carrier velocity due to ultra-long mean free path (MFP). Highly aligned CNTs can be grown on full wafer scale for the construction of complex logic gates with stable and complementary n- and p-channel MOSFETs on single chip.

It is necessary for a device to operate at room temperature. Tans et al. [1] in their work reported about the fabrication of semiconducting carbon nanotube FET. The device operates at room temperature with high switching speed. They utilize semi classical band-bending models for explaining device electrical characteristics. Javey et al. shares the work on contacts of semiconducting Single-walled Carbon Nano Tube transistor (SWCNT). It is specified that if the contacts of Nano tubes are with high work function and with wetting interactions like palladium, then the transport barrier through valence band of the tube is greatly reduced. Using square law model it is concluded that diffusive transport model does not suit for the short channel length Nano tube devices, only ballistic transport model holds good [2].

Furthermore, a fabrication technic for CNTFETs to show high electrical performance is described by Radosavljevic et al. [3]. By exposing potassium (K) vapour and high vacuum device annealing the contact metal is prepared. Current flow is improved due to low device resistance at K metal with the tube and due to voltage reduction of the Schottky barrier height at the K metal-channel contact. To achieve higher

electrical performance for semiconducting CNTFETs, Javey et al. [4] proposes the device with ohmic metal tube contact, for doped source/drain regions and high k dielectric material for gate-channel insulation. HfO_2 is chosen instead of SiO_2 for gate insulator. It is found that with all the above components, the device provides high ON and low OFF currents.

The effect of parasitic capacitances, screening or imaging of neighbouring channels and low channels density effects the performance of 1-D devices. By optimizing, the advantages of such devices can be quantified [5]. Wei et al. followed analytical and numerical simulation models to project the current improvement of 1-D devices.

Classification based on the number of enclosed graphene sheets, CNTs are categorized into Single and Multi walled CNTs. For single-walled CNT substantial work has been done for studying and realizing the devices. But, complex structured multi-walled CNTs need more research work. The resistance is low in Multi-walled carbon nanotube (MWCNT) claims Nihei et al. [6]. It is lowered by optimizing the interface between the inter walls of MWCNTs and by parallel conduction of the channels. It is proved that MWCNT provides low resistance and high tolerance of migration. The density of MWCNT bundles has to be increased to reach the resistance of Cu wire. Li et al. [7] explored the details of interconnect performance of MWCNT. The inter connects are calculated and compared with Cu, Single-Walled CNT (SWCNT)-based, local, intermediate, and global interconnects. MWCNT experiences lesser signal delay over Cu. With significant improvement through scaling technology and increasing wire lengths, MWCNTs manage smaller signal delay. Moreover, fabrication of MWCNT is easier with little stress about the chirality and density control that can be used as horizontal wires in VLSI. To outperform MWCNT, SWCNTs need to be high and densely packed bundles.

SPICE model has been reported by Deng et al. [8] for an array of CNTFET including non-idealities for channel region and full device. Using HSPICE the work presents circuit-compatible model improving CV/I 13 times in the un-doped channel region with respect to bulk MOSFET. Same authors Deng et al. [9] in their next paper, included elastic scattering, the resistive source/drain, Schottky-barrier resistance and parasitic capacitance along with the non-idealities for modelling CNTFET. HSPICE is used and performance comparison is done with standard digital library cells between CNTFET and bulk CMOS random logic. It is found that CNTFET is faster than CMOS circuits by two to ten times with one to ten CNTs per gate. The energy consumption and energy delay product are lower. Applications and circuit features are also studied in [8,9].

Modelling of gate capacitance, fringing and gate-to-gate capacitance for array of planar gate CNTFET is done by Deng et al. [10]. All screening and imaging effects of neighbouring cylinders are included in the analytical model and verified with simulated numerical model. It is concluded from this paper that increasing the channel density and decreasing gate height will increase device speed. Double walled CNT is the simplest form of multi-walled CNTs and it is discussed and reported that it exhibits enhanced electrical characteristics like current and power handling capability [8,9,11,15]. Huang et al. [11] proposed a planar model of Double-Walled Carbon Nano tube field effect transistor (DWCNTFET) and proved that the device enhances in its current flow. The device is numerically modelled and partially verified using Non-equilibrium Green's function approach. The comparison of the electrical performance of proposed Double-Walled CNTFET with Single-Walled Carbon Nano tube field effect transistor (SWCNTFET) is also done. It is found that DWCNTFET has larger ON current, shorter delay and higher cut off frequency.

To drive larger current and larger capacitive loads, array of carbon Nano tubes are needed as reported by Wang et al. [12]. The three different configurations of gate electrode (a) bottom gate, (b) top gate and (c) wrap around gate CNTFET are studied and compared. It is concluded that the third category, wrap-around gate configuration gives the largest gate capacitance. The advantage of array of transistor improve the current drive capability of the CNTFET reports Wang et al. [13]. In their work three gate configurations are simulated and compared to prove that the gate wrap around transistor provides the largest gate capacitance. Array of surrounding gate CNTFET for single wall device is capacitance modelled by Akanda et al. [14]. Moreover, the proposed finite element method model includes all the screening effects and imaging effects of neighbouring channels due to multiple channels. Three key capacitances gate-channel capacitance, fringing capacitance and gate-to-gate capacitances are analytically modelled and verified with FEM model. The device has enhanced gate capacitance over the planar gate is the conclusion drawn from the work.

The performance of SWCNT and DWCNT bundle interconnects are compared with Cu wire to study the cross talks effects using numerical characterization. Crosstalk-induced time delay is reduced in DWCNTs compared to SWCNTs. So, DWCNT suits well in next generation technology due to its reduced time delay is in literature of Pu et al. [15]. Castro et al. [16] used small-signal equivalent circuit and solved Schrodinger–Poisson equation to predict the cut off frequency. Reason for f_t dependence on gate voltage is due to quasi-bound states in CNTs and the peak value is 600 GHz are found. Pulfrey [17] reviewed the response of CNTFET at high frequency. He stressed that an array of short length channels will help to improve the cut off frequency. The signal delay analysis done by simulation study shows that the same design used to design BJTs can also be used for CNTFET. It is found that the tunnelling barrier of the channel is the reason behind the larger signal delay Pulfrey et al. [18]. Numerical study of

Carrier transit delay and cut off frequency in graphene FET by Wang et al. [19] extracted carrier density delays.

In brief, Akanda et al. [14], proposed capacitance model for Wrap around CNTFET With Multi-CNTs. This paper discussed the gate wrap around device with single walled channel. Huang et al. [11] proposed, "Modelling and Performance Characterization of Double-Walled Carbon Nanotube Array Field-Effect Transistors". This research work details modelling of planar gate with double-walled channel CNTFET. Both papers consider array of channels. So, equations of gate wrap around are taken from [14], using the equations of double-walled array are from [11] and relations for new device are developed. Thus, the proposed GWA with double-walled channel array CNTFET is the combination of these two works.

This research paper, explores the chance of utilizing the superior electrical characteristics of Double-Walled Gate Wrap Around Carbon Nanotube Array Field Effect Transistors which includes the benefits of Gate Wrap Around CNTs, multi-channel CNTs and double wall CNTs. An effective model of DWGWA is proposed, studied and compared with its deepened competence over SWGWA. The screening or imaging effects of neighbouring channels and adjacent walls are included.

The paper is organized as follows. In Sect. 2, the structure of the device is explained with its geometric descriptions. With developed equivalent circuit, a set of equations is derived for calculating each distributed component is detailed in Sect. 3. Results and discussions for comparison of DWGWA with SWGWA are presented in Sect. 4. Drawn conclusions are discussed in Sect. 5.

2 Structure of the device

The structure of DWGWA is shown in the Fig. 1a and the device cross section in Fig. 1b, c. The device is 80 nm length and 48 nm width. The device is grown on Si base of 5 nm, the bulk dielectric of 10 μm, Gate height (Hgate) of 12nm and connecting electrode of 2nm thickness. Drain and Source regions are heavily doped and connected to both the inner and outer walls of DWGWACNTs whereas the channel region is un-doped.

The length of gate (Lg), source/drain (Lsd) are 16 and 32 nm respectively. The chiralities of outer and inner walls are (26,0), (17,0) [11] with diameter of do (outer wall) 2 and d_I (inner wall)1.34 nm.The inter space distance between the co-axial channel is 0.34 nm [9,11]. The pitch distance(s) and oxide thickness (Tox) are taken as 20 and 4 nm. The gate controls the current flow in the channel region through high-k dielectric material HfO_2 of value 16.The bulk dielectric k_2 has the value of 4.

3 Device modelling

High-k material Hfo_2 is taken for the insulator, since CNTFET provides high gate control with high-k insulator material in 1-D channel [4,11]. Equivalent circuit drawn for DWGWA is derived from [11] (Fig. 2). The current contributions of both the walls are marked as 'Io' for outer wall and 'I_I'inner wall. Here semiconductor-semiconductor combination is assumed since switching off FET for metal-semiconductor and metal-metal combination is not effective.

The details of the various capacitances per unit length are as below:

(a) *Cgc,o* is the electrostatic capacitance between gate and the outer wall of the channel
(b) *Cgc,I* is the electrostatic capacitance between gate and the inner wall of the channel
(c) *CoI* is the electrostatic capacitance between outer and inner wall of the channel due to coupling
(d) *Cgs,Cgd (Cgtg)* is the fringing capacitance between gate and source/drain or gate-to-gate capacitance.
(e) *Cfrg,g* is the fringing capacitance between gate and outer wall of the channel
(f) *Cfrg,sub* is the fringing capacitance between substrate and outer wall of the channel
(g) *Csub,o* is the electrostatic capacitance between substrate and the outer wall of the channel
(h) *Csub,I* is the electrostatic capacitance between substrate and the inner wall of the channel
(i) *Cgsub* is the electrostatic capacitance between gate and substrate.
(j) *Cqs,o* is the quantum capacitance between source and the outer wall of the channel
(k) *Cqs,I* is the quantum capacitance between source and the inner wall of the channel
(l) *Cqd,o* is the quantum capacitance between drain and the outer wall of the channel
(m) *Cqd,I* is the quantum capacitance between drain and the inner wall of the channel

3.1 Gate-channel capacitance *(Cgc)*

1-D device current mainly hinge on gate-to-channel capacitance for ballistic and quasi-ballistic transport providing larger current per unit gate width. The induced charge carriers in the channel governed by gate electric field are proportionate to *Cgc*. So, the gate to channel capacitance has to be calculated before finding the current flow through the device. Screening and imaging effects of neighbouring channels which are densely packed will reduce gate to channel capacitance (*Cgc*) and therefore those factors are to be included. The equations are derived from [10,11] and [14]

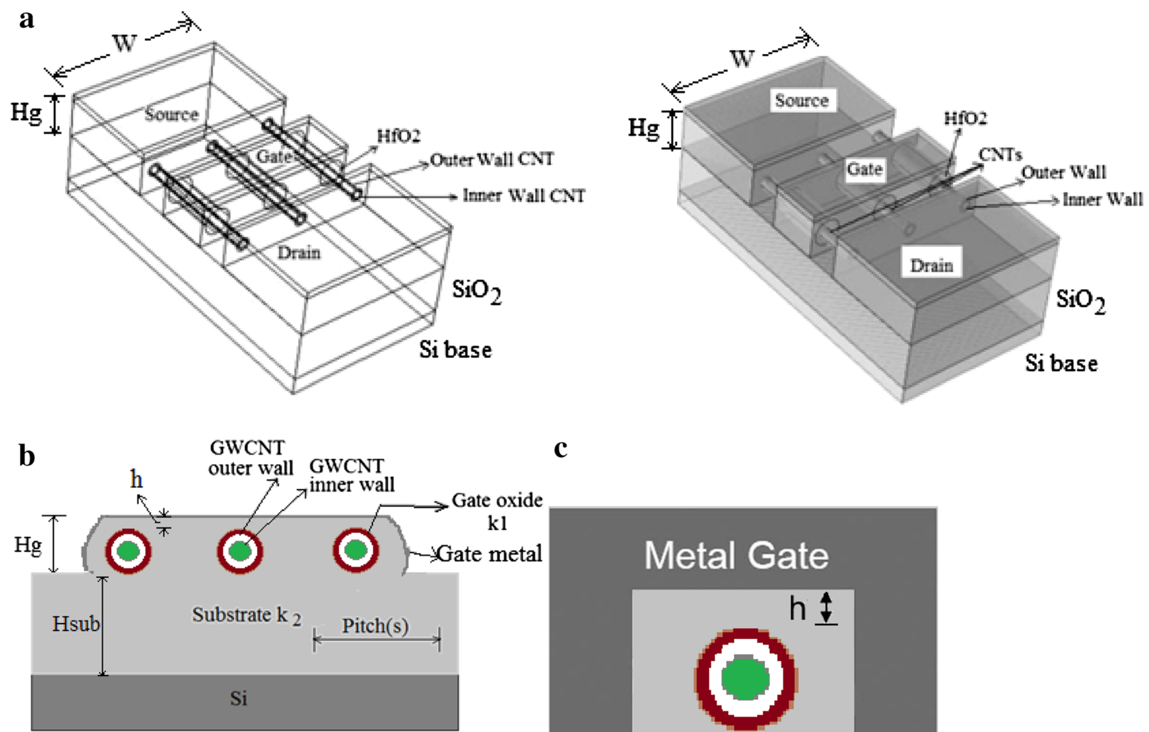
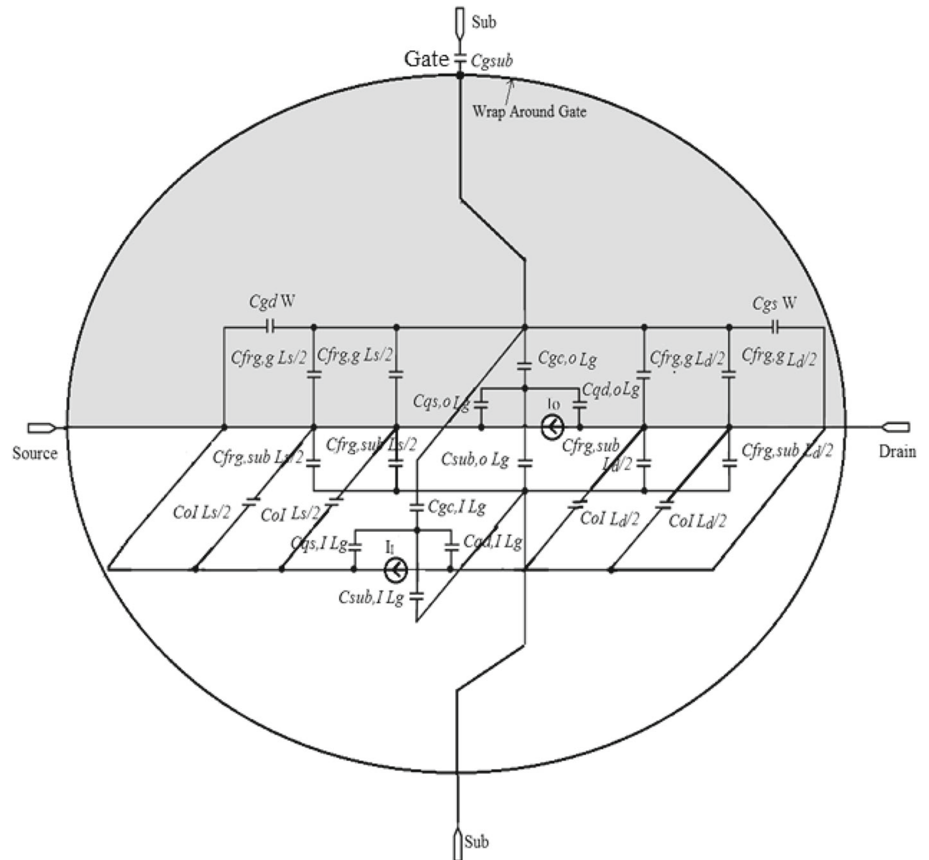


Fig. 1 **a** Internal 3-D Views of DWGWA CNTFET. **b**, **c** Cross sectional views of Gate Wrap Around Double walled Carbon Nanotube array FET

Fig. 2 Capacitive circuit model for DWGWA CNTFET



and the details are presented in Appendix 1. In an array of channels, the middle tube is affected by neighbouring channels at both the sides whereas the end tube does by the adjacent channels of one side only. So, both the capacitances with and without screening effects are included with separate calculations. The variation of end tubes gate to channel capacitance (*Cgc,e*), middle tube gate to channel capacitance (*Cgc,m*), total gate to channel capacitance (*Cgc*), gate to channel capacitance without screening effects (*Cgc,inf*) and drive capacitance ratios are studied with respect to dielectric value 'k1','s','h','Lsd'and 'N'. The drive capacitance ratio shows 1.6 to 2.0 times greater with respect to'k1', above 1.6 times for 's', about 1.5 times for 'h', 1.2 to 1.5 times for 'Lsd' and around 1.64 for 'N'. More the number of channels, larger the drive capacitance ratio. Larger the Hgate value, smaller the drive capacitance ratio. In all the cases, DWGWA exceeds SWGWA in its performance. Actual values are projected (Figs. 17, 18, 19, 20, 21) in Appendix 2.

3.2 Parasitic capacitance

The device speed is a mandatory calculation because it is a dependent factor upon parasitic capacitances [10,14]. The fringing capacitance between gate and the outer wall of the channel*(Cfrg,g)* and fringing capacitance between gate and source/ drain or gate-to-gate capacitance *Cgs,Cgd(Cgtg)* and capacitance between gate and substrate*(Cgsub)* are parasitic capacitances. There is no fringing effects due to inner wall on gate and substrate, as it is isolated well from gate and the substrate by outer wall of CNT. Outer fringing capacitances at the end, middle and total are plotted against the pitch distance(s) and 'h' distances. The capacitance values of DWGWA are greater than SWGWA [14]. It is found that capacitance values increases and nears 22 aF/m with 30 nm pitch distance and it is apparent that the increase in 'h' distance decreases the capacitance. The variation of gate-to-gate capacitance with respect to source/drain length (Lsd) DWGWCNTs shows that the values are in fF for SWGWA [14], in pF for planar gate cylindrical channels [10] and our model improves with values in nF. Another parasitic capacitance, the electrostatic capacitance between gate and substrate is calculated by 1) [9,11]. It is 0.083 nF/m for the proposed device, 2.84 times smaller than gate capacitance. In an array SWCNT C_{gsub} is about one third of gate capacitance [9].

$$C_{gsub} = 2\pi L_g k_2 \varepsilon_0 \big/ \ln\left(4H_{sub}/H_g\right) \tag{1}$$

3.3 Substrate capacitance

The substrate capacitance is an electrostatic capacitance between substrate and the channel. It can be divided into two parts, (a) capacitance due to screening effects of outer walls of adjacent channels ($C_{sub,o}$) and (b) screening effects of the inner wall ($C_{sub,I}$) [11].

$$C_{sub,o} = \frac{1}{\frac{1}{C_{sub,oo}} + \frac{1}{C_{sub,oI}}} \tag{2}$$

where $C_{sub,oo}$ is the capacitance of the outer wall due to the outer wall of neighbouring channels.

$C_{sub,oI}$ is the capacitance of the outer wall due to inner wall of the channel.

$$C_{sub,oo} = \frac{2\pi k_2 \varepsilon_0}{\cosh^{-1}\left(\frac{2H_{sub}}{d_o}\right)} \tag{3}$$

$$C_{sub,oI} = \left(\frac{Q_{wall,o}}{Q_{wall,I}}\right) C_{sub,oo} \tag{4}$$

Similarly, $C_{sub,I}$ can be categorized and calculated by the following expressions

$$C_{sub,I} = \frac{1}{\frac{1}{C_{sub,Io}} + \frac{1}{C_{sub,II}}} \tag{5}$$

$$C_{sub,Io} = \left(\frac{Q_{wall,I}}{Q_{wall,o}}\right) C_{sub,o} \tag{6}$$

$$C_{sub,II} \approx C_{oI,cox} \tag{7}$$

3.4 Quantum capacitance

For large gate bias (Em, 0 $\ll \Delta\Phi_B$), the surface potential is limited by quantum capacitance, whereas for small gate bias (Em, 0 $<< \Delta\Phi_B$), channel acts as a linear voltage divider with less reliance on quantum capacitance [8]. With larger gate bias, the equations (14) and (15) from [8,9,11] relates quantum capacitance with surface potential. The factor of 4 indicates spin and double degeneracies of the sub band.

$$C_{qs}^{(i)} = \frac{dQ_{wall,s}^{(i)}}{d\frac{\Delta\Phi_B^{(i)}}{-e}} = 4\frac{e^2}{L_x kT} \times \left[\sum_{\substack{k_m^{(i)} \\ m=1}}^{M} \sum_{\substack{k_l^{(i)} \\ l=0}}^{L} \frac{e^{\frac{\left(E_{m,0}^{(i)} - \Delta\Phi^{(i)}\right)}{kT}}}{\left(1 + e^{\frac{\left(E_{m,0}^{(i)} - \Delta\Phi_B^{(i)}\right)}{kT}}\right)^2}\right] \tag{8}$$

$$C_{qD}^{(i)} = \frac{dQ_{wall,D}^{(i)}}{d\frac{\Delta\Phi_B^{(i)}}{-e}} = 4\frac{e^2}{L_x kT} \times \left[\sum_{\substack{k_m^{(i)} \\ m=1}}^{M} \sum_{\substack{k_l^{(i)} \\ l=0}}^{L} \frac{e^{\frac{\left(E_{m,0}^{(i)} - \Delta\Phi^{(i)} + eV_{ch,DS}^{(i)}\right)}{kT}}}{\left(1 + e^{\frac{\left(E_{m,0}^{(i)} - \Delta\Phi_B^{(i)} + eV_{ch,DS}^{(i)}\right)}{kT}}\right)^2}\right] \tag{9}$$

where,

$$E_{m,0}^{(i)} = \frac{\sqrt{3}}{2} a V_\pi k_m \quad (10)$$

3.5 Coupling capacitance

The electrostatic capacitance between outer and inner wall of the channel due to coupling (*CoI*) is the same as that of $C_{sub,II} \approx C_{oI,cox}$.

$$C_{oI} = C_{sub,II} \approx C_{oI,cox} \quad (11)$$

3.6 Current

The currents through the outer and inner wall are calculated with the following Eqs. [8] and [11].

$$I_{semi}^{(i)}\left(V_{ds}^{(i)}, V_{gs}^{(i)}\right) = 2 \sum_{\substack{k_m^{(i)} \\ m=1}}^{M} \sum_{\substack{k_l^{(i)} \\ l=0}}^{L} \left[T_{LR}^{(i)} J_{m,l}^{(i)} \left(0, \Delta\Phi_B^{(i)}\right)|_{+k} - T_{RL}^{(i)} J_{m,l}^{(i)} \left(0, \Delta\Phi_B^{(i)}\right)|_{-k} \right] \quad (12)$$

The inter wall tunnelling current is ignored [7,11]. Here, m, l are the number of sub bands and substates. T_{LR} is the transmission probability of the carriers at the substate (m, l) in $+k$ branch, similarly, T_{RL} is in $-k$ branch due to scattering effect of acoustic phonon and optical phonon at the channel region. It is assumed that the transmission probability to be unity for ballistic transport. Vds and Vgs are the corresponding voltage across drain-source and gate-source at the channel end. The wave numbers $k_m^{(i)}$ and $k_l^{(i)}$ are along the circumferential and axial directions. $\Delta\Phi_B^{(i)}$ is the surface potential of channel, the superscript 'i'' stands for outer and inner wall. The relation for k_l is taken from [13]. Double degeneracy is reflected by the factor of 2 in the equation.

$$k_l = 2\pi l / L_x,\ l = 0, 1, 2 \text{ and } L_x \approx L_g + L_s + L_d \quad (13)$$

where i = o, I.

To calculate the surface potential $\Delta\Phi_B$, Eqs. (14)–(19) [10,13] are solved iteratively.

$$Q_{cap,o} = C_{gc,o}(V_G - V_{FB}) + C_{sub,o} V_{sub} + C_{c,o}\beta_o V_{ds,o} + C_{c,o}(1 - \beta_o) V_{gs,o} - \left(C_{gc,o} + C_{sub,o} + C_{c,o}\right) \frac{\Delta\Phi_{B,o}}{e} \quad (14)$$

$$Q_{cap,I} = C_{gc,I}(V_G - V_{FB}) + C_{sub,I} V_{sub} + C_{c,I}\beta_I V_{ch,D,I} + C_{c,o}(1 - \beta_I) V_{ch,S,o} - \left(C_{gc,I} + C_{sub,I} + C_{c,I}\right) \frac{\Delta\Phi_{B,I}}{e} \quad (15)$$

$$Q_{wall,s}^{(i)} = 4\frac{e}{L_x} \sum_{\substack{k_m^{(i)} \\ m=1}}^{M} \sum_{\substack{k_l^{(i)} \\ l=0}}^{L} \left[\left(\frac{1}{1 + e^{\frac{\left(E_{m,0}^{(i)} - \Delta\Phi_B^{(i)}\right)}{kT}}} \right) \right] \quad (16)$$

$$Q_{wall,d}^{(i)} = 4\frac{e}{L_x} \sum_{\substack{k_m^{(i)} \\ m=1}}^{M} \sum_{\substack{k_l^{(i)} \\ l=0}}^{L} \left[\left(\frac{1}{1 + e^{\frac{\left(E_{m,0}^{(i)} - \Delta\Phi_B^{(i)} + eV_{ch,DS}^{(i)}\right)}{kT}}} \right) \right] \quad (17)$$

$$Q_{wall}^{(i)} = Q_{wall,s}^{(i)} + Q_{wall,d}^{(i)} \quad (18)$$

$$Q_{cap,o/I} = Q_{wall}^{(i)} \quad (19)$$

where k Boltzmann constant, T Kelvin temperature, Cc, $o(Cc, I)$ coupling capacitance of the outer (inner) wall due to surface potential, $Q_{cap,o/I}$ charge induced on the electrodes per unit length and $Q_{wall}^{(i)}$ charge induced on both the outer and inner walls.

The surface potential responds to the drain voltage which is explained by the fitting parameter β Cc ($\beta = 0.8$, $Cc = Cgc/15$) [11]. It is due to lowering of the surface-potential by (1) electrostatic coupling between CNT and drain electrode through fringing field and (2) drain induced barrier lowering (DIBL) which remains as the base for non-uniform surface-potential profile. V_{FB} is the flat band voltage and is assumed to be zero [11], Vsub is the potential difference between source and substrate.

3.7 Signal delay and cut off frequency

The total signal delay time 'τ' is inversely proportional to the cut off frequency f_t. The signal delay τ is found from the following equations.

$$\tau_{total} = \frac{1}{2\pi f_t} \quad (20)$$

where,

$$f_T = \frac{g_m}{2\pi C} \quad (21)$$

$$g_m = \frac{\partial I}{\partial V_G}\Big| V_G = V_D. \quad (22)$$

The driven capacitance and drive current are calculated with following relations [8,10,11].

$$I = \min(N, 2) . \left(I_e^{(o)} + I_e^I\right) + \max(N - 2, 0) . \left(I_m^{(o)} + I_m^I\right) \quad (23)$$

Driven capacitance

$$C = C_g L_g + f_{miller}.2\left(C_{of}^{(g)} L_s + C_{gs} W_{pitch}\right) + C_{gsub} \quad (24)$$

where,

$$C_g = \min(N, 2) \cdot \left(C^{(o)}_{g,e} + C^{I}_{g,e}\right) + \max(N-2, 0) \cdot \left(C^{(o)}_{g,m} + C^{I}_{g,m}\right) \quad (25)$$

$$C^{(i)}_g = \frac{\partial Q^{(i)}_{wall}}{\partial V_G} \quad (26)$$

$$C^{(g)}_{of} = \min(N, 2) \cdot \left(C^{(o)}_{of,e}\right) + \max(N-2, 0) \cdot \left(C^{(o)}_{of,m}\right) \quad (27)$$

4 Results and discussions

Capacitance equations for planar double-walled CNTFET is derived in [11] and capacitances for gate wrap around CNTFET is derived in [14]. Referring the equations from [11,12] and [14] gate capacitances, parasitic capacitances, substrate capacitance, coupling capacitance and quantum capacitances are derived. Surface potential for individual walls are calculated by solving equations from (14) through (19).The corresponding currents are calculated by solving Eq. (12). Drive currents for both double and single-walled with and without screening effects are calculated, plotted and compared. Response of drain current is studied with respect to drain voltage, gate voltage, number of channels and tube diameters. Driven capacitance ratio is plotted for various values of gate dielectric and gate length. Using (20) through (22) cut off frequency and time delay are calculated, the ratio between DWGWA and SWGWA is plotted for source/drain length, channel density and tube diameters. Gate wrap around device structure provides good channel control, double wall enhances the current flow, array of channels handles larger capacitance loads and drive larger current. DWGWA shows the improved response compared to SWGWA with the same working temperature, drain and gate voltage. All the devices parameters are listed in the following Table 1 [11].

The output drain current is plotted against output drain voltage for various gate voltage. Figure 3 shows increasing drain current with increasing drain voltage and gate voltage. The drive current starts at Vds = 0.1 V itself and reaches maximum. After that it maintains almost constant variation. Drive current for DWGWA ranges around 36 μA for 1 V Vgs to 20 μA for 0.1 V Vgs. Increasing the number of channels per gate, increases the drain current profile. More number of channels (Channel density) has two effects.

(i) Each individual channels contribute for increasing the driven capacitance and drive current.
(ii) In contrast, it leads to more screening and imaging effects in turn increasing parasitic capacitance. This will reduce the drive capacitance and degrades drive current.

Table 1 Details of the device parameters and values

S. no.	Device parameters	Symbol	Values
1	Pitch distance	s	20 nm
2	Gate distance from the channel	h	5 nm
3	Gate length	Lg	16 nm
4	Source/drain length	Lsd	32 nm
5	Outer wall chirality	n11, n12	(26 ,0)
6	Inner wall chirality	n21, n22	(17 ,0)
7	Outer wall diameter	do	2 nm
8	Inner wall diameter	dI	1.34 nm
9	Number of channels	N	3
10	Gate dielectric	k1	16
11	Bulk dielectric	k2	4
12	Gate height	Hg	12 nm
13	Bulk dielectric thickness	Hsub	10 μ m
14	Oxide thickness	Tox	4 nm
15	Device pitch in the width direction	Wpitch	48 nm
16	Lattice constant	a	2.49 Å
17	Temperature	T	300 K
18	Flat band voltage	F_B	0 V

There needs a trade-off in designing such devices with array of channels. In this case, besides the second effect, first effect enhances the drive current compensating the parasitic effect of channel density (Fig. 4).

This is the graph between drain current and gate source voltage. The drain current is checked for Vds = 0.1 V, 0.6 V, 1 V and found that it is around 35 μA utmost for N = 3 and nears 100 μA with N = 9. Increasing the number of channels, increases the current flow. It has almost same value with various values of drain voltage. It is evident that the transverse current values of the proposed device DWGWA (35 μA) approximates to planar DWCNTFET [11] (40 μA). The graph shows a linear relation between drain current and gate voltage which is a proof of good channel control. Though the screening effect of inner wall reduces the outer wall current, the channel density supports for the total current.

The number of channels is one of the key parameter to be addressed, variation of which effects the flow of current. Drain current response of both double-walled and single-walled gate wrap around CNTFET for different channel densities is shown in Fig. 5. I1 through I10 corresponds to Vgs & Vds 0.1 V through 1.0 V. It is apparent that the DWGWA makes more current flow compared with its counterpart. DWGWA gives 273.6 μA current for Vgs =1.0 V and N = 21 whereas it is 117.3 μA in the case of SWGWA for same Vgs and N. The improvement of drive current is because of more driven capacitance in DWGWA. The channel density

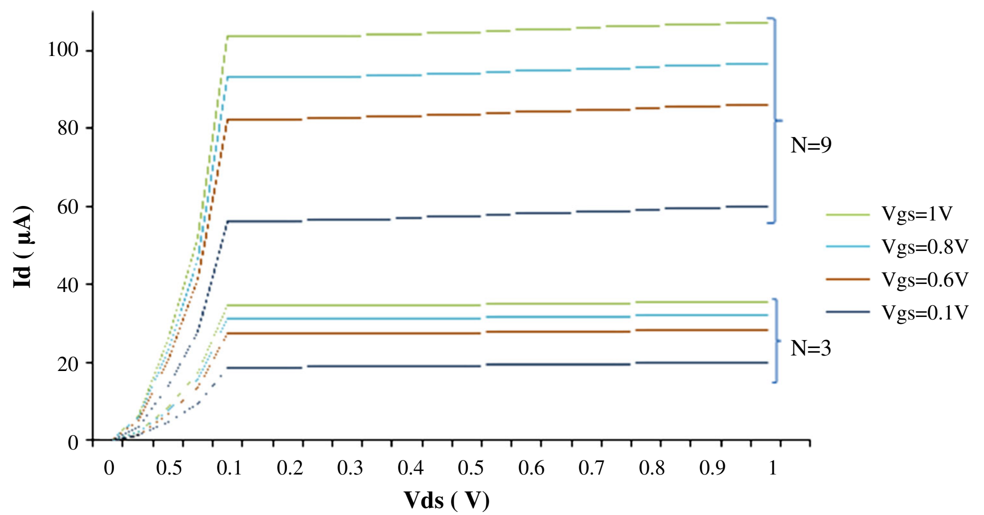


Fig. 3 The variation of drain current with respect to drain voltage for N = 3, 9

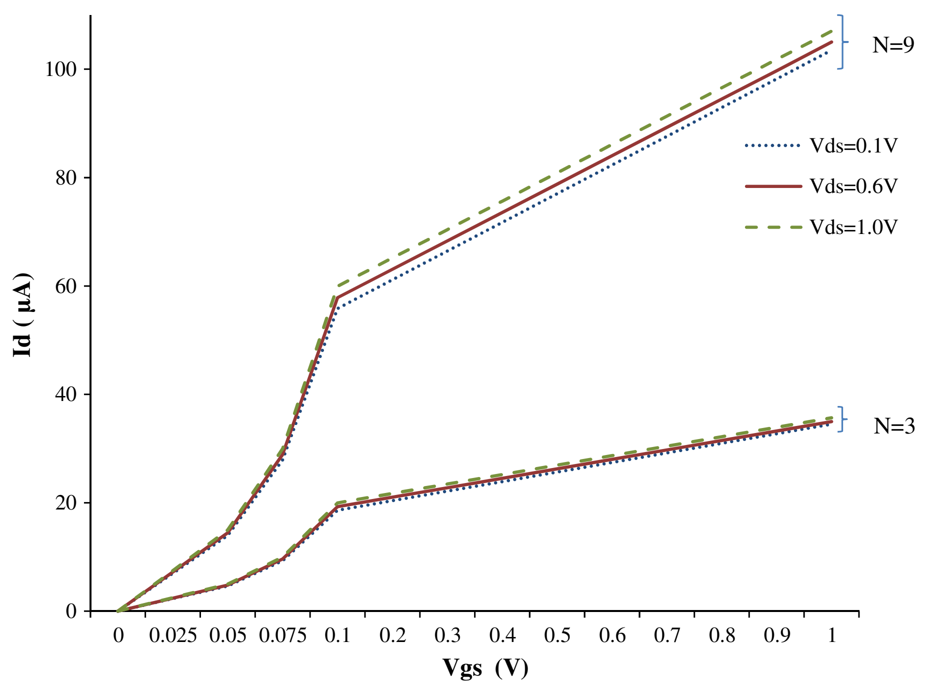


Fig. 4 The variation of drain current with respect to gate voltage for N = 3 and 9

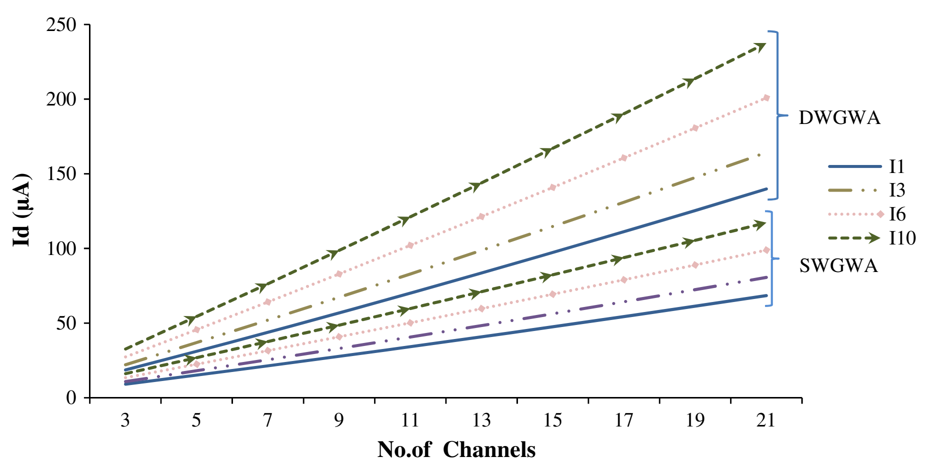


Fig. 5 Variation of DWGWA and SWGWA drain current with respect to channel density

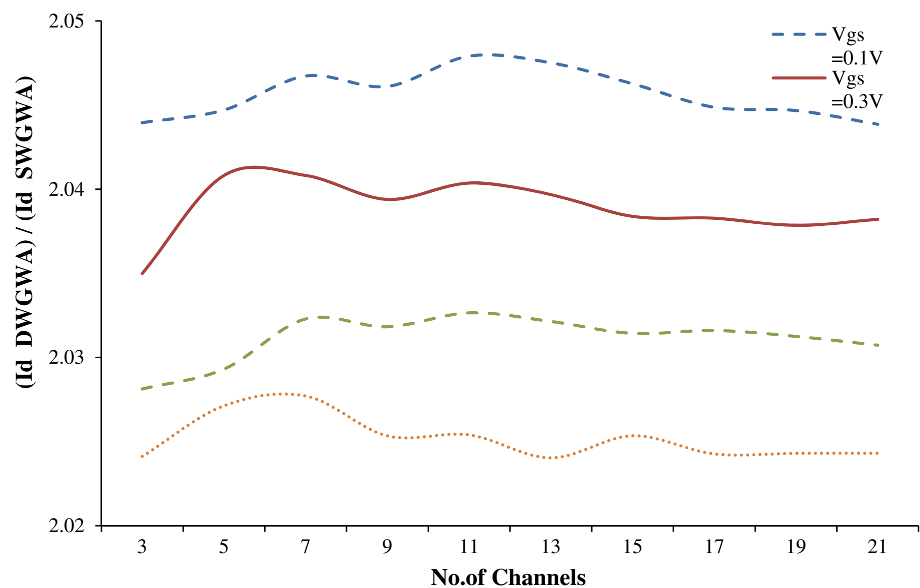


Fig. 6 Variation of the drive current ratio for various channel density and gate voltage

supports for increase in drive current flow. So, more the number of channels and more the Vgs value, more is the current flow in the channels.

(1) Co-axial device makes the capacitance to increase using the relation

$$C = \frac{2\pi \varepsilon L}{\ln\left(\frac{r_o}{r_I}\right)}$$

where L is the length of the tube; r_o is the outer tube diameter; r_I is the inner tube diameter.
Here, the value of the ratio $\ln\left(\frac{r_o}{r_I}\right)$ is 0.4, reciprocal of which is 2.5. More the capacitance, more drive current.

(2) The contribution of the inner wall may be small but array of parallel channels contribute more in cumulative.

So, the device containing double-wall channel has improved performance over single-wall channelled device.

Comparison of drive current for the proposed device, DWGWA with that of the SWGWA is studied to project the improved difference. It is done for varying channel densities to show the device significance towards its merit of applications. The current ratio between DWGWA and SWGWA for number of channels is illustrated in Fig. 6. This ratio is derived from Fig. 5 for studying the improvement of DWGWA over SWGWA. It is seen that with increase in number of channels the current ratio shows almost constant difference. The curve shows lesser value for more Vgs. That is, the ratio is almost constant, since the curves in Fig. 5 are linear and the ratio decreases with increase in Vgs. More the gate voltage, lesser the ratio value but almost constant for varied number of channels. In spite of the imaging and screening effects, the device shows enhanced performance. The ratio is not due to two paths but both contribute individually to have more throughput. It may vary for three and more walled CNTs. Figure 12 shows the behaviour of both devices for Cgc with respect to k1.

The drive current ratio for various diameters (chiralities) of the channel is an important study, as it gives idea about selecting the channel specifications for device design. Figure 7a shows the variation of drive current ratio and drain voltage for diameters d = 1.6 nm, 2.0 nm, 2.4 nm, 2.8 nm (chiralities= [(35,0), (19,0)], [(26,0), (17,0)], [(31,0), (16,0)], [(35,0), (22,0)]). The ratio is almost constant and in order to see the variations closely the graphs are plotted separately and made as insets. Figure 7a shows the variation for diameters 2.4 and 2.8 nm. The drive current of DWGWA maintains 1.7 and 2.26 times the drive current value of SWGWA. For d = 2.4 nm, the variation decreases at the starting point but with a linear increment till Vds = 0.6 V after which again there is a fall. In the next case, d = 2.8 nm the variation starts above 1.7 and oscillates around the same point and falls after Vgs = 0.6 V. This variation is very small but for nano scale device these variations also has to be considered.

Figure 7b shows the variation of drive current ratio and drain voltage for diameters d = 1.6 nm, 2.0 nm, 2.4 nm, 2.8 nm similar to Fig. 7a. This graph shows the variation for diameters 1.6 and 2.0 nm as insets. The graph for d = 1.6 nm resembles the curve for d = 2.8 nm. It is because of the similar chiralities of the outer wall of both the channels (35,0). But in overall appearance, it can be concluded that the

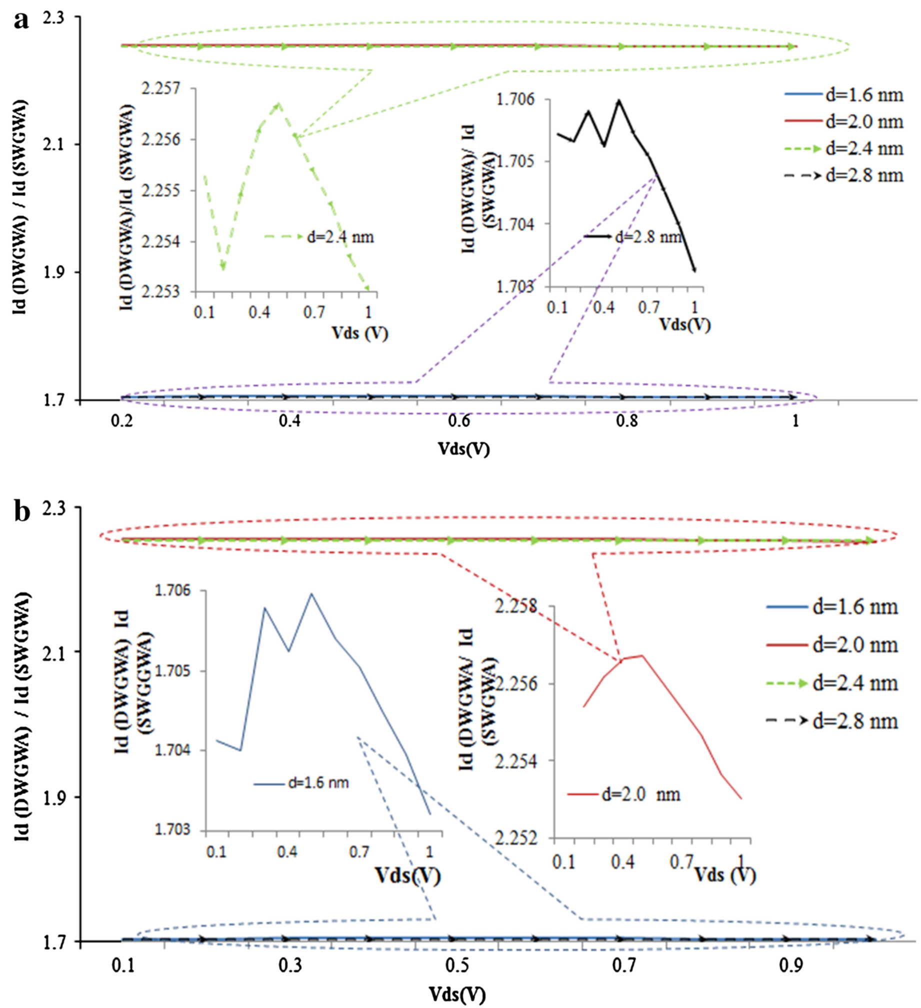


Fig. 7 **a** The change of current ratio with respect to drain voltage for d = 2.4 nm, d = 2.8 nm. **b** The change of current ratio with respect to drain voltage for d = 1.6 nm, d = 2.0 nm

variations are 1.7 and 2.26. For Vgs $>$ 0.6 V, all the curves shows a roll off even the variation is negligibly small. As the device design is in Nano scale, the above variation has to be followed closely. Otherwise the curves are very similar and coincidental.

The driven capacitance ratio is checked for verifying the role of gate dielectric value. Also, the behaviour of the capacitance ratio for various channel densities and tube diameters has to be added to know the electrostatic performance of the proposed device. Figure 8 is the graph between the driven capacitance ratio of DWGWA and SWGWA, with respect to dielectric values for different diameters and channel densities. The value of the driven capacitance increases when the channel density increases and the increment is greater in case of double-walled gate wrap around transistor than that of single-walled gate wrap around transistor. It gives, 1.55, 1.6, 1.7 increment before maintaining a constant ratio for d = 1.6, 2.0, 2.8 respectively, for k1 $\geq$ 16 and N $\geq$ 12. For lesser N, the increment approximates the same value but for k1 $\geq$ 30. Conclusion is, high-k ielectric value increases the capacitance ratio but limitation of the dielectric value of the gate oxide is greater than or equal to 16 after which it has the similar effect.

Gate or channel length is the transient distance for the current to travel from source side to drain side. Although the transport is ballistic, the study of electrostatic variation with gate length for various tube diameters and channel density becomes specific. Figure 9 shows the drive capacitance ratio with respect to the gate length for different values of diameters and channel densities. The constant variation shows that the behaviour of capacitance curve for both single and double-walled device is similar but the values of DWGWA is greater than SWGWA. The improvement graph show a constant behaviour and the ratio are reduces with reducing density of channels. The values of DWSWA are around 1.5, 1.55, 1.6 times for diameters 1.6, 2.8 and 2.0 nm respectively. The reason that d = 2.8 nm lies in between the other two is its outer wall chirality is same as that of d = 1.6 nm (35,0). This complexity shuffles the graph. Otherwise, the ratio will increase with larger diameter. As a justification, examples for actual quantities are shown in Appendix 2.

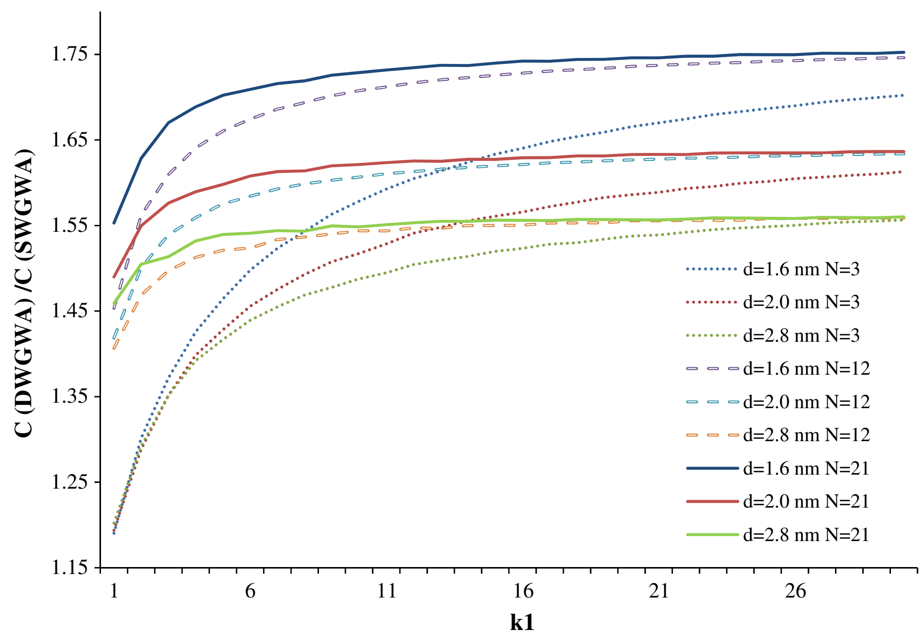


Fig. 8 Variation of drive capacitance ratio with respect to k1 for various diameters and channel density

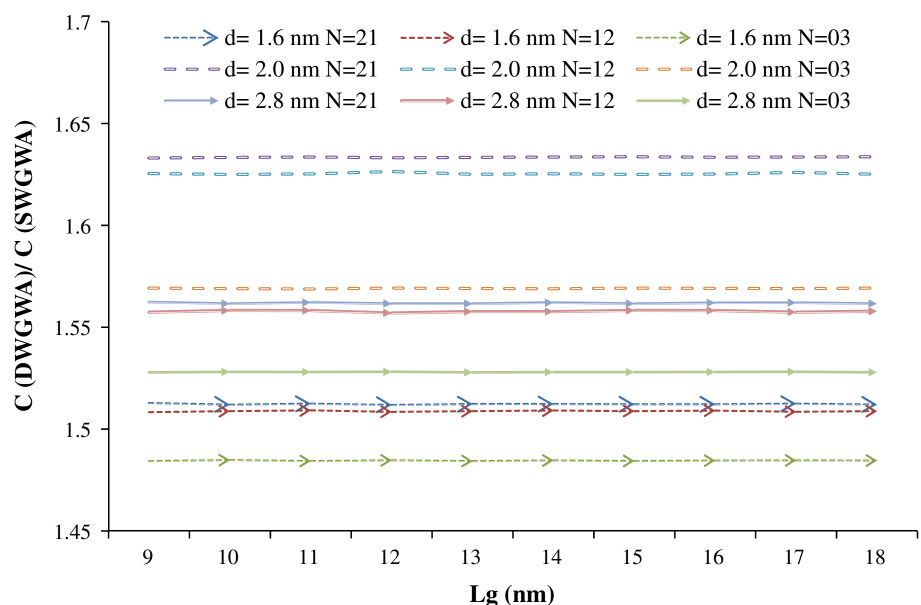


Fig. 9 Variation of drive capacitance ratio with respect to gate length for various diameters and channel density

Since the transport through the channel is ballistic instead of diffusive and the comparison of capacitance ratio is done, the behaviour of the cut off frequency for variation in source/drain length is studied. The ratio of f_T is plotted in Fig. 10 for d = 1.6[(35,0), (19,0)], 2.0[(26,0), (17,0)], 2.4[(31,0), (16,0)], 2.8[(35,0), (22,0)]. The curves shows a complex performance because of the typical signal band structure of CNTs and chirallities of individual walls. It shows improved values from 0.9 to 1.5 for N = 9 and around 0.2 for N = 21. Cut off frequency is more N = 9 and it is 1.4 times greater for d = 2.4 nm, around 1.1 times that of SWGWA for d = 2.0 nm .For N = 21, the ratio shows very poor performance of DWGWA than SWGWA. This is because of the screening effects with larger number of tubes. So, the selection of channel density restricts for the number of channels about 21.

Signal delay is the inverse of cut off frequency and its variation towards the change in tube diameters along with the number of channels has to be projected. Figure 11 depicts the delay ratio of DWGWA over SWGWA for various values of source/drain length and number of channels. The ratio is plotted in Fig. 11 for d = 1.6[(35,0), (19,0)], 2.0[(26,0), (17,0)], 2.4[(31,0), (16,0)], 2.8[(35,0), (22,0)] similar to that of f_T. The delay ratio "τ" increases with larger number of channels and increasing diameters. The d = 1.6 nm curve is in between d = 2.8 nm and d = 2.4 nm because of the chirality

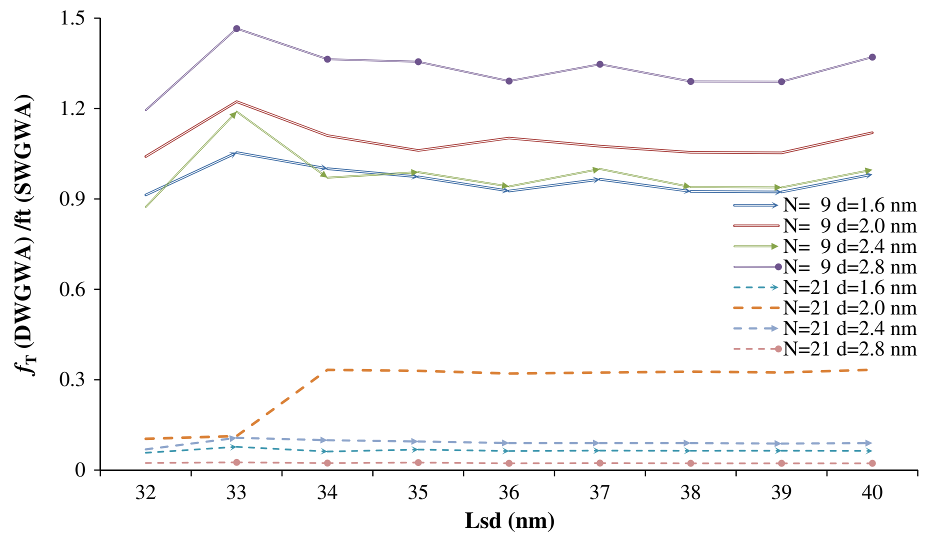


Fig. 10 The variation of cut off frequency ratio with respect to Lsd, diameters and number of channels

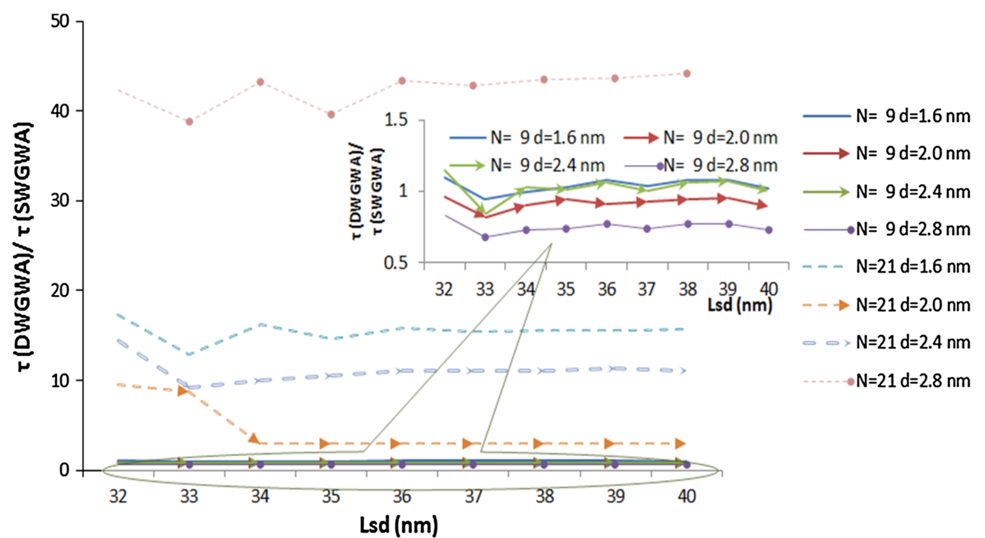


Fig. 11 The variation of delay time ratio with respect to Lsd, diameters and number of channels

chosen. The variation of delay ratio for N = 9 is projected as inset and the values are around 1.0 for all the diameters chosen. So, larger the diameter of the tube and more the density of channels, better the delay of DWGWA compared to its counterpart. It is due to ballistic transport and high drive current.

5 Conclusions

A compact model of intrinsic channel region of MOSFET-like DWGWA is presented in this research paper. This model supports for linear (summation) approximation instead for non-linear (integral) approach so as to apply easily for other types of 1-D devices with less computational work and suits well for a wide range of channel diameters, therefore the chiralities. Drain current profile increases with density of the channels in the array. Delay ratio decreases for smaller diameters and lesser channel density. With lesser density of channels and for smaller diameter the delay ratio of DWGWA is more than SWGWA. More cut off frequency ratio is found for N = 9 and d = 2.8 nm, d = 2.0 nm. In core, DWGWA (a) contributes more ON-current with denser array of channels because of ballistic transport and higher drive capacitance-this property can be used while designing high power handling 1-D Nano devices, (b) more delay ratio for higher density of channels-this property can be used to construct high speed device. So, in core this model can be considered while designing such device structures. Cut off frequency for the chirality (26,0), (17,0) is greater (1.1 times) for N = 9 and lesser for N = 3, 21. It is again checked for N = 9, N = 21 for other diameters. It can be concluded that $3 \leq N \leq 12$ may suit well as the number of CNTs in the array. Number of channels can be nine or twelve may be a better choice. This

model can be utilized for future high performance device. The transition of the current behaviour is sharper, the boost of current for DWGWA is double compared to SWGWA are complicated and needs more detailed work for future.

Appendix 1

The equations for the following three capacitances considered in [14] for gate wrap around is taken for discussion in our paper.

(a) Gate to channel Capacitance (*Cgc*)
(b) Fringe Capacitance and (*Cof*)
(c) Gate to gate capacitance (or) gate to source/drain capacitance (*Cgtg*)

(a) Gate to channel capacitance (*Cgc*)

There are two calculations for Gate to channel capacitance (*Cgc*), since both individual walls of the channel are to be taken separately. One is the capacitance due to gate and outer wall of the channel (*Cgc,o*) and the other is due to capacitance between gate and inner wall of the channel (Cgc, I).
Cgc,o is further divided into

(a) Gate channel capacitance of the outer wall and the screening effects of other DWCNTs ($Cgc, o^{(o)(o)}$) and
(b) Gate channel capacitance due to imaging effects of the inter walls of the same channel ($Cgc, o^{(o)(I)}$).

They are related by the following equations as in [10] and [11].

$$Cgc, o = \frac{1}{\frac{1}{Cgc,o^{(o)(o)}} + \frac{1}{Cgc,o^{(o)(I)}}} \tag{28}$$

The reason behind to take Eq. (1) from [11] is that double wall is considered in this paper and the equations are similar for planar [11] and gate wrap around [14].

Again, $Cgc^{(o)(o)}$ can be divided for capacitance of the channels at

(i) end of the array ($Cgc, e^{(o)(o)}$) caused by the neighbouring channel at one side alone and
(ii) middle of the array ($Cgc, m^{(o)(o)}$) caused by the neighbouring channel at both the sides.

They are calculated using the relations from [10,11] and [14]

$$Cgc, o^{(o)(o)} = \begin{cases} Cgc, e^{(o)(o)} = \frac{Cgc,inf.Cgc,sr}{Cgc,inf+Cgc,sr} \\ Cgc, m^{(o)(o)} = 2.Cgc, e^{(o)(o)} - Cgc, inf \end{cases} \tag{29}$$

where *Cgc,inf* is the gate channel (outer wall) capacitance without any screening effects, *Cgc,sr* the equivalent capacitance including the screening effects of the other channels in the array.

Cgc,inf is calculated for cylindrical Gate Wrap Around CNTFET, the ratio $\frac{1}{3}$ in second term of denominator of Eq. (3) is for cylindrical gate wrap around as in [14].

$$Cgc, inf = \frac{2\pi\kappa_1\varepsilon_0}{\cosh^{-1}\left(\frac{2h}{d_o}\right) + \frac{1}{3}\lambda_1 \ln\left(\frac{2h+2d_o}{3d_o}\right)} \tag{30}$$

Cgc,sr is calculated by taking the potential drop

(i) between gate and outer wall of the same channel and
(ii) due to the screening effects of the double walls of the neighbouring DWCNTs [10] and [11].

$$Cgc, sr = \frac{1}{\frac{1}{Cgc,sr^{(o)(o)}} + \frac{1}{Cgc,sr^{(o)(I)}}} \tag{31}$$

where,

$$Cgc, sr^{(o)(o)} = \frac{4\pi\kappa_1\varepsilon_0}{\ln\left(\frac{s^2+2(h-r_o).\left[h+\sqrt{h^2-r_o^2}\right]}{s^2+2(h-r_o).\left[h-\sqrt{h^2-r_o^2}\right]}\right) + \ln\left(\frac{s^2+2(h-r_o).\left[h+\sqrt{h^2-r_o^2}\right]}{s^2+2(h-r_o).\left[h-\sqrt{h^2-r_o^2}\right]}\right) + \lambda_1 \ln\left(\frac{(h+d_o)^2+s^2}{9r_o^2+s^2}\right).tanh\left(\frac{h+r_o}{s-d_o}\right)} \tag{32}$$

Equation (5) is taken from [14] (gate wrap around transistor). The term highlighted in blue is for gate wrap around transistors.
Here,

$$Cgc, sr^{(o)(I)} = \frac{Q_A^{(o)}}{Q_A^{(I)}} Cgc, sr^{(o)(o)} \tag{33}$$

$$Cgc, o^{(o)(I)} = \frac{Q_A^{(o)}}{Q_A^{(I)}} Cgc, inf \tag{34}$$

Equation (6) and (7) are derived with (5) [14] with the format of device containing the channel as double wall [11].

To find out Gate and inner wall of the channel *(Cgc,I)* [10], comprising

(i) The effects of inhomogeneous gate dielectric and the imaging effects of other neighbouring GWADWCNTs $Cgc, I^{(I)(o)}$.
(ii) The imaging effects of the outer wall $Cgc, I^{(I)(I)}$,

$$Cgc, I = \frac{1}{\frac{1}{Cgc,o^{(I)(o)}} + \frac{1}{Cgc,o^{(I)(I)}}} \tag{35}$$

$$Cgc, I^{(I)(o)} = \frac{Q_A^{(I)(o)}}{Q_A^{(o)}} Cgc, o \tag{36}$$

$$\mathrm{Cgc}, \mathrm{I}^{(\mathrm{I})(\mathrm{I})} = \frac{2\pi\varepsilon_0}{\ln\left(\frac{\mathrm{d_o}}{\mathrm{d_I}}\right)} \tag{37}$$

where do and are d_I diameters of the cylinder, a is Lattice Constant (2.49 Å).

Equations (8), (9) and (10) are for double wall channelled array device, so it is taken from [11] and the corresponding values of gate wrap around from (1) is substituted for Cgc, o. Next is about the fringing capacitance,

For wrap around gate FET equation (11) and (12) are taken from [14], the difference with respect to planar gate is highlighted in blue.

$$Cof, m = \frac{2\alpha}{\eta_1} Cof, e + \left(\frac{1-2\alpha}{\eta_1}\right) \cdot \left(\frac{\pi\kappa_2\varepsilon_0 Lsd}{1/3\,\cosh^{-1}\left(\frac{(4h^2)+(0.56Lsd)^2}{d_o}\right)}\right) \tag{38}$$

where,

$$\alpha = \exp\left(\frac{N-3}{\tau_2 N}\right), N \geq 3 \tag{39}$$

$$Cof, e = \frac{\pi\kappa_2\varepsilon_0 Lsd}{\ln\left(\frac{(4h^2)+(0.56Lsd)^2+s^2}{s}\right) + \ln\left(\frac{\sqrt{(s/2^2)}}{2}\right) + \exp\left(\frac{\sqrt{Na^2-2N}+N-2}{\tau_1 N}\right) \cdot \frac{1}{3}\cosh^{-1}\left(\frac{(4h^2)+(0.56Lsd)^2}{d_o}\right)}, N \geq 2 \tag{40}$$

τ_1 τ_2 are fitting parameters describing the rate of decrement in electric flux of the neighbouring cylinders with increase in distance between them. τ_1, τ_2 are taken as 2.5 and 2.0 respectively from [14]

The gate-to-gate (or) gate to source/drain capacitance *(Cgtg)* is taken from [14] for gate wrap around and number of walls is the independent factor for this capacitance. (The equation in [11] is taken from [10]).

$$C_{gtg} = \frac{3\kappa_2\varepsilon_0 H_{gate}}{Lsd} + \alpha_{gtg,sr}\frac{\pi\kappa_2\varepsilon_0}{\ln\left(\frac{2\pi(Lsd+L_g)}{2L_g+\tau_{bk}(H_{gate}+h+r_O)}\right)} \tag{41}$$

α_{gtg} is the factor due to screening effect of neighbouring conductors (Gate/ Source/ Drain)

$(\alpha_{gtg} = 0.7)$

where,

$$\tau_{bk} = \exp\left(\frac{(2-2\sqrt{1+2}(H_{gate}+L_g)}{Lsd}\right) \tag{42}$$

The drive capacitance is calculated [11] using the following relation,

$$C = C_g L_g + f_{miller}.2\left(C_{of}^{(g)} L_s + C_{gtg} W_{pitch}\right) + C_{gsub} \tag{43}$$

where,

$f_{miller} = 1.5.$

Thus, the equations for gate wrap around transistors is taken from [14], relations for double walled channel array is taken from [11], and new device gate wrap around double walled array CNTFET is developed.

Appendix 2

For the Fig. 6, the drive current values of both the walls are projected in Fig. 5.

For Fig. 7a, b sample graph is shown in Fig. 12. The graph is for d = 2.0 nm and N = 21.

For Fig. 8 sample graph for drive capacitance with respect to 'k1' is shown. The graph is for d = 2.0 nm (Fig. 13).

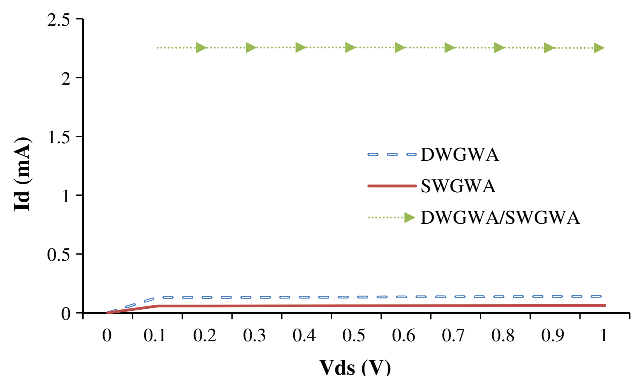


Fig. 12 Variation of drain current of DWGWA, SWGWA and their ratio with respect to drain voltage

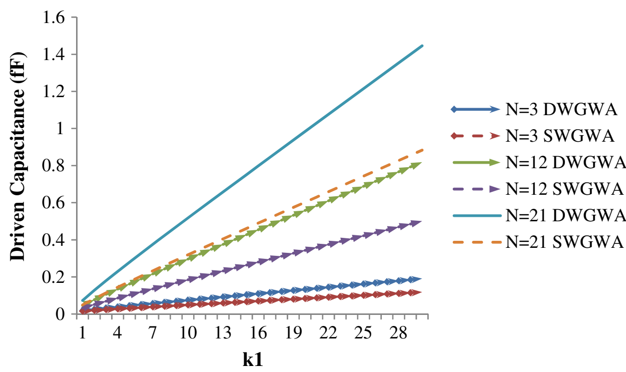


Fig. 13 Variation of driven capacitance with respect to k1 for DWGWA & SWGWA

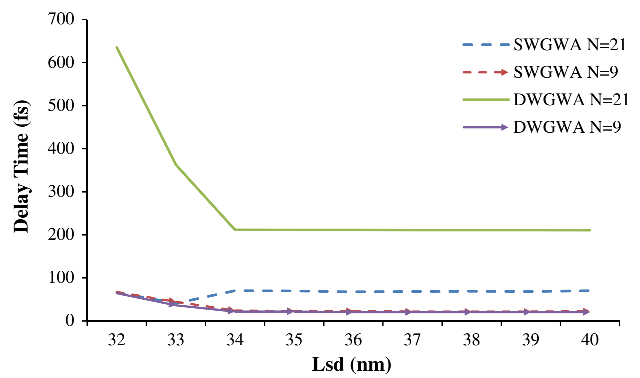


Fig. 16 Variation of delay time with respect to source/drain length of DWGWA, SWGWA

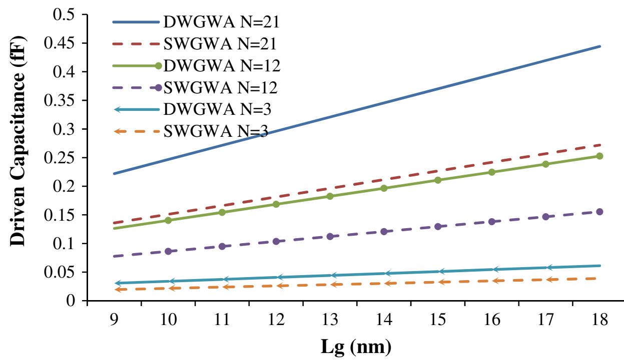


Fig. 14 Driven capacitance with respect to gate length is shown. The graph is for d = 2.0 nm

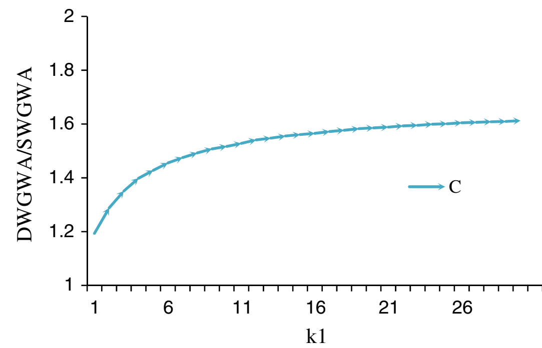


Fig. 17 Driven capacitance and its ratio between DWGWA and SWGWA for different gate dielectrics

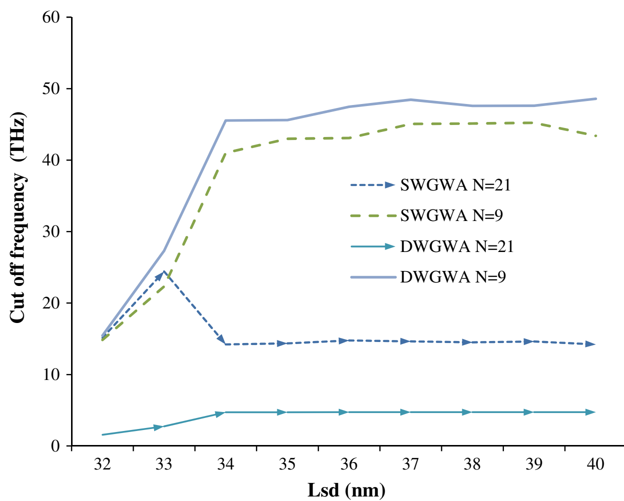
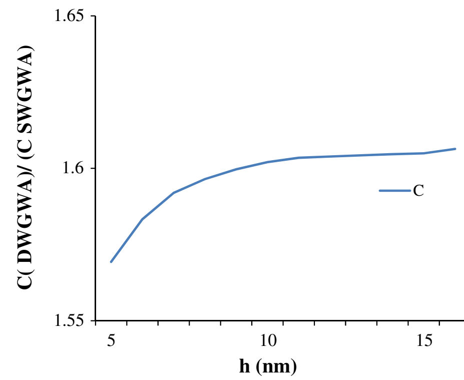


Fig. 15 Variation of cut-off frequency with respect to source/drain length of DWGWA, SWGWA



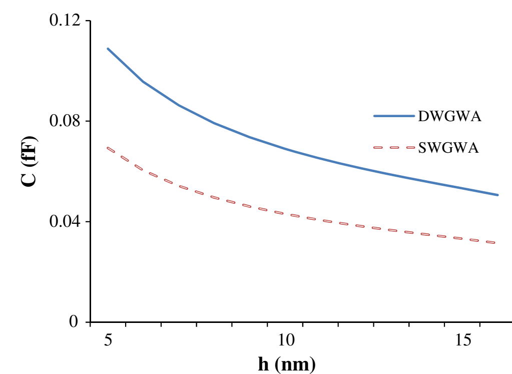


Fig. 18 Driven capacitance and its ratio between DWGWA and SWGWA for different 'h' distance

For Fig. 9 sample graph for drive capacitance with respect to gate length is shown. The graph is for d = 2.0 nm (Fig. 14).

For Fig. 10 sample graph for cut-off frequency is shown. The graph is for d = 2.0 nm (Fig. 15).

For Fig. 11 sample graph for delay time is shown. The graph is for d = 2.0 nm (Fig. 16).

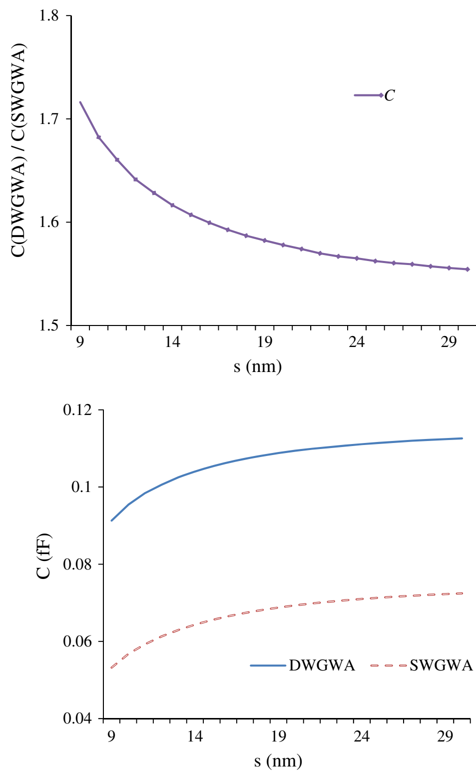


Fig. 19 Driven capacitance and its ratio between DWGWA and SWGWA for different ‘s’ distance

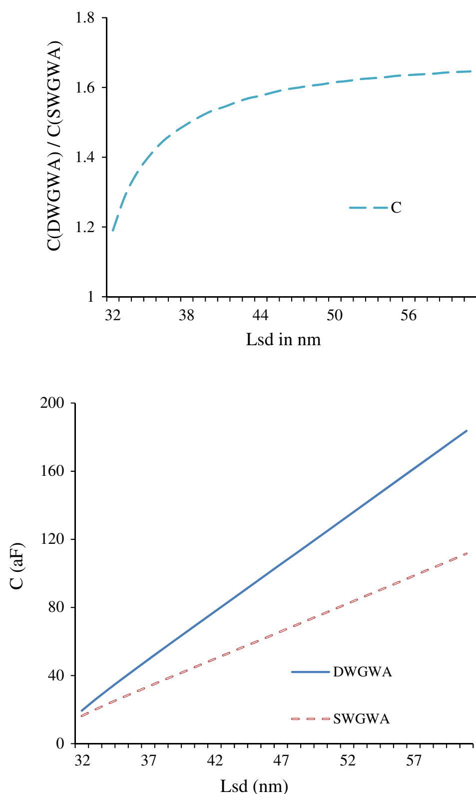


Fig. 20 Driven capacitance and its ratio between DWGWA and SWGWA for different ‘Lsd’ distance

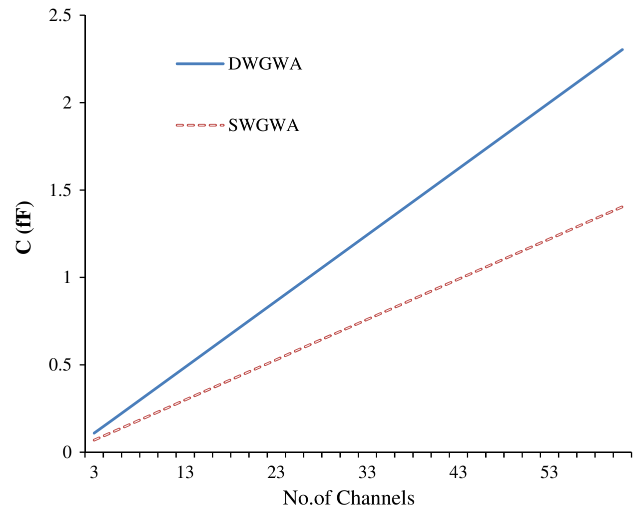


Fig. 21 Driven Capacitance and its ratio between DWGWA and SWGWA for various N

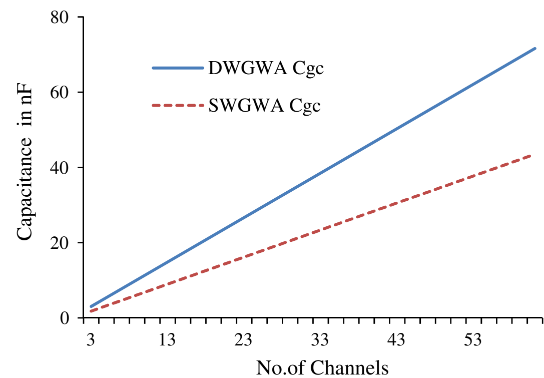


Fig. 22 Variation of Cgc of DWGWA and SWGWA with respect to number of channels

The behavior of both the devices for driven capacitance project the variations as shown in the figures from Fig. 17 to Fig. 22.

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