J Comput Electron (2008) 7: 346–349
DOI 10.1007/s10825-008-0224-4

Fully 3D self-consistent quantum transport simulation of Double-gate and Tri-gate 10 nm FinFETs

H. Khan · D. Mamaluy · D. Vasileska

Published online: 20 February 2008

Abstract We utilize a fully self-consistent 3D quantum mechanical simulator based on the Contact Block Reduction (CBR) method to investigate the effects of fin height and unintentional dopant on the device characteristics of a 10-nm FinFET device. The per-fin height off-current is found to be relatively insensitive to fin height while the corresponding per fin height on-current may significantly depend on fin height due to the stronger confinement with decreasing fin height. Also gate leakage is found to show similar behavior as device on-current with decreasing fin height. Tri-gate (TG) FinFET is found to show better performance compared to Double-gate (DG) FinFET, with the exception of gate leakage current. Simulation results show that an unintentional dopant within the channel can significantly alter device characteristics depending on its position and applied biases. In addition, the effects of unintentional dopant are found to be stronger at high drain bias than at low drain bias.

Keywords FinFETs · Unintentional dopant · Tri-gate FinFET · CBR

1 Introduction

Due to the aggressive scaling of semiconductor devices towards 22 node technology, a fully three dimensional (3D) simulation is becoming increasingly important for the accurate modeling of ultra scaled devices. Two dimensional (2D) simulations become less accurate once device dimensions become comparable to each other (such as fin width and fin height in ultra-scaled FinFETs). Investigation of the effects due to unintentional dopant, discrete doping and the presence of a top gate require a fully 3D simulation. In this work we utilize a fully 3D self-consistent quantum mechanical transport simulator based on the CBR method [1] within the effective mass approximation [2] to investigate electron transport properties of ultra-small DG and TG FinFET devices with comparable fin width and fin height. In addition, we analyze the impact of an unintentional dopant on the characteristics of the device. All the results presented here correspond to fully charge self-consistent quantum ballistic simulation, with electron–electron interaction taken into account using exchange-correlation terms in LDA [2]. No other scattering mechanisms are included. Figure 1 depicts the geometry of the 10-nm FinFET device being investigated in this study. Fin thickness, t_{Si} of 4 nm and gate oxide (SiO_2) thickness, t_{ox} of 12 Å have been used for all gates in the simulation.

Source, drain and gate doping of 2×10^{19} cm^{-3} with a lightly doped body and a doping gradient of 1.25 nm/decade across source/drain-body junctions have been adopted.

2 Effects of Fin height

We investigate the effects of fin height (h) on drain and gate current (due to electrons only). Figure 2 shows the drain current (normalized by the fin height h) for $h = 4$ nm and 8 nm along with 2D simulation result. 2D simulation assumes uniform distribution of electron along the fin height (very tall fin), and breaks up as fin height becomes comparable to fin width for narrow fin width FinFETs. For $h = 4$ nm, electrons in the channels are strongly confined along both Y

H. Khan (✉) · D. Mamaluy · D. Vasileska
Department of Electrical Engineering, Arizona State University, Tempe, AZ 85287, USA
e-mail: hrkhan@asu.edu

D. Mamaluy
e-mail: mamaluy@asu.edu

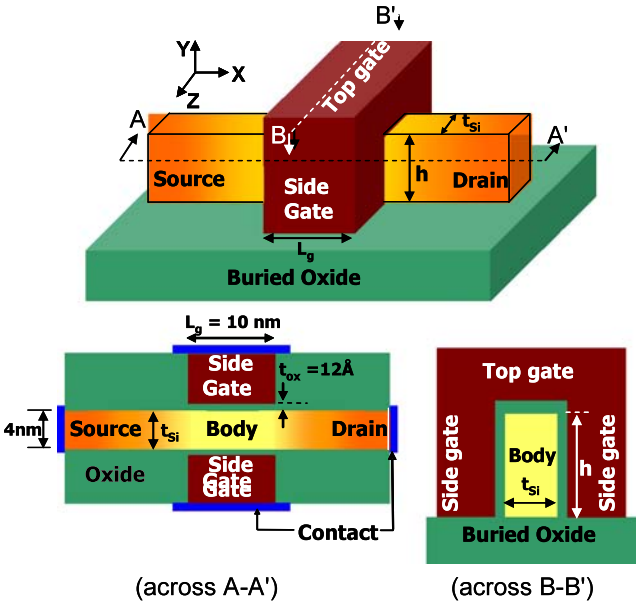

Fig. 1 *Top*: 3D schematic view, *bottom left*: top view along A–A′ cross section, and *bottom right*: side view along B–B′ cross section

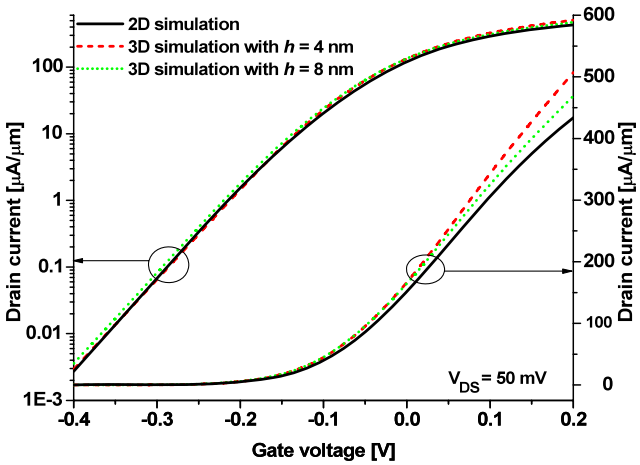

Fig. 2 Drain current (normalized by fin height h) vs. gate voltage as a function of fin height

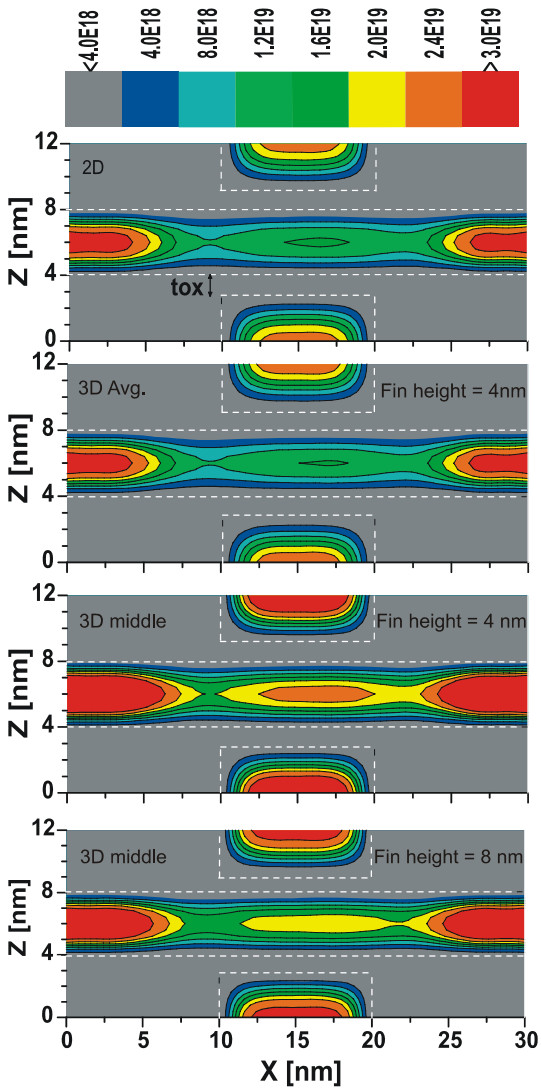

Fig. 3 2D electron density in XZ plane: from *top down* 2D simulation, average (over fin height) electron density with $h = 4$ nm, density at $y = h/2$ with $h = 4$ nm, density at $y = h/2$ with $h = 8$ nm. All evaluated at $V_{GS} = 0.2$ V and $V_{DS} = 50$ mV

and Z directions and electron density increases significantly around the center of the fin as can be seen from Fig. 3 (second from bottom). In this case, therefore, the drain current shows higher value compared to the 2D case at larger gate voltages. Note that the average (taken over $h = 4$ nm) electron density is slightly smaller than the 2D case, but the current is mainly contributed by electrons in the middle of the fin height region.

As h increases, confinement along h decreases and the distribution of electron approaches uniformity along the fin height. Figure 3 (bottom) shows the electron distribution at $y = h/2$ with $h = 8$ nm. One can see reduced electron density compared to the case with $h = 4$ nm (Fig. 3, second from bottom). Consequently for $h = 8$ nm we see smaller value of per fin height drain current (relative to $h = 4$ nm case) which approaches the 2D simulation values.

Gate leakage obtained using 2D and 3D simulators are shown in Fig. 4. Gate current shows similar trend as the drain current with fin height variation.

3 Double-gate vs. Tri-gate FinFET

The simulation results presented in the previous section assume that the top gate oxide thickness is much larger than side gate oxide thickness. We also analyze device behavior with the top gate oxide thickness being equal to the side gate oxide thickness. Transfer characteristics for DG and TG FinFETs at $V_{DS} = 0.4$ V are shown in Fig. 5.

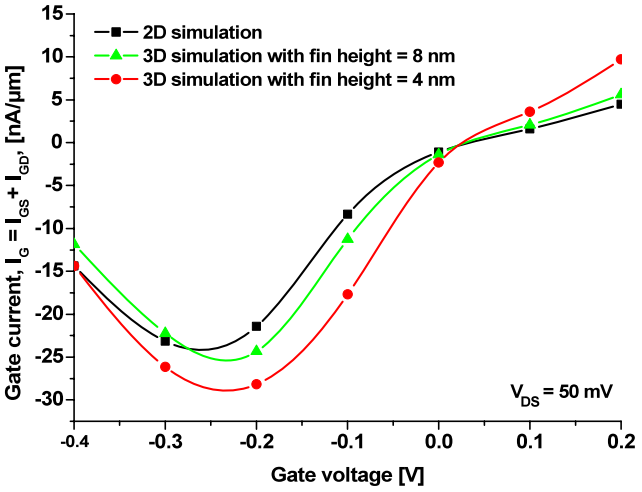

Fig. 4 Net gate current (normalized by fin height h) obtained using 2D and 3D simulators with fin height of 4 nm and 8 nm

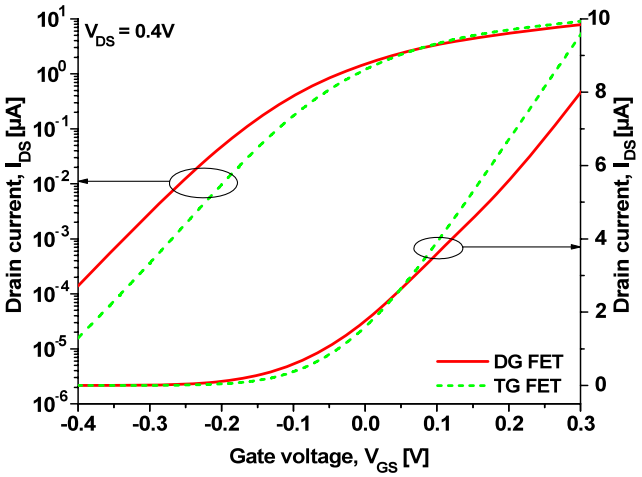

Fig. 5 Transfer characteristics of DG and TG FinFETs at a drain bias, $V_{DS} = 0.4$ V

Adding top gate increases the on-current and improves subthreshold swing. Also the value of off-current is significantly smaller than that for DG FinFET. Figure 6 shows the net gate leakage ($I_{GS} + I_{GD}$) as a function of gate voltage for DG and TG FinFETs. We note that the off-state ($V_{GS} = -0.4$ V) gate leakage is about 300% higher in TG case compared to DG value, which is not proportional to the increased gate area, but rather determined by the quantum-mechanical resonances.

The 3D electron density in on-state for DG and TG FinFETs are shown in Fig. 7 which shows increased electron density in the channel for TG case. Table 1 summarizes different performance matrices obtained from 3D simulation of DG and TG FinFETs.

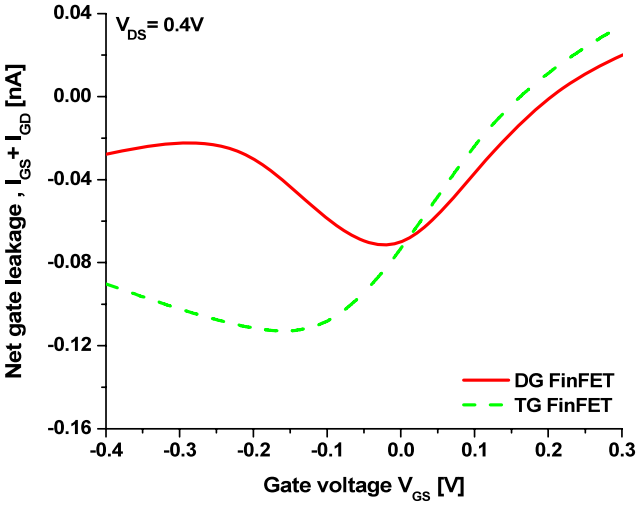

Fig. 6 Net gate leakage current as a function of gate voltage for DG and TG FinFETs at a drain bias, $V_{DS} = 0.4$ V

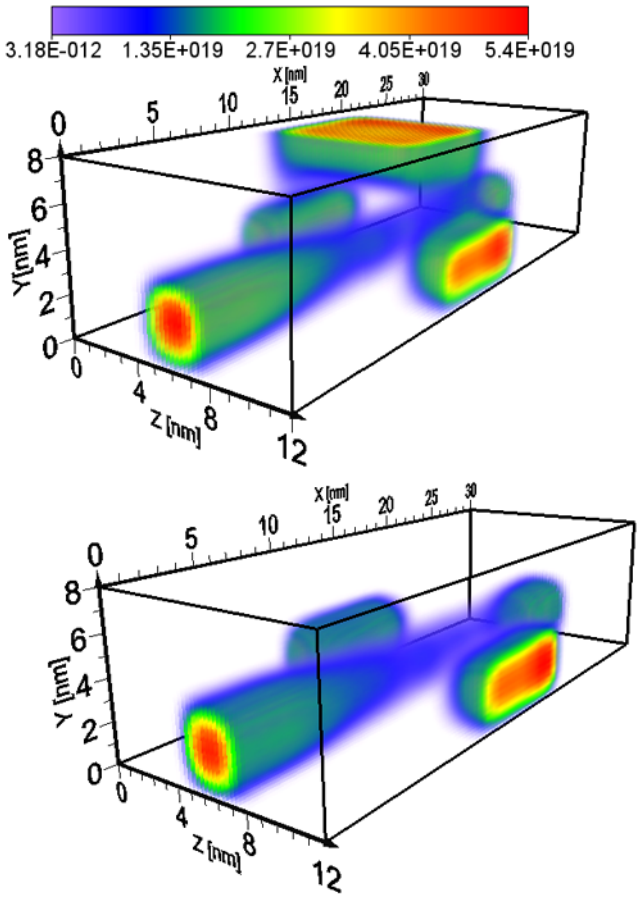

Fig. 7 3D electron density for DG (*bottom*) and TG (*top*) FinFETs at $V_{GS} = 0.2$ V and $V_{DS} = 0.4$ V

4 Effects of an unintentional dopant

We examine the effects of an unintentional dopant (UD) within the channel region on device characteristics using the

Table 1 Performance matrices for DG and TG FinFETs

Parameter	DG	TG
I_{DS} @ $V_{DS} = 0.4$ V, $V_{GS} = 0.3$ V (μA)	8	9.6
I_{DS} @ $V_{DS} = 0.4$ V, $V_{GS} = -0.4$ V (nA)	0.138	0.015
Subthreshold swing (mV/dec)	78	70
$\|I_G\|$ @ $V_{DS} = 0.4$ V, $V_{GS} = -0.4$ V (nA)	0.027	0.090

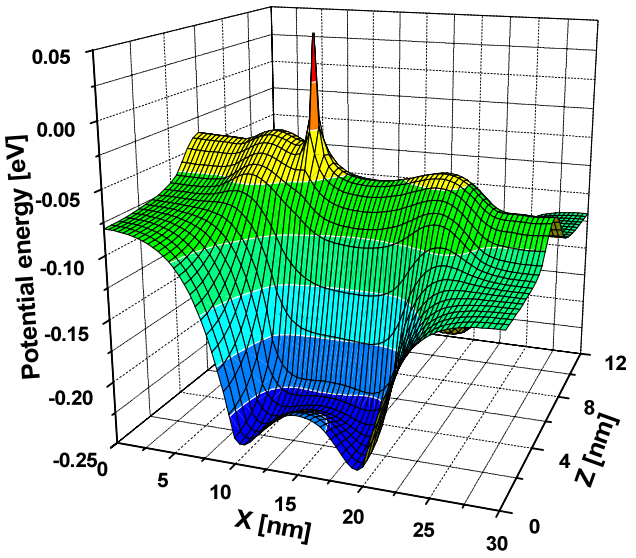

Fig. 8 Potential energy profile in XZ plane at $y = 2$ nm when an UD is present near the source end of the channel at $V_{GS} = 0.2$ V and $V_{DS} = 50$ mV

finite differences approximation and including the unintentional doping into the r.h.s of the discrete Poisson equation. We have checked that in this case, sufficiently small grid size (2 Å) does not introduce any significant inaccuracies in the short-range Coulomb interaction. An unintentional dopant sitting near the source end of the channel degrades the device performance significantly compared to other probable positions [3]. The impact of unintentional dopant heavily depends on its position and applied biases. With change in applied biases the position of the intrinsic barrier shifts and consequently the relative importance of the localized barrier introduced by the unintentional dopant changes.

Figure 8 shows the localized barrier created by an unintentional dopant sitting near the source end of the channel. Also shown in Fig. 9 is the degradation in drain current for the same position of the unintentional dopant in linear and saturation regime of operation.

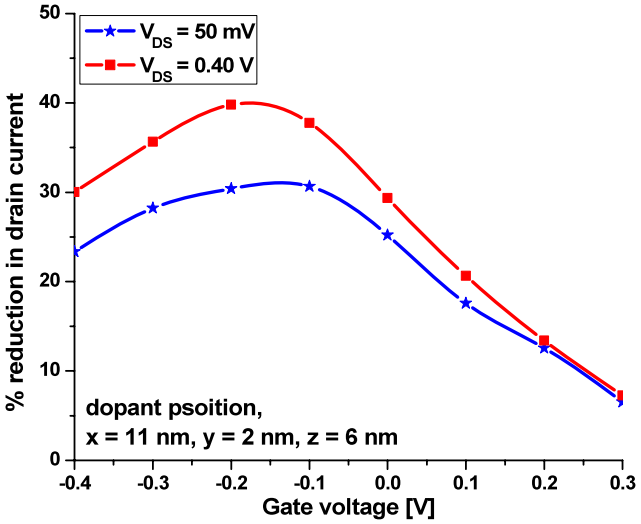

Fig. 9 Decrement in drain current for DG FinFET due to the presence of an UD near the source end of the channel

The reduction in drain current is found to be more pronounced in subthreshold regime than on-state. Also the impact of unintentional dopant is more significant in saturation regime than at linear regime of operation.

5 Conclusion

In this work ultra-scaled DG and TG FinFETs have been simulated to study the impact of fin height and unintentional dopant on device behavior. For small fin height devices, confinement along height is no longer negligible and a truly 3D simulation is necessary. As expected, overall the TG device shows superior performance compared to the DG device (e.g. [4]), however we find that the off-state gate leakage current is about 300% larger in TG case (i.e. in the considered case gate leakage is not linearly scaled with the gate area). We have also found that in both TG and DG devices, unintentional dopant sitting near source end gives highest reduction in drain current. This reduction is more pronounced in saturation than in linear regime.

References

1. Mamaluy, D., et al.: Phys. Rev. B **71**, 245321-1–245321-14 (2005)
2. Khan, H., Mamaluy, D., Vasileska, D.: IEEE Trans. Electron Devices **54**, 784–796 (2007)
3. Khan, H., et al.: J. Comput. Electron. **3**, 337–340 (2004)
4. Kranti, A., et al.: Semicond. Sci. Technol. **21**, 409–421 (2006)