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Modeling of FinFET: 3D MC Simulation Using FMM and Unintentional Doping Effects on Device Operation

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Abstract. Novel device concepts such as dual gate SOI, Ultra thin body SOI, FinFETs, etc., have emerged as a solution to the ultimate scaling limits of conventional bulk MOSFETs. These novel devices suppress some of the Short Channel Effects (SCE) efficiently, but at the same time more physics based modeling is required to investigate device operation. In this paper, we use semi-classical 3D Monte Carlo device simulator to investigate important issues in the operation of FinFETs. Fast Multipole Method (FMM) has been integrated with the EMC scheme to replace the time consuming Poisson equation solver. Effect of unintentional doping for different device dimensions has been investigated. Impurities at the source side of the channel have most significant impact on the device performance.

Keywords: FinFET, unintentional doping, FMM, 3D Monte Carlo

1. Introduction

Scaling of conventional bulk-MOSFETs is approaching physical limits due to the upper limit imposed on the oxide thickness, S/D junction depth, etc. As channel length shrinks below 50 nm [1], complex channel profiles are required to achieve desired threshold voltage and to alleviate short channel effects [2]. The double gate MOSFET has been proposed as a promising structure [3]. With two gates controlling the entire fully depleted channel film, SCEs can be greatly suppressed. Among different double gate devices, FinFET, a recently reported novel device structure is found to show better performance. FinFET becomes attractive due to its quasi-planar structure, better immunity to SCEs, range of channel lengths, CMOS compatibility, good area efficiency compared to other double gate structures [4] and the possibility of using it with strained Si.

Figure 1 depicts the geometry of FinFET being simulated. It consists of channels formed in vertical Si fin controlled by self-aligned double gate [5–7]. The gate straddles the fin on the three faces. The fin height represents the channel width of a single-fin transistor. Fin extensions on both sides of the gate play a significant role on device performance. n^+ polysilicon gate has been assumed as a gate electrode. The fin is usually lightly doped to avoid channel dopant fluctuation and threshold voltage sensitivity to fin width.

2. Simulation Methodology

2.1. Ensemble Monte Carlo

We have used our in house 3D classical Monte Carlo device simulator to obtain transfer and output characteristics. Electron-electron and electron-ion

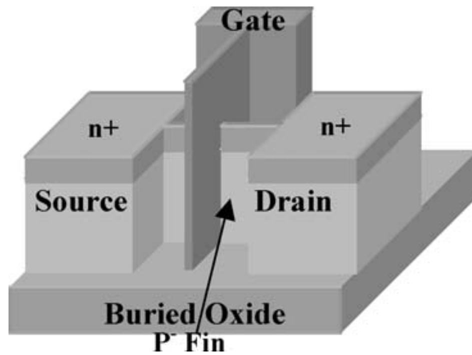

Figure 1. Schematic view of a FinFET structure.

interaction has been included using P3M approach. Intravalley scattering is limited to acoustic phonons. For intervalley scattering we have included both g and f phonons [8]. We have used Incomplete Lower Upper decomposition method to solve 3D Poisson equation. However, the charges obtained from the EMC simulation are usually distributed within the continuous mesh cell instead of on the discrete grid points. The particle mesh method (PM) is used to perform the switch between the continuum in a cell and discrete grid points at the corners of the cell. NEC (Nearest Element Center) scheme has been adopted. The device current is determined by keeping track of the charges entering and exiting each terminal; the net number of charges over a period of the simulation is then used to calculate the terminal current. The method is quite noisy, due to the discrete nature of the electrons and requires long simulation times, on the order of 2 to 3 ps.

2.2. *Fast Multipole Method (FMM)*

FMM algorithm is a novel approach to evaluate all interactions of an N body system with CPU time requirements of order *O(N)*. Direct evaluation requires $O(N^2)$. The complexity of particle-in-cell methods is of the order of $O(N + M \log M)$, where M is the number of mesh points. The basic idea behind FMM algorithm is to use *multipole expansion* [9] to determine the potential V due to a collection of charges as given below

$$V = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{n=0}^{\infty}\frac{1}{R^{n+1}}\int r^n P_n(\cos\theta)\rho(r)d^3r, \quad (1)$$

where $P_n(x)$ is the Legendre polynomial of degree and R is the distance from the origin to the observation point and $\rho(r)$ is the charge density.

This corresponds to a series expansion of charge density $\rho(r)$ in terms of its moments, normalized by the distance to a point R far from the charge distribution. The multipole moment associated with a distant group can be translated into the local coefficient of the expansion associated with a local group. Interactions with particles, which are nearby, are handled directly. Instead of using Poisson solver, FMM library file [10] has been integrated inside 3D Monte Carlo simulator to determine the resultant field experienced by particles.

3. Unintentional Doping Effect

Unintentional doping effect on device performance has been investigated. As device size shrinks, a single dopant atom is likely to exist in the channel region. Even for undoped channel, background doping contribute at least one ionized dopant atom at random position in the channel. This potential source of localized charge gives rise to localized barrier to current flow. Device operation is affected by this localized barrier from both electrostatic (effective increase in doping) and dynamics (transport) points of view. The effect becomes dominant for decreasing fin width. The size of fin extension on both sides of gate affects the role of unintentional doping. Also the change in device on-state current as well as threshold voltage depends on the position of the dopant in the channel.

4. Simulation Results

FinFET devices of different dimensions have been simulated. Short-range interactions have been included using P^3M approach as well as FMM. Results are in good agreement as shown in Fig. 2. Note that the threshold voltage, as seen in transfer characteristics, Fig. 3, is negative due to the use of n^+ polysilicon gate.

We have used FinFET device with $L_g = 20$ nm, S/G gap = D/G gap = 10 nm, Fin width = 10 nm, and t_{ox} = 2.5 nm.

Figure 4 shows the average velocity profile along the channel. Significant velocity overshoot has been observed near source and drain end of the channel. The amount of velocity overshoot heavily depends on the length of the extension length on each side of the gate. As seen in Fig. 4, keeping D/G gap fixed longer

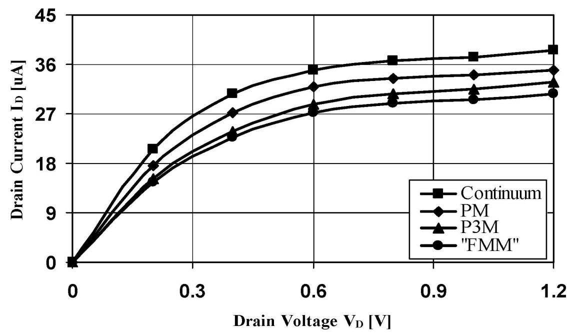

Figure 2. Device Output Characteristics for $V_G = 0.6$ V.

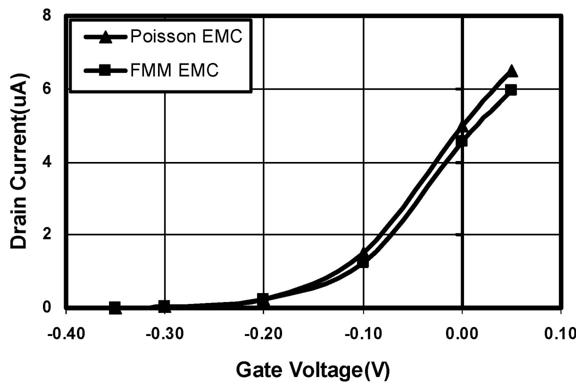

Figure 3. Device Transfer Characteristics for $V_D = 0.1$ V.

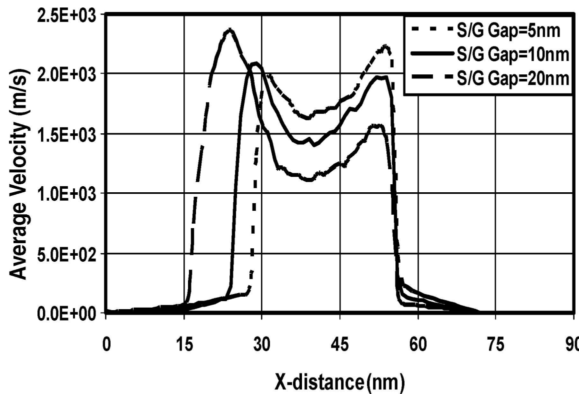

Figure 4. Velocity (along the channel) profile for $V_G = V_D = 0.8$ V.

extension length on source side results in higher velocity near source end and lower velocity near drain end. Opposite phenomena happens for varying D/G gap keeping S/G gap constant.

The effect of fin width on drain current reduction due to unintentional dopant has been observed. For increasingly smaller fin width while keeping other parameters constant, the effect of unintentional dopant on drain current becomes more pronounced. From simulation results it can be concluded that smaller geometry devices will have more impact on performance due to unintentional single charge in the channel region.

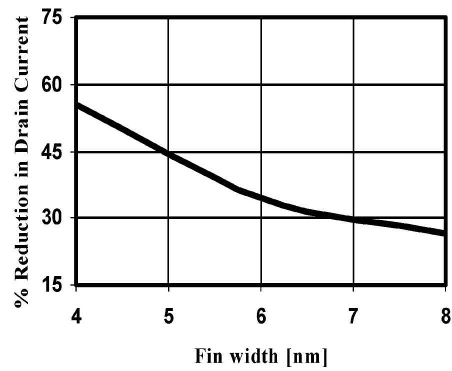

Figure 5. Reduction in drain current as a function of fin width. Dopant atom is placed at the source end of the channel. Fin width = 4 nm, Fin height = 10 nm, $V_G = 0.4$ V, $V_D = 0.1$ V.

Fin extension length also affects the decrement in drain current due to unintentional doping. Longer fin extension results in less influence of drain and source field on barrier created by unintentional dopant and thereby the decrement in drain current becomes more as shown in Fig. 6.

Figure 7 shows the reduction in drain current as a function of single ion dopant position along the channel.

From the simulation result it is vivid that dopant ion at the source side of the channel affects the on

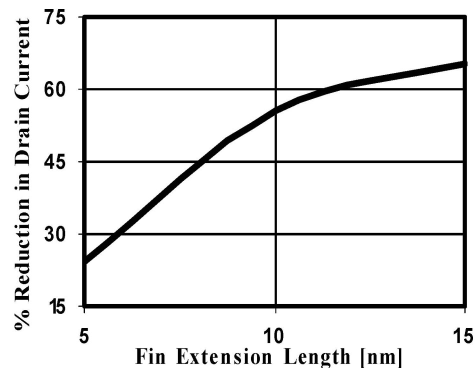

Figure 6. Reduction of drain current as a function of fin extension length. Dopant is placed at the source end of the channel. Fin width = 4 nm, Fin height = 10 nm, $V_G = 0.4$ V, $V_D = 0.1$ V.

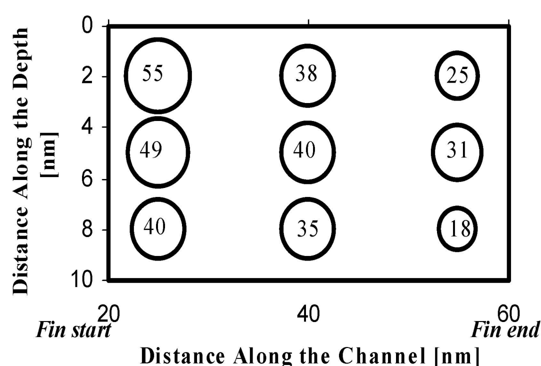

Figure 7. Reduction in drain current as a function of position of unintentional dopant atom along the channel. $V_G = 0.4$ V, $V_D = 0.1$ V.

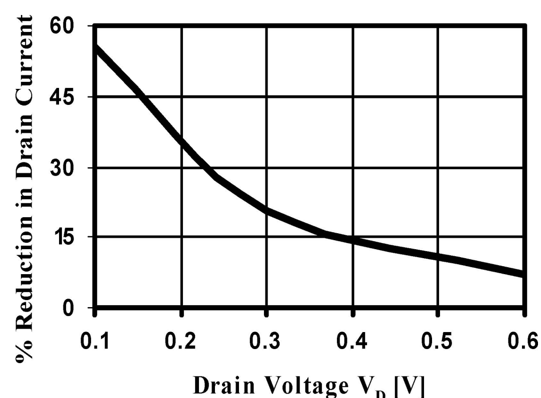

Figure 8. Reduction in drain current as a function of drain voltage. Dopant atom is placed at the source end of the channel near the top interface. Fin width = 4 nm, Fin height = 10 min.

state current most. Near drain end the effect is less pronounced.

The effect of unintentional doping becomes dominant near sub-threshold regime where number of mobile carriers is very few. As gate voltage increases, the electrons in the channel begin to screen the localized potential of the single dopant ion, thus reducing its impact on the current flow. Similarly an increase in drain voltage results smaller reduction in drain current due to more acceleration of the carriers over the localized barrier produced by unintentional dopant.

5. Conclusions

In this work, we have presented the results obtained from 3D Monte Carlo simulation of FinFET devices. Use of FMM algorithm speeds up the simulation significantly and the results are comparable with those obtained by P^3M approach. Appropriate corrections like inclusion of boundary condition and Image charges have been made to FMM library file [10] to make it fully functional for simulating FinFET devices.

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