International Journal of Theoretical Physics (2021) 60:2400–2411
https://doi.org/10.1007/s10773-020-04558-2

An Efficient Design of Parallel and Serial Shift Registers Based on Quantum-Dot Cellular Automata

Shuyan Fan [1] · Maryam Sadat Khamesinia [2]

Received: 16 May 2020 / Accepted: 25 July 2020/ Published online: 26 August 2020
© Springer Science+Business Media, LLC, part of Springer Nature 2020

Abstract
Quantum-dot cellular automata (QCA) is considered as rising nanotechnology, which offers computer calculations at the stage of nano by employing molecular modules as calculational modules. Employing this engineering leads to lower splinter region along less power dissipation and can remove the spatial constraints of Complementary Metal Oxide Semiconductor (CMOS) procedure. Shift registers generally utilize currents in a smart scheme. Therefore, modeling these constructions, along with higher consistency and strength, is significant. This article uses a robust dual-edge triggered QCA-based D flip flops. Efficient parallel-in-parallel-out (PIPO) and serial input-serial output (SISO) QCA-based shift registers are also introduced. The simulation and functionality of the suggested constructions have been verified with QCA designer, and their credit is also verified. Presented architectures contain proper QCA execution and provide the minimum difficulty and occupy an area rather than previous constructions. These circuits achieve a noticeable improvement in cell number.

Keywords Shift register · Serial-input-serial-output (SISO) · Parallel-input-parallel-output (PIPO) · Edge triggered · D flip flop · Quantum-dot cellular automata (QCA)

1 Introduction

Recently, the researches in the nanostructures and quantum dot fields have gained much attention [1–4]. Quantum-dot cellular automata (QCA) as a new electronic paradigm is possibly going to be the main hopeful substitute for future high performance integrated circuits [5–9]. Following the

✉ Shuyan Fan
shuyanifan@126.com

Maryam Sadat Khamesinia
Maryam.Kh@iau.ac.ir

[1] College of Electronic and Information Engineering, Nanjing University of Technology, Nanjing, Jiangsu 211816, China

[2] Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Saveh, Iran

apparent reduction of property extent of Very Large Scale Integration (VLSI) systems, Complementary Metal Oxide Semiconductor (CMOS) technology has met many critical challenges and problems [10–13]. In recent years, research attempts have been concentrated on novel devices to substitute CMOS technology. In this regard, QCA has more attractive due to its ability for performing standard calculations with its vast computation switching velocity, down potency dissipation, and little measures [14–18]. Logic states of QCA are expressed by cells that are constructed from two extra electrons and four quantum dots [19–22]. Information is transmitted through interactions among QCA cells. Therefore, it only eludes flow discharge in circuits [23–27].

One of the most popular sequential circuits is the shift register, which is broadly used in digital systems. The presentation of many digital flows is measured by utilized shift register efficiency [28]. Shift register flow is produced using a collection of flip flops connected to save the data [29]. It can transfer the input signal from one position to either right or left. Shift registers can contain consecutive and collateral entrances and productions. The essential part of the structure of each shift register is the D-flip flop circuits [30–32]. Thus, due to the importance of Parallel-In-Parallel-Out (PIPO) and Serial Input-Serial Output (SISO) among many types of shift registers and their inherent efficient performance, designing new structures with the reduced size is of great importance.

This research proposes an emerging and efficient design for SISO and PIPO shift registers standing on well-optimized dual edge-triggered D-flip flop in QCA technology. Offered 3-bit shift registers are combined of three cascading D-flip flops with the capability to shift data to the right for each clock cycle. Evaluation of suggested structures has been carried out by comparison with some earlier designs in the literature. Proposed power-efficient shift registers have a robust implementation with developments in cell count, area, and latency. The contributions of the current work are:

- Designing a new shift register of PIPO and SISO based on QCA applying dual edge-triggered D-flip flop;
- Examining the offered shift registers and comparing them with existing circuits;
- Verifying the operation and accuracy of suggested plans utilizing QCA designer instrument.

This research is explained in five sections. In the second part, prior similar works of the shift register circuits are reviewed. The new scheme of SISO and PIPO shift register with the utilization of dual edge-triggered D flip flop have been represented in Section 3. QCA layout along simulation outcomes is demonstrated in the fourth part. Besides, the comparison of offered shift registers with other circuits for various parameters is shown in this section. Finally, a conclusion is given in the last section.

2 Related Work

A design of serial shift register using a recent emerging edge-triggered D flip-flop containing readjust susceptibility has been proposed by Zoka and Gholami [33]. Effective execution of D-flip flop flows has utilized a measure for implementing a readjust entrance into D-flip flop. This D-flip flop along a reset entrance is susceptible to a clock edge. Presented D flip flop was applied in a 3-bit sequential shift register for demonstrating the accurate circuit execution. In this shift register, as the readjust entrance is triggered, total outputs become 0. The used cells of

current design have been more than equivalent flows, but it is able to work with identical velocity and postponements of shift registers.

A new designed reversible Serial In Parallel Out (SIPO) shift register with the utilization of reversible Dual Edge Triggered (DET) D flip flop is presented by Singh and Pandey [34]. The used DET D flip flop in this shift register has been schemed to employ two pairs of Fredkin and Feynman gates, which constitute two parallel opposite level-sensitive flip-flops, and the last Fredkin gate is employed as a multiplexer. In 4-bit SIPO shift register, input has been utilized by first flip flop and four outputs taken from all the flip flops. The consequences have illustrated the fact that the energy consumed of introduced design is ultra-low.

Also, a new 3-bit SISO QCA-based shift register depending on three new D flip flop circuits has been presented by Divshali et al. [28]. In this work, the first three QCA D-flip flops are provided, and then they are used to design the SISO shift register. This shift register has been executed in 5 categories that D flip flops have been applied in groups 1, 3, and 5. The second and fourth categories have been executed to transfer information. 5-layer 3-bit QCA-based SISO shift register flow provides better performance of the region.

In the end, Das and De [35] have suggested an optimum SISO shift register structure with the utilization of a novel QCA D flip-flop layout. Level sensitive construction D flip-flop has been obtained utilizing a bound node 3-bit SISO shift register, which is produced of three connected D flip flops. The presented shift register has been obtained in one category and has a lower cell amount with more system aggregate in compared to others. Energy utilization examinations have demonstrated that the suggested scheme includes down power utilization. Table 1 compares the significant benefits and defects of reviewed QCA-based shift register schemes.

3 Proposed Design

D-type flip flops are primary blocks in many digital circuits such as shift registers and as an essential storage element that can maintain a binary state [36]. Therefore, many researchers try to complete the efficiency of D flip flop circuits. This section introduces a Dual Edge Triggered QCA-based D-flip flop

Table 1 Summary of prior explained QCA shift registers

Article	Main opinion	Pros	Cons
Zoka and Gholami [33]	Presenting serial shift register using a new appearing edge-triggered D flip-flop utilizing QCA	• Low delay • High speed	• High area consumption • High complexity
Singh and Pandey [34]	Proposing a reversible dual edge-triggered D flip flop and implementation of a new reversible SIPO shift register in QCA technology	• Low power consumption • Improving latency	• Increasing complexity • Increasing area
Divshali, et al. [28]	Proposing a new multilayer 3-bit SISO QCA shift register	• Low consumption area • Improving cell count • High performance	• High clocking cycle
Das and De [35]	Proposing an optimized design and execution of D flip-flop and 3-bit SISO shift register utilizing QCA	• Low cell numbers • Low area • Low energy utilization • Stability under thermal randomness	• Low speed

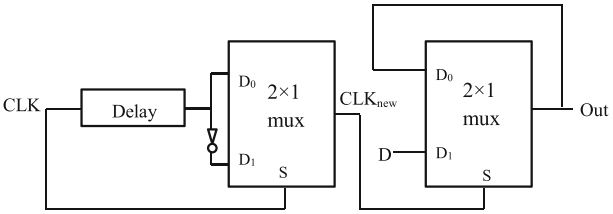

Fig. 1 Schematic of dual edge-triggered D flip flop

extracted from a suggested design by Roshan and Gholami [37]. Then, an impressive and novel scheme has been proposed for PIPO and SISO shift registers standing on QCA-based D-flop flop circuit. In the current structure, D latch has been planned using a multiplexer through response by production toward first input along with proper postponement with feedback route. A level-to-edge triggered converter has been utilized for transforming latch to flip flop. In this converter, a 2 to 1 multiplexer is utilized, where a clock signal applied to select input and created a postponement cycle in clock conversion route to two D_0 and D_1 inputs of multiplexer. Therefore, standing on this method, the clock ongoing amount with the previous state of it can be produced. Thus, eq. 1 can be considered for the converter of dual-edge. Figure 1 depicts the Dual Edge Triggered D flip flop structure.

$$CLK_{new} = \overline{CLK_t}.CLK_{t-1} + CLK_t.\overline{CLK}_{t-1} \tag{1}$$

Table 2 summarizes the falling edge-triggered D Flip-Flop truth table. As can be seen, if CLK_t and CLK_{t-1} are 0, the output on the base flip flop prior amount (D_0) is determinant and indicating that there is no edge. When CLK_t is 1 and $CLK_{t-1}$is 0, the production has been the same with the amount in D_1 that illustrates the accurate recognition of emerging edge. When CLK_t is 0 and $CLK_{t-1}$is 1, the output is the same with the amount on D_1, which reflects the accurate falling edge recognition. Eventually, if CLK_t and CLK_{t-1} are equal to 1, the output is the same with the amount of D_0 and maintains the prior flip flop amount.

Shift register as a type of sequential circuits is composed of a flip-flops chain linked to each other in a way that its content is able to modify one location to right or left. An *n* bit shift register includes *n* D flip flop. Those flip flops have been managed by an ordinary clock. SISO and PIPO shift registers are the most comfortable shift registers that contain only flip flops. The single flip flop production is inputted to the subsequent flip flop following the clock in SISO shift register. In suggested QCA SISO shift register, serial input has been utilized for the leftmost dual edge-triggered QCA D flip flop, and sequential production has been obtained from the rightmost dual edge. The 3-bit SISO shift register schematic structure that, with each

Table 2 The dual edge-triggered D flip flop truth table

CLK_{t-1}	CLK_t	D	Out
0	0	0	Q_{t-1}
0	0	1	Q_{t-1}
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	Q_{t-1}
1	1	1	Q_{t-1}

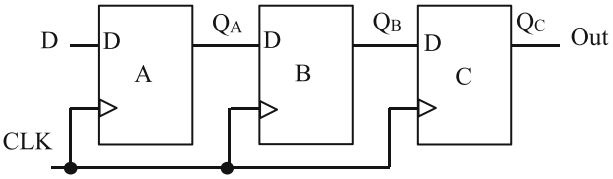

Fig. 2 Schematic 3-bit SISO shift register diagram

clock, pulse changes the input register data one bit to the right, has been indicated in Fig. 2. In QCA PIPO shift register, the entrances have been filled in parallel in dual edge-triggered QCA flip flops concurrently. Besides, they are accessible in collateral by flip flops' different stages in the chain. Figure 3 shows a 3-bit PIPO shift register block diagram with 3 separate inputs.

4 Simulation Results

In this part, first, a glance at the used tool to simulation is provided, and then the suggested shift registers' QCA-based plan, their output waveforms, and analogy with modern plans have been considered.

4.1 Simulation Tool

QCA designer has been considered as an accurate simulator that mimics the QCA parts and finds the condition of the entrance to production signs as the outcomes. This tool is developed for functionality checking of QCA circuits and allows the designer to abruptly layout [38]. QCA designer version 2.0.3 has been applied to detect functional correctness of suggested structures. Simulation parameters, which mentioned in Fig. 4, have been in predetermined values, and a bistable approximation processing engine is employed for testing various settings.

4.2 The Layout of Suggested Designs

QCA dual edge-triggered D flip flop execution architecture has been indicated in Fig. 5. As can be seen, in this architecture, the whole of the outputs and inputs have been accessible for utilizing in huger circuits, and only one layer is needed. This D flip flop is composed of 49 QCA cells with an occupation space of 0.04 $\mu m^{2,}$ and the input signal is delivered to the output after 2 clock flow delay. Cells containing diverse colors express four signals of the clock that are employed for contemporizing and manage one another cycle pieces by rights.

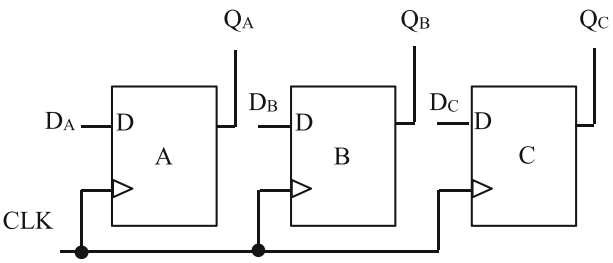

Fig. 3 Schematic 3-bit PIPO shift register diagram

Number Of Samples:	12800
Convergence Tolerance:	0.001000
Radius of Effect [nm]:	65.000000
Relative Permittivity:	12.900000
Clock High:	9.800000e-022
Clock Low:	3.800000e-023
Clock Shift:	0.000000e+000
Clock Amplitude Factor:	2.000000
Layer Separation:	11.500000
Maximum Iterations Per Sample:	100

Fig. 4 QCADesigner parameters for bistable approximation engine

The 3-bit SISO shift register QCA layout standing on dual edge-triggered D-flip flop has been indicated in Fig. 6. The proposed single layer shift register is constructed of three D-flip flops and includes one clock entrance, single information entrance, and one production from last flip flop. As can be seen in this SISO shift register, 167 QCA cells have been used, and the space occupied is 0.22 μm^2. Serial data are shifted to the right and appear on output after 6 cycles of clock postponement. Moreover, presented 3-bit PIPO shift register QCA plan has been indicated in Fig. 7. The offered flow has been executed in one layer and produced of three dual edges triggered D-flip flops. This type of shift register has three data inputs, three outputs, and one common clock input. The cells' item of this execution has been considered about 177,

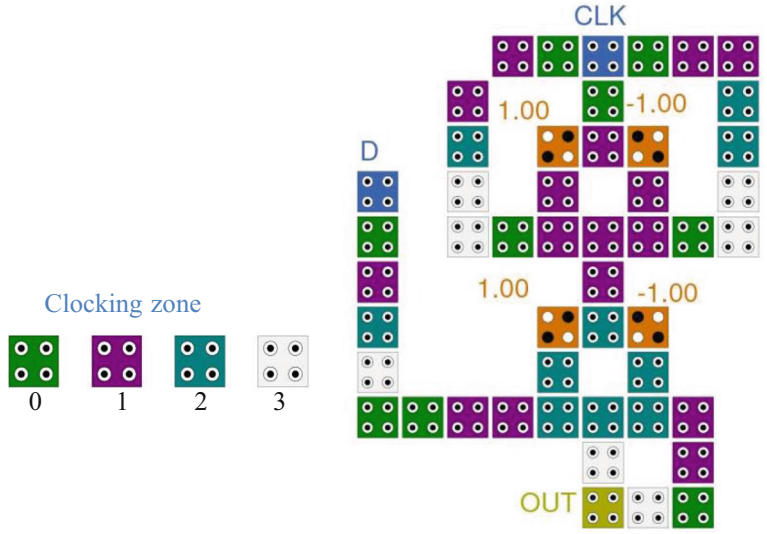

Fig. 5 The dual edge-triggered D flip flop scheme in QCA

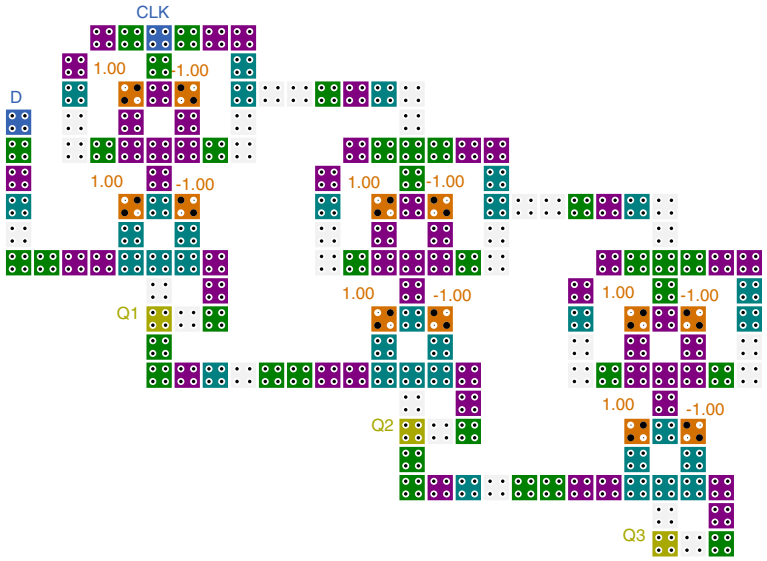

Fig. 6 Suggested 3-bit SISO shift register design in QCA

and the region reports 0.16 μm^2. 3-bit information has been produced by D_1, D_2, D_3 in collateral, and after 2 clock cycle postponement, information obtained is gathered as production based on their ranking from Q_1, Q_2, Q_3.

4.3 Validity Analysis

Figure 8 depicts the valid performance of dual edge-triggered D flip flop. Different dual amounts have been utilized at D entrance. The D input amounts are moved to the output in falling and rising clock edges. D has been 0 in clock's first collapsing edge. So, the efficiency will be 0. The output does not experience any alternation until the subsequent ascending clock edge. Now, the insert of D is equal to 1, so the output is changed to 1. This design spans 2 clock cycle delay from input to output.

Implementation outcomes of suggested 3-bit QCA SISO shift register have been indicated in Fig. 9. In the earliest falling of the clock edge, the D input values are 0,

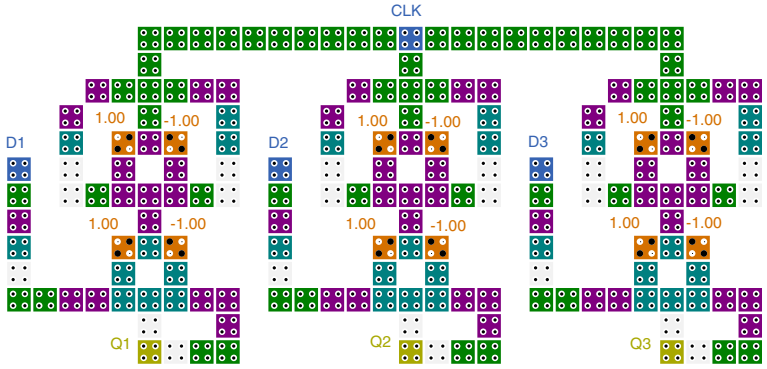

Fig. 7 Suggested 3-bit PIPO shift register design in QCA

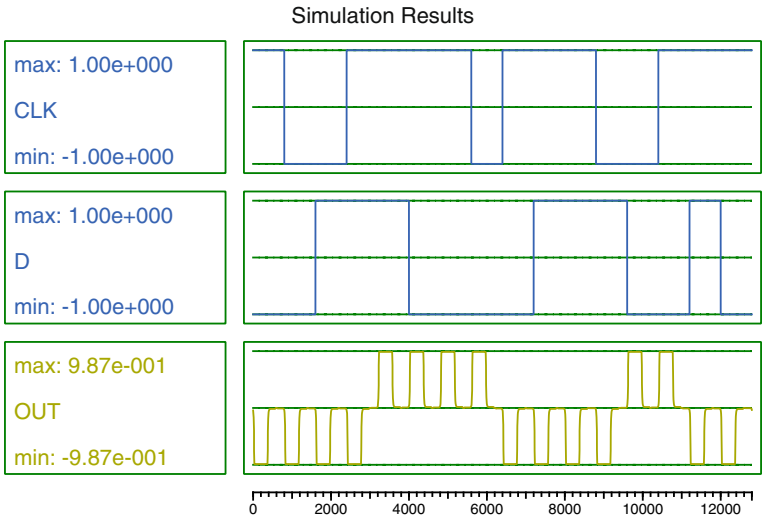

Fig. 8 Simulation waveforms for QCA dual edge-triggered D flip flop

which is entered to Q_A while Q_B and Q_C are still empty. In the next ascending clock edge, the input of D has been 1, which is entered to Q_A, and prior D amount input is shifted to the right at located Q_B while Q_C still remains empty. In the third clock edge, the input of D entered to Q_A with the amount of 0, value of insert of D from the second stage is shifted to B while the value of D input in Q_B previously is now shifted to Q_C and so on. Afterwards, the earliest significant Q_C efficiency will be

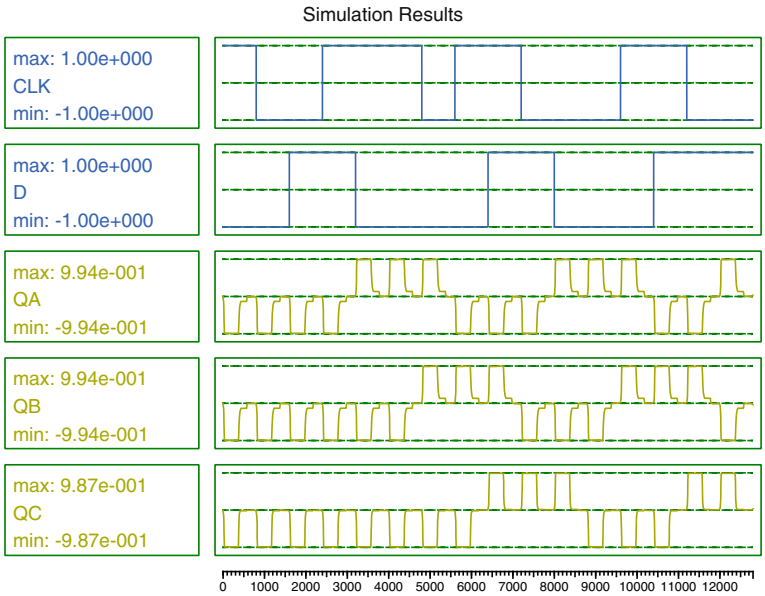

Fig. 9 Simulation waveforms for 3-bit QCA SISO shift register

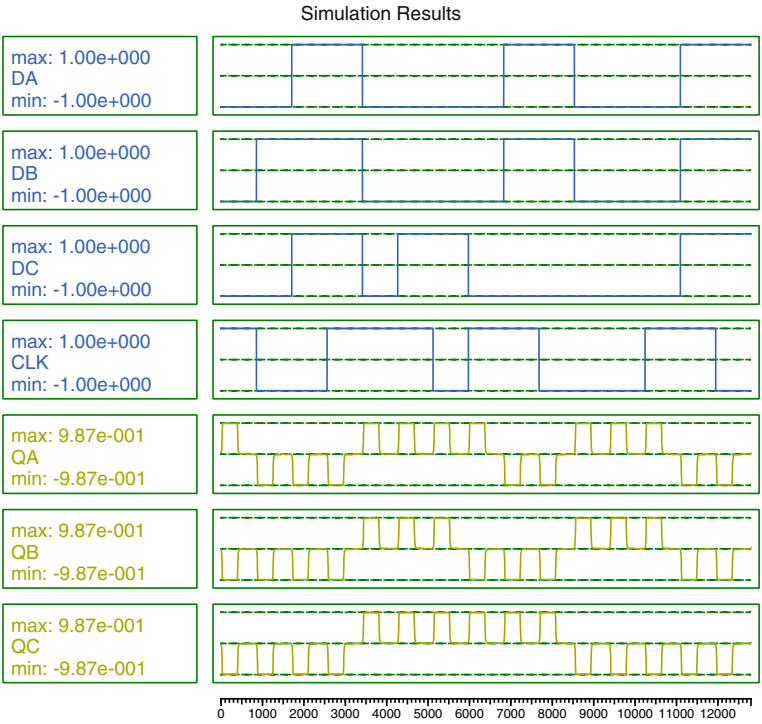

Fig. 10 Simulation waveforms for 3-bit QCA PIPO shift register

obtained after 6 clock flow postponement. Moreover, Fig. 10 depicts the execution outcomes of suggested 3-bit QCA PIPO shift register. Collateral data have been filled in register altogether and shifted to their relevant productions via the same clock edge. Consequences show accurate production after 2 clock flow.

Table 3 The presented 3-bit QCA shift registers' comparative table with other related works

QCA shift register	Effective area (μm^2)	Number of QCA cells	Delay (clock cycle)	Type of layer
3-bit SISO shift register				
SISO shift register utilizing edge triggered D flip flop of [33]	0.50	470	3	Coplanar
Proposed SISO shift register utilizing edge triggered D flip flop	0.22	167	6	Not required
3-bit PIPO shift register				
PIPO shift register utilizing level triggered D flip flop of [39]	0.19	188	1	Not required
Proposed PIPO shift register utilizing edge triggered D flip flop	0.16	177	2	Not required

4.4 Comparisons

Suggested PIPO and SISO shift registers are compared in Table 3 with previous designs. Based on implementation results, it can be proven that the proposed 3-bit shift registers are superior compared to other related works concerning the occupied area requirement and the number of cells. The 3-bit shift registers are based on edge-triggered D flip flop while PIPO shift register in [39] is based on Level Triggered D flip flop. The indicated designs can be easily extended to n-bit since all inputs are available. Also, the results can be found that although proposed shift registers operate with a higher latency than similar circuits, but provide better performance.

5 Conclusion and Future Works

Efficient and robust 3-bit PIPO and SISO shift register designs based on an optimal dual edge-triggered D flip flop model in QCA technology have been introduced in this article. Suggested 3-bit QCA shift register circuits are executed in one layer that supplies the circulations' easiness. Simulations are performed using the bistable approximation engine and a collection of vector table simulation outcomes of QCA designer tool. Also, these two circuits' structural attributes are discussed in effective regions, difficulty, and delay that indicate a significant preference of suggested layouts due to the area occupation and cell count. These structures may be impressive for the design of high-performance digital systems and circuits in the future. Moreover, the proposed QCA-based shift registers are able to be developed to the great layout of instruction. They might be utilized as the main instruction block of common target nano-computers. Risk and reliability assessment [40–42] of suggested design is another absorbing script for further investigations. Finally, the delay and speed optimization from sequential circuit modules could be considered for future studies.

References

1. Farhangian, H., Abrishamifar, S.M., Palizian, M., Janghorban Lariche, M., Baghban, A.: The application of nanofluids for recovery of asphaltenic oil. Pet. Sci. Technol. **36**(4), 287–292 (2018)
2. Hosseini, M., Kahkha, M.R.R., Fakhri, A., Tahami, S., Lariche, M.J.: Degradation of macrolide antibiotics via sono or photo coupled with Fenton methods in the presence of ZnS quantum dots decorated SnO2 nanosheets. J. Photochem. Photobiol. B Biol. **185**, 24–31 (2018)
3. M. J. Lariche *et al.*, "Developing supervised models for estimating methylene blue removal by silver nanoparticles," Energy Sources, Part A: Recovery, Utilization, and Environmental Effects, pp. 1–8, 2019
4. Zuo, X., Behradfar, K., Liu, J.-B., Lariche, M.J., Najafi, M.: Theoretical study of ability of boron nitride nanocone to oxidation of sulfur monoxide. Acta Chim. Slov. **65**(2), 296–302 (2018)
5. Afrooz, S., Navimipour, N.J.: Memory designing using quantum-dot cellular automata: systematic literature review, classification and current trends. *Journal of Circuits, Systems and Computers*. **26**(12), 1730004 (2017)
6. Fam, S.R., Navimipour, N.J.: Design of a loop-based random access memory based on the nanoscale quantum dot cellular automata. Photon Netw. Commun. **37**(1), 120–130 (2019)
7. Gadim, M.R., Navimipour, N.J.: A new three-level fault tolerance arithmetic and logic unit based on quantum dot cellular automata. Microsyst. Technol. **24**(2), 1295–1305 (2018)
8. Gadim, M.R., Navimipour, N.J.: Quantum-dot cellular automata in designing the arithmetic and logic unit: systematic literature review, classification and current trends. *Journal of Circuits, Systems and Computers*. **27**(10), 1830005 (2018)

9. A. Sandhu and S. Gupta, "Performance Evaluation of an Efficient Five-Input Majority Gate Design in QCA Nanotechnology," *Iranian Journal of Science and Technology, Transactions of Electrical Engineering,* 2019/12/16 2019
10. Roohi, A., Khademolhosseini, H., Sayedsalehi, S., Navi, K.: A symmetric quantum-dot cellular automata design for 5-input majority gate. J. Comput. Electron. **13**(3), 701–708 (2014)
11. Xiao, L.-r., Chen, X.-x., Ying, S.-y.: Design of dual-edge triggered flip-flops based on quantum-dot cellular automata. Journal of Zhejiang University SCIENCE C. **13**(5), 385–392 (2012)
12. Moharrami, E., Navimipour, N.J.: Designing nanoscale counter using reversible gate based on quantum-dot cellular automata. Int. J. Theor. Phys. **57**(4), 1060–1081 (2018)
13. Afrooz, S., Navimipour, N.J.: Fault-tolerant Design of a Shift Register at the nanoscale based on quantum-dot cellular automata. Int. J. Theor. Phys. **57**(9), 2598–2614 (2018)
14. Yang, X., Cai, L., Zhao, X., Zhang, N.: Design and simulation of sequential circuits in quantum-dot cellular automata: falling edge-triggered flip-flop and counter study. Microelectron. J. **41**(1), 56–63 (2010)
15. Chaves, J.F., Ribeiro, M.A., Silva, L.M., de Assis, L.M., Torres, M.S., Neto, O.P.V.: Energy efficient QCA circuits design: simulating and analyzing partially reversible pipelines. J. Comput. Electron. **17**(1), 479–489 (2018)
16. S. Babaie, A. Sadoghifar, and A. N. Bahar, "Design of an Efficient Multilayer Arithmetic Logic Unit in Quantum-Dot Cellular Automata (QCA)," IEEE Transactions on Circuits and Systems II*:* Express Briefs*,* 2018
17. Seyedi, S., Darbandi, M., Navimipour, N.J.: Designing an efficient fault tolerance D-latch based on quantum-dot cellular automata nanotechnology. Optik. **185**, 827–837 (2019)
18. Seyedi, S., Navimipour, N.J.: An optimized design of full adder based on nanoscale quantum-dot cellular automata. Optik. **158**, 243–256 (2018)
19. R. Chakrabarty, D. K. Mahato, A. Banerjee, S. Choudhuri, M. Dey, and N. Mandal, "A novel design of flip-flop circuits using quantum dot cellular automata (QCA)," in *2018 IEEE 8th Annual Computing and Communication Workshop and Conference (CCWC)*, 2018: IEEE, pp. 408–414
20. Shamsabadi, A.S., Ghahfarokhi, B.S., Zamanifar, K., Movahedinia, N.: Applying inherent capabilities of quantum-dot cellular automata to design: D flip-flop case study. J. Syst. Archit. **55**(3), 180–187 (2009)
21. Afrooz, S., Navimipour, N.J.: Memory designing using quantum-dot cellular automata: systematic literature review, classification and current trends. Journal of Circuits, Systems and Computers. **26**, 1730004 (2017)
22. Kummamuru, R.K., Orlov, A.O., Ramasubramaniam, R., Lent, C.S., Bernstein, G.H., Snider, G.L.: Operation of a quantum-dot cellular automata (QCA) shift register and analysis of errors. IEEE Transactions on electron devices. **50**(9), 1906–1913 (2003)
23. Zhang, Y., Xie, G., Lv, H.: Dual-edge triggered JK flip-flop with comprehensive analysis in quantum-dot cellular automata. The Journal of Engineering. **2018**(7), 354–359 (2018)
24. Abedi, D., Jaberipur, G.: Decimal full adders specially designed for quantum-dot cellular automata. IEEE Transactions on Circuits and Systems II: Express Briefs. **65**(1), 106–110 (2018)
25. Seyedi, S., Navimipour, N.J.: Design and evaluation of a new structure for fault-tolerance full-adder based on quantum-dot cellular automata. Nano communication networks. **16**, 1–9 (2018)
26. S. Seyedi and N. J. Navimipour, "An optimized three-level Design of Decoder Based on Nanoscale quantum-dot cellular automata," Int. J. Theor. Phys*.,* pp. 1–12, 2018
27. Sherizadeh, R., Navimipour, N.J.: Designing a 2-to-4 decoder on nanoscale based on quantum-dot cellular automata for energy dissipation improving. Optik. **158**, 477–489 (2018)
28. Divshali, M.N., Rezai, A., Karimi, A.: Towards multilayer QCA SISO shift register based on efficient D-FF circuits. Int. J. Theor. Phys. **57**(11), 3326–3339 (2018)
29. N. M. Nayeem, M. A. Hossain, L. Jamal, and H. M. H. Babu, "Efficient design of shift registers using reversible logic," in *2009 International Conference on Signal Processing Systems*, 2009: IEEE, pp. 474–478
30. Abutaleb, M.: A novel power-efficient high-speed clock management unit using quantum-dot cellular automata. *Journal of Nanoparticle Research*. **19**(4), 128 (2017)
31. B. Sen, M. Goswami, S. Some, and B. K. Sikdar, "Design of sequential circuits in multilayer qca structure," in *2013 International Symposium on Electronic System Design*, 2013: IEEE, pp. 21–25
32. R. Binaei and M. Gholami, "Design of Multiplexer-Based D Flip-Flop with set and reset ability in quantum dot cellular automata nanotechnology," Int. J. Theor. Phys*.,* pp. 1–13, 2018
33. Zoka, S., Gholami, M.: A novel rising edge triggered resettable D flip-flop using five input majority gate. Microprocess. Microsyst. **61**, 327–335 (2018)
34. Singh, R., Pandey, M.K.: Analysis and implementation of reversible dual edge triggered d flip flop using quantum dot cellular automata. International journal of innovative computing information and control. **14**(1), 147–159 (2018)

35. Das, J.C., De, D.: Operational efficiency of novel SISO shift register under thermal randomness in quantum-dot cellular automata design. Microsyst. Technol. **23**(9), 4155–4168 (2017)
36. T. Sarkar, "Design of D Flip-Flip Using Nano-Technology Based Quantum Cellular Automata," *International Journal of Soft Computing and Engineering (IJSCE),* 2013
37. Roshan, M.G., Gholami, M.: Novel D latches and D flip-flops with set and reset ability in QCA nanotechnology using minimum cells and area. Int. J. Theor. Phys. **57**(10), 3223–3241 (2018)
38. Walus, K., Dysart, T.J., Jullien, G.A., Budiman, R.A.: QCADesigner: a rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans. Nanotechnol. **3**(1), 26–31 (2004)
39. T. Purkayastha, D. De, and T. Chattopadhyay, "Universal Shift Register Implementation Using Quantum Dot Cellular Automata," *Ain Shams Engineering Journal,* 2016
40. Bagal, H.A., Soltanabad, Y.N., Dadjuo, M., Wakil, K., Ghadimi, N.: Risk-assessment of photovoltaic-wind-battery-grid based large industrial consumer using information gap decision theory. Sol. Energy. **169**, 343–352 (2018)
41. Ahadi, A., Ghadimi, N., Mirabbasi, D.: Reliability assessment for components of large scale photovoltaic systems. J. Power Sources. **264**, 211–219 (2014)
42. Saeedi, M., Moradi, M., Hosseini, M., Emamifar, A., Ghadimi, N.: Robust optimization based optimal chiller loading under cooling demand uncertainty. Appl. Therm. Eng. **148**, 1081–1091 (2019)

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.