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Design of Ultra-Efficient Reversible Gate Based 1-bit Full Adder in QCA with Power Dissipation Analysis

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Abstract
The difficulties which the CMOS technology is facing at the nano scale has led to the investigation of quantum-dot cellular automata (QCA) nanotechnology and reversible logic as an alternative to conventional CMOS technology. In this paper, these two paradigms have been combined. Firstly, a new 3 × 3 reversible gate, SSG-QCA, which is universal and multifunctional in nature, is proposed and implemented in QCA using conventional 3-input majority voter based logic. By using the concept of explicit interaction of cells, the proposed gate is further optimized and then used to design an ultra-efficient 1-bit full adder in QCA. The universal nature has been verified by designing all the logic gates from the proposed SSG-QCA gate whereas the multifunctional nature is verified by implementing all the 13 standard Boolean functions. The proposed 3 × 3 gate and adder designs are then extensively compared with the existing literature and it is observed that the proposed designs are ultra-efficient in terms of both area and cost in QCA technology. In addition to this energy dissipation analysis for different scenarios is also done on all the designs and it is observed that the proposed designs dissipate minimum energy thereby making them suitable for ultra-low power designs.

Keywords QCA · Reversible gate · Universal gate · Full adder · Nanotechnology · Quantum cells · Energy estimation

1 Introduction

CMOS-VLSI technology is facing serious challenges such as high power consumption, threshold voltages, thermal runaway and high leakage current [1–3]. ITRS (International Technology and Roadmap for Semiconductors) has led to significant efforts to find appropriate alternatives to these challenges [3, 4]. Emerging nanotechnologies seems a good competition for future generation digital systems [2, 5]. In this direction, Quantum-Dot Cellular Automata (QCA) is one of the promising

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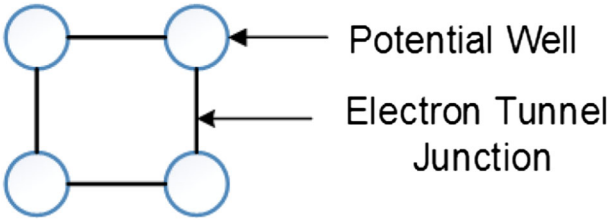


Fig. 1 Basic QCA cell

technology. Quantum-dot Cellular Automata (QCA) is a newly developed paradigm for digital design and offers a breakthrough required for the fulfilment of certain lacking aspects of CMOS technology in the nano regime [4, 6]. Since the technology is new and in the premature phase a lot of scope lies ahead of researchers to take the designing using QCA to a commercial level.

Information loss is indeed the major issue among VLSI micro-technologies. According to Landauer [7], the processing of information in digital circuits leads to the generation of heat due to the erasing of bits. He suggested that for 1 bit loss of information, KTln2 joules of energy is dissipated. However, in 1973 Bennett demonstrated the validity of KTln2 joules of energy dissipation in irreversible circuits can be recovered by reversible circuit [8–11]. Less energy dissipation is possible only if the gate is reversible. A gate is said to be logically reversible if there is one-to-one mapping between the inputs and outputs and the number of inputs are equal to the number of outputs. Besides this logical reversibility the physical reversibility is also important. This means that the reversible logic gates must be optimized in accordance with the circuit stability. This would result in an effective reversible computation.

1.1 QCA Nanotechnology

The basic component in the QCA circuits consists of QCA cell as shown in Fig. 1.

The basic cell consists of four quantum dots or metal islands in which two electrons are allowed to localize [4, 6]. The dots are separated by tunnel junctions through which the electrons can move from one site to another. Columbic electromagnetic interactions are responsible for QCA operation. Due to columbic forces the electrons are allowed to occupy the antipodal sites. This results in two polarization states, binary zero and binary one as shown in Fig. 2.

The cell to cell interactions are responsible for the transmission of information between the cells. So, there is no voltage or current flow between the cells. Therefore, there is no energy dissipation during the state transition and propagation. As a result, low energy is dissipated as compared to the CMOS-VLSI technology [3, 12, 13]. The basic building blocks in QCA are the binary wire, inverter and majority voter. Grid of QCA cells acts as a wire and is used for signal propagation as shown in Fig. 3. The 3 input Majority gate and Inverter are used for implementing QCA circuit techniques as shown in Fig. 4 and Fig. 5.

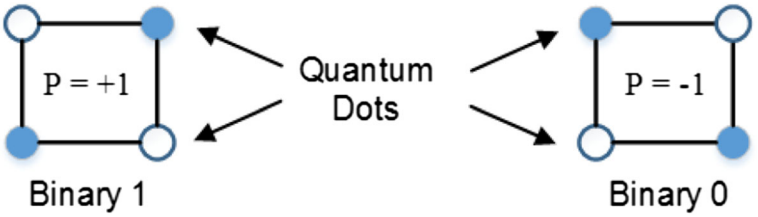


Fig. 2 QCA cell polarization and binary representation

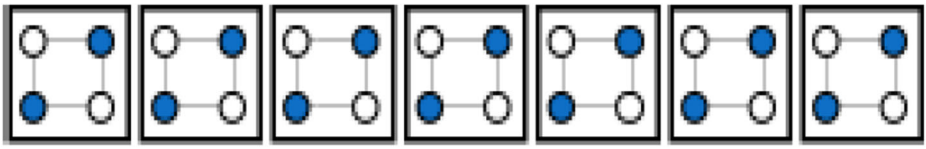


Fig. 3 Interaction between the cells in QCA wire

For the proper functioning of the QCA circuits, they are provided with the clock signals which controls the information flow. The clock is provided in four zones with each zone having four phases. The four phases are switch, hold, release and relax. Initially the cells have low potential barriers and are in the unpolarized state. During the switch phase of the clock cycle the cell is influenced by the neighbouring cell polarization which causes it to take up a new state. After achieving the new polarization due to the neighbouring cell the barriers between the dots are raised such that no further change of state can occur. During the hold phase the cell holds the state and barriers are maintained high. In this phase the cells act as input to the neighbouring cells. In the release and relax phase the barriers between the dots are lowered which results in the loss of polarisation due to tunnelling of electrons and the cell again achieves a null polarization [3, 4, 6]. The entire clocking process and its different phases are shown in Fig. 6.

2 Proposed Reversible SSG-QCA Gate

In this paper, a 3 × 3 reversible logic gate called SSG-QCA is proposed. The proposed gate is a 3 input and 3 output gate having its input vector (IV) and output vector (OV) as:

$$IV = (A, B, C) \tag{1}$$

$$OV = (P = B \oplus C, Q = A \oplus B, R = AB + BC + CA) \tag{2}$$

Figure 7 shows the block diagram representation of the proposed gate whereas the truth table presented in Table 1 verifies the reversible nature of the proposed gate.

The equations of the proposed gate have been designed in such a way that there is a one-to-one mapping between the inputs and outputs as is evident from Table 1.

3 SSG-QCA AS a Universal Structure

A gate is said to be universal if it can operate as all seven logic gates. The SSG-QCA can act as universal gate by manipulating the various inputs of the gate. The input combinations required for implementation of these logic functions are given in Table 2.

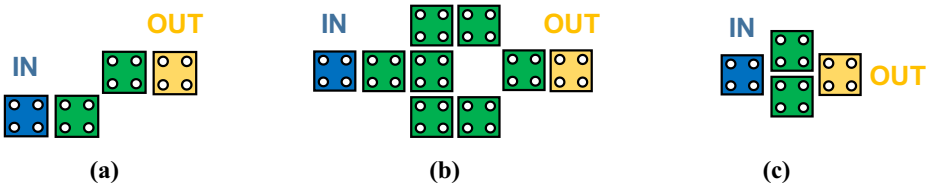


Fig. 4 Various QCA Inverters (**a**) Half-Cell Displaced, (**b**) Large Robust and (**c**) Rotated Cell

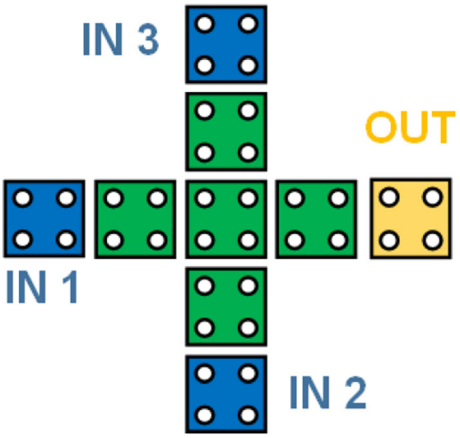


Fig. 5 3-Input Majority Voter Gate in QCA

A gate is said to be universal if it can implement the basic seven Boolean functions. The SSG-QCA can act as universal gate by manipulating the various inputs of the gate. If the gate is to be used as an inverter i.e., NOT gate then the desired output whose compliment is to be achieved is applied at input B in its complemented form and a logic 1 is applied to input A and a logic 0 to input C. An AND operation for two inputs A and B can be realized, if the first input and the second input is kept as it is at input A and input B respectively, and the input C is set to logic 0. Now, if the first input and the second input is set to the complemented value of the input A and input B, and input C is set to logic 1 then NAND operation can be realized for the two inputs. In order to perform OR operation, the first input and the second input is kept as it is at input A and input B, and logic 1 is applied at input C. A NOR operation can be realized, if input A and input B is set to the complemented value of the first and second input respectively, and logic 0 is applied to the input C. To obtain the exclusive OR operation, inputs A, B and C are kept as it is. To perform exclusive NOR operation, the complemented value of the first and third input is applied at input A and input C and input B is kept as it is.

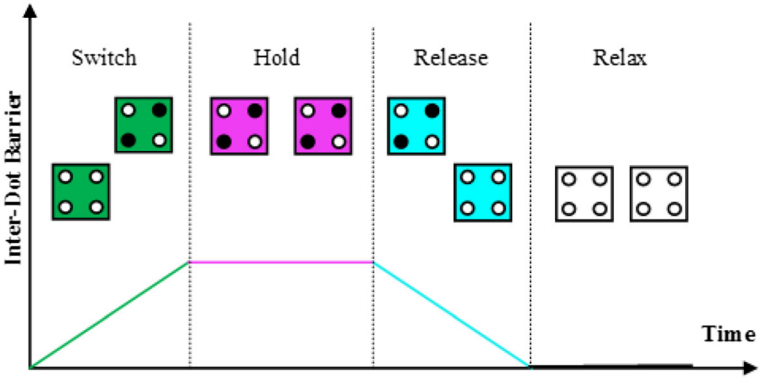


Fig. 6 Illustration of clocking and different clock phases in QCA

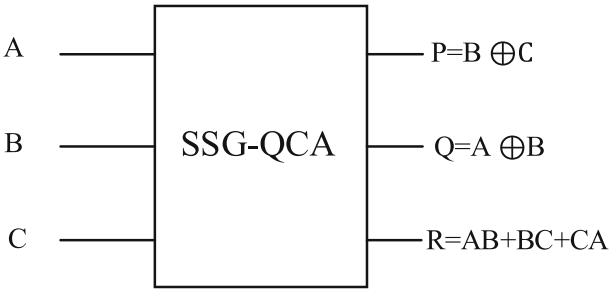


Fig. 7 Block diagram representation of proposed reversible SSG-QCA Gate

4 Hardware Complexity of SSG-QCA

Hardware complexity of a reversible gate is defined by the number of Exclusive-OR, AND and NOT operations required to realize all the outputs of the gate. The logical calculation for Ex-OR is calculated as α, for the AND operation the logical calculation is given by β and for the NOT operation it is defined by γ. In order to calculate the hardware complexity of the proposed SSG-QCA gate, equation of output 'R' has been slightly modified to include Ex-OR, AND and NOT operations while maintaining the same output combination and thus keeping the gate still reversible in nature. The equations are rewritten as,

$$P = B \oplus C \tag{3}$$

$$Q = A \oplus B \tag{4}$$

$$R = (A \oplus B)C \oplus AB \tag{5}$$

Table 3 represents the logical calculations for EX-OR, AND and NOT operations in the eqs. (3), (4) and (5) of the proposed SSG-QCA gate.

This results in the following equation for the hardware complexity of SSG-QCA. Total logical calculation is given as:

$$4\alpha + 2\beta \tag{6}$$

where α and β are the logical calculations for Ex-OR and AND operations respectively.

Table 1 Truth table of proposed SSG - QCA gate

Input encoding	Input			Output			Output encoding
	A	B	C	P	Q	R	
0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	*4*
2	0	1	0	1	1	0	*6*
3	0	1	1	0	1	1	*3*
4	1	0	0	0	1	0	*2*
5	1	0	1	1	1	1	*7*
6	1	1	0	1	0	1	5
7	1	1	1	0	0	1	1

Table 2 Implementation of Various Logic Gates Using SSG-QCA Gate

S.NO.	Logic Gate	SSG-QCA Function
1	NOT	SSG-QCA (1,B′,0)
2	AND	SSG-QCA (A,B,0)
3	NAND	SSG-QCA (A',B'1)
4	OR	SSG-QCA (A,B,1)
5	NOR	SSG-QCA (A',B′,0)
6	Ex-OR	SSG-QCA (A,B,C)
7	Ex-NOR	SSG-QCA (A',B,C')

5 Implementing 13 Standard Functions Using SSG-QCA

The effectiveness of SSG-QCA is evaluated by implementing the 13 standard logical functions. The block diagrams given in Table 4, show how the 13 standard functions can be realized by using SSG-QCA gate.

The number of gates used for the implementation of each function and the total number of gates used for the implementation of all the 13 standard functions is shown in Table 5.

6 QCA Implementation of SSG-QCA Gate Using Majority Voter Gates

The simplest implementation of the proposed 3 × 3 SSG-QCA gate in QCA can be achieved by using only the conventional 3-input majority gates shown in Fig. 5. The majority voter equations for the output of the SSG-QCA gate can be written as:

$$P = M\left[M\left(B', C, -1\right), M\left(C', B, -1\right), 1\right] \tag{7}$$

$$Q = M\left[M\left(A', B, -1\right), M\left(B', A, -1\right), 1\right] \tag{8}$$

$$R = M(A, B, C) \tag{9}$$

The block diagram representation of the above mentioned majority voter equations are given in Figs. 8, 9 and 10 respectively.

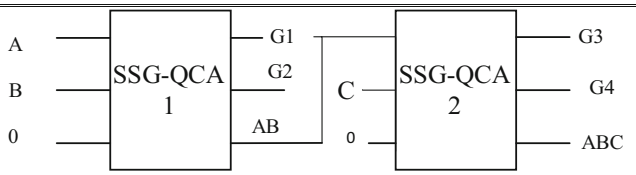
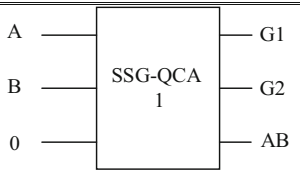
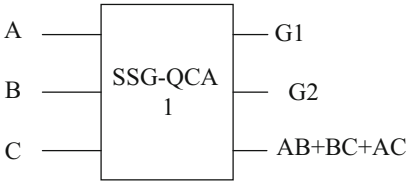
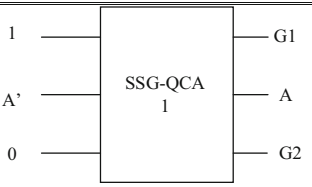
The QCA implementation of SSG-QCA and its simulation waveform are shown in Fig. 11 and Fig. 12 respectively.

This design has a higher cell count which leads to large area consumption and also the latency of the circuit is on the higher side.

Table 3 Computation of the hardware complexity of SSG-QCA Gate

OUTPUT	Number of EX-OR operations	Number of AND operations	Number of NOT operations
P	1	0	O
Q	1	0	0
R	2	2	0
TOTAL	**4**	**2**	**0**

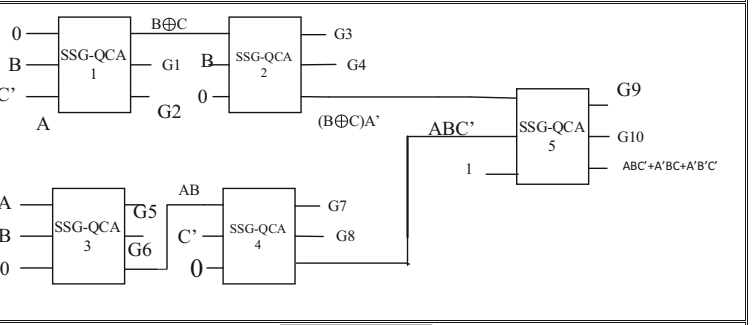
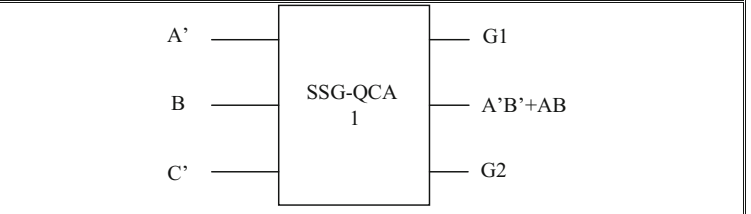
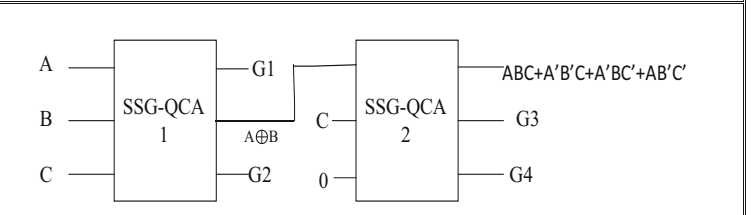
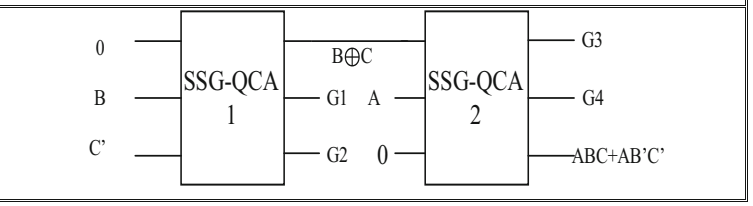
Table 4 Block Diagrams Representations of the 13 Standard Boolean Function Implemented using the Proposed SSG-QCA Gate

FUNCTIONS	BLOCK DIAGRAMS
ABC	
AB	
$AB + BC + CA$	
A	

7 Optimized QCA Design of SSG-QCA Gate

The proposed SSG-QCA gate, designed using 7 majority voter gates shown in Fig. 11, is optimized using the concept of explicit interaction of cells [3, 12, 14] which leads to an optimized design consisting of 2 ultra-efficient Ex-OR gates and 1 majority voter and no crossover. The optimized design of SSG-QCA and the simulation waveforms are shown in Figs. 13 and 14 respectively. These simulation results satisfy the truth table given in Table 1 and the condition of reversibility. The performance parameters of SSG-QCA designs using majority voter approach and explicit interaction of cells are presented in Table 6 along with the improvement achieved by the optimized design.

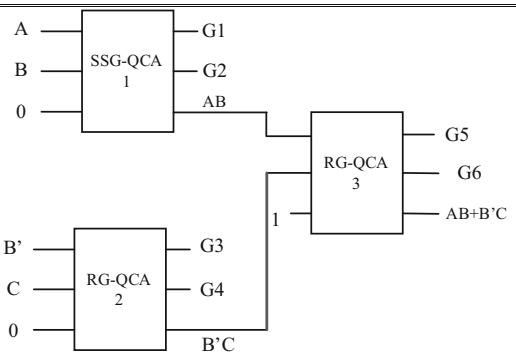
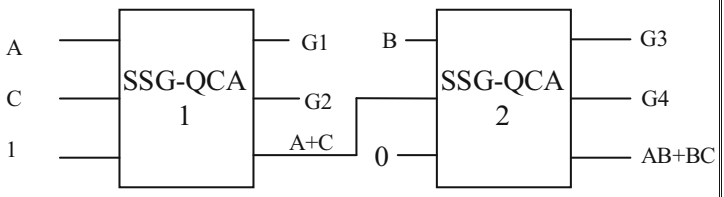
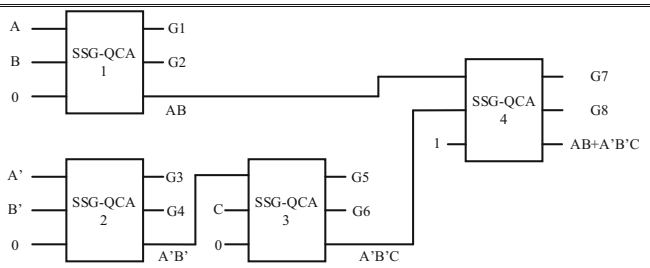
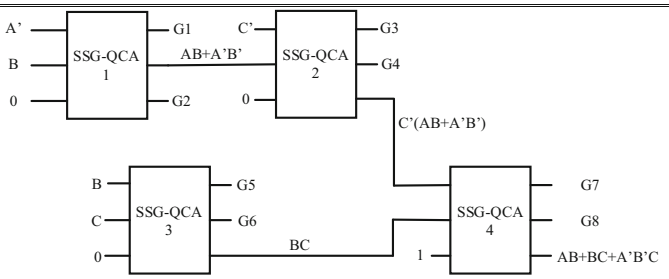
Table 4 (continued)

$A'BC + A'B'C'$	
$ABC' + A'BC + A'B'C'$	
$AB + A'B'$	
$ABC + A'B'C + A'BC' + AB'C'$	
$ABC + AB'C'$	

8 Proposed Full Adder Design Using SSG-QCA

From the extensive literature study, it is envisaged that there is need for an optimized design of adder circuits for QCA nanotechnology based applications. Adders form the core component of all the digital circuits and the overall performance of the system is highly dependent on the type, speed and performance of the adder circuits used in it. In this paper, a new reversible 1-bit full adder using the proposed SSG-QCA gate has been proposed. The new adder requires one SSG-QCA and one MFG (Modified Feynman Gate) gate for its implementation and results in

Table 4 (continued)

$AB + B'C$	
$AB + BC$	
$AB + A'B'C$	
$AB + BC + A'B'C$	

the production of three garbage outputs and doesn't require any constant input as shown in Fig. 15 along with the truth table presented in Table 7.

The explicit interaction of cell based QCA implemented design of the proposed 1-bit full adder and the simulations waveform are shown in Figs. 16 and 17 respectively.

The performance parameters of the full adder design using the proposed SSG-QCA are shown in Table 8.

Table 5 Implementation of 13 standard logic functions using SSG-QCA gate

S.No.	Function	No. of gates	Constant input	Garbage output
1	ABC	2	2	4
2	AB	1	1	2
3	AB+BC + AC	1	0	2
4	A	1	2	2
5	A'BC + A'B'C'	2	2	4
6	ABC' + A'BC + A'B'C'	5	5	10
7	AB+A'B′	1	0	2
8	A'B'C + AB'C′ + A'BC' + ABC	2	1	4
9	ABC + AB'C'	2	2	3
10	AB+B'C	3	3	6
11	AB+BC	2	2	4
12	AB+A'B'C	4	4	8
13	AB+BC + A'B'C'	4	4	8
Total		**30**	**28**	**59**

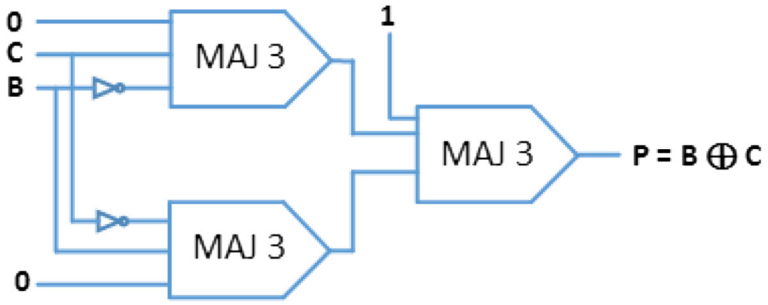


Fig. 8 Block diagram representation of output P of proposed SSG-QCA gate using majority voters

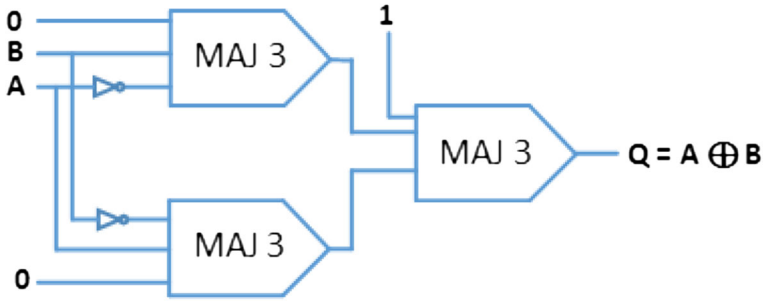


Fig. 9 Block diagram representation of output Q of proposed SSG-QCA gate using majority voters

Fig. 10 Block diagram representation of output P of proposed SSG-QCA gate using majority voters

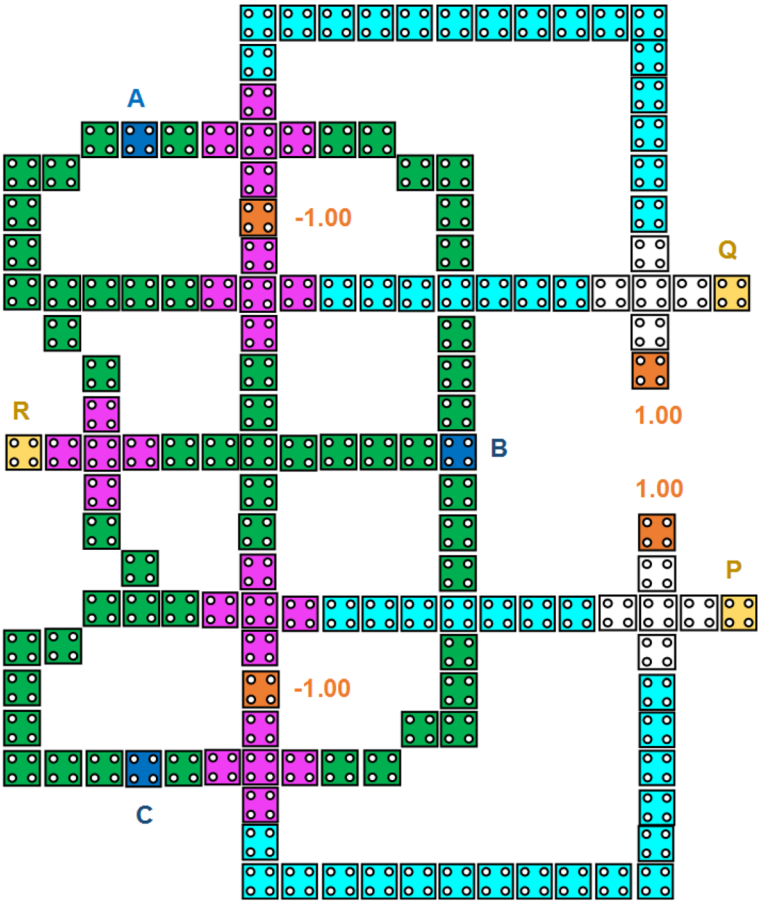


Fig. 11 QCA Implementation of proposed SSG-QCA gate using 3-input majority voter approach

9 Power Dissipation Analysis

QCAPro tool, a probabilistic modelling tool [15], has been used for energy dissipation analysis. It uses a fast approximation based technique to estimate highly erroneous cells in QCA circuit design. The leakage energy, switching energy, and the average energy dissipations, respectively, are illustrated using this tool. The power dissipation of proposed gate and adder circuits is calculated using the Hartree-Fock mean-field approach approximation which is illustrated as [15–17].

$$H = \begin{bmatrix} \frac{-E_k}{2}\sum_i C_i f_{i,j} & -\gamma \\ -\gamma & \frac{E_k}{2}\sum_i C_i f_{i,j} \end{bmatrix} = \begin{bmatrix} \frac{-E_k}{2}\left(C_{j-1} + C_{j+1}\right) & -\gamma \\ -\gamma & \frac{E_k}{2}\left(C_{j-1} + C_{j+1}\right) \end{bmatrix} \quad (10)$$

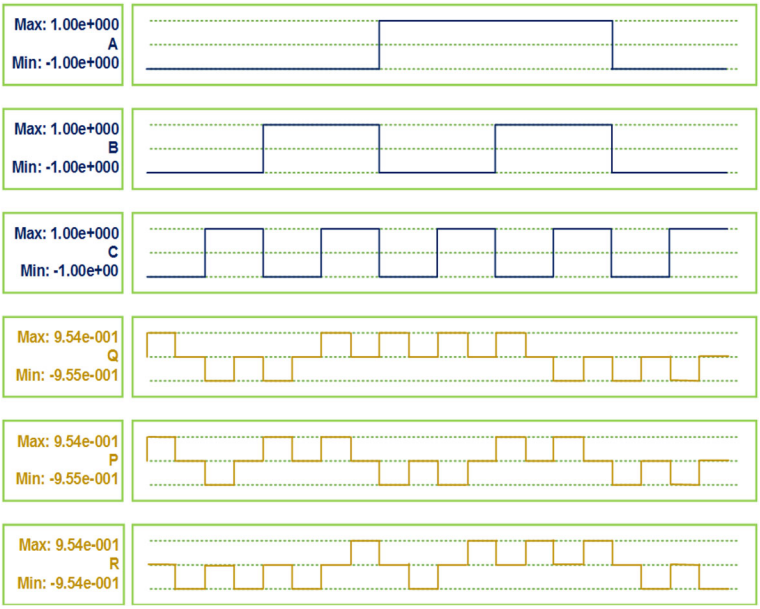


Fig. 12 Output waveform of QCA implementation of 3-input majority voter based SSG-QCA gate

According, to the upper bound power dissipation model [16], the power dissipation of a QCA cell is calculated as:

$$P_{diss} = \frac{E_{diss}}{T_{cc}} \left\langle \frac{\hbar}{2T_{cc}} \vec{\Gamma}_+ \times \left[-\frac{\vec{\Gamma}_+}{\left|\vec{\Gamma}_+\right|} \tanh\left(\frac{\hbar \left|\vec{\Gamma}_+\right|}{k_B T} \right) + \frac{\vec{\Gamma}_-}{\left|\vec{\Gamma}_-\right|} \tanh\left(\frac{\hbar \left|\vec{\Gamma}_-\right|}{k_B T} \right) \right] \right\rangle \tag{11}$$

Here, T is the temperature and k_B denotes the Boltzmann constant. In an array of similar QCA cells; total energy dissipated power (leakage" and "switching") of all identical QCA cells can be calculated using the Eq. (11) [18].

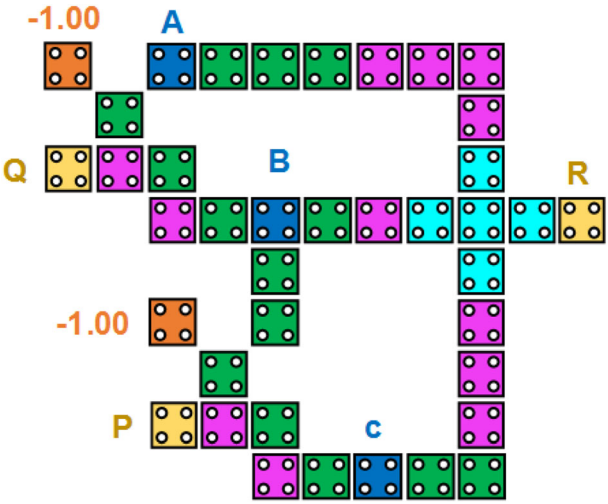


Fig. 13 QCA implementation of proposed SSG-QCA gate

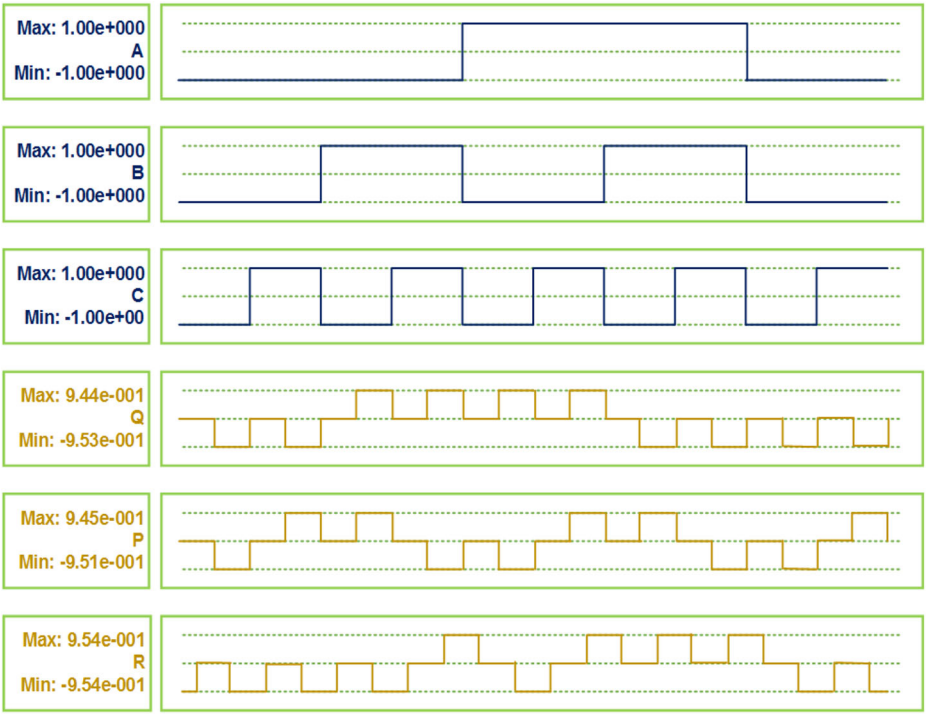


Fig. 14 Output waveform of QCA implementation of proposed SSG-QCA gate

The power dissipation map of the optimized 3 × 3 SSG-QCA gate at temperature of 2 K and tunneling energy levels of 0.5 E_k, 1 E_k, and 1.5 E_k is shown in Figs. 18, 19 and 20 respectively, whereas the power dissipation map of the proposed full adder designed using optimized 3 × 3 SSG-QCA gate at temperature of 2 K and tunneling energy levels of 0.5 E_k, 1 E_k, and 1.5 E_k is shown in Figs. 21, 22 and 23 respectively.

It is observed from the power dissipation maps that as the tunneling energy is increased from 0.5 Ek to 1.5Ek, the average switching energy dissipation of the gate and adder decreases whereas the average leakage energy dissipation increases thereby resulting in the increase in the total energy consumption. The darker cells in the power dissipation maps indicates that the cell is dissipating high energy. On the other hand, input cells do no dissipate any power and hence are depicted in white (~zero power).

Table 6 Comparison between SSG-QCA using majority voter approach and optimized SSG-QCA

Parameter	Majority Voter approach	Optimized design	%age Improvement in optimized SSG-QCA
Cell Count	148	39	73.65%
Cell Area (μm²)	0.0479	0.0126	73.65%
Total Area (μm²)	0.1757	0.0396	77.46%
Latency	1	0.75	25%
Area Delay Product	0.1757	0.0297	83.1%

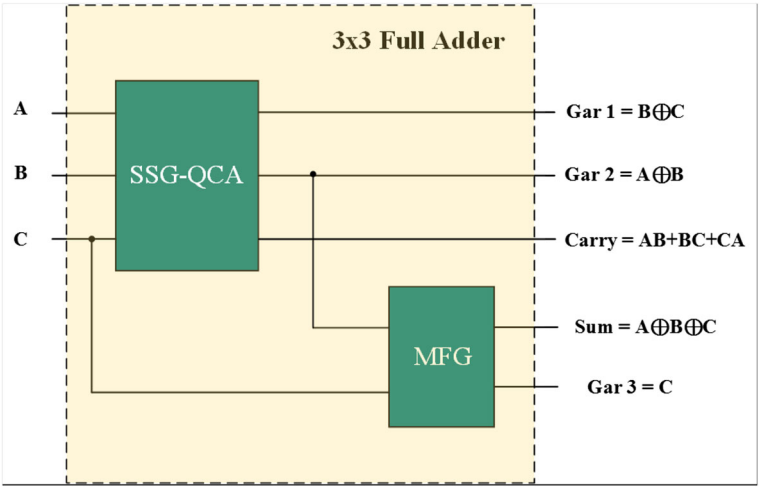


Fig. 15 Block diagram representation of full adder using proposed SSG-QCA gate

Table 7 Truth table of full adder using SSG-QCA gate

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

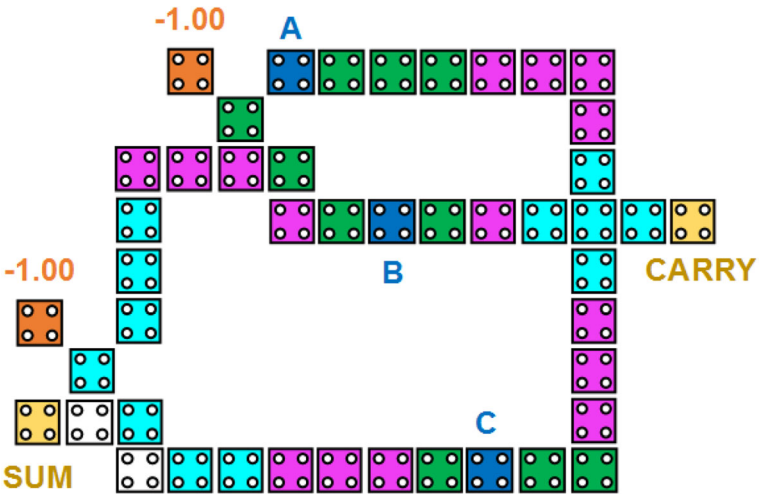


Fig. 16 QCA implementation of full adder using proposed SSG-QCA gate

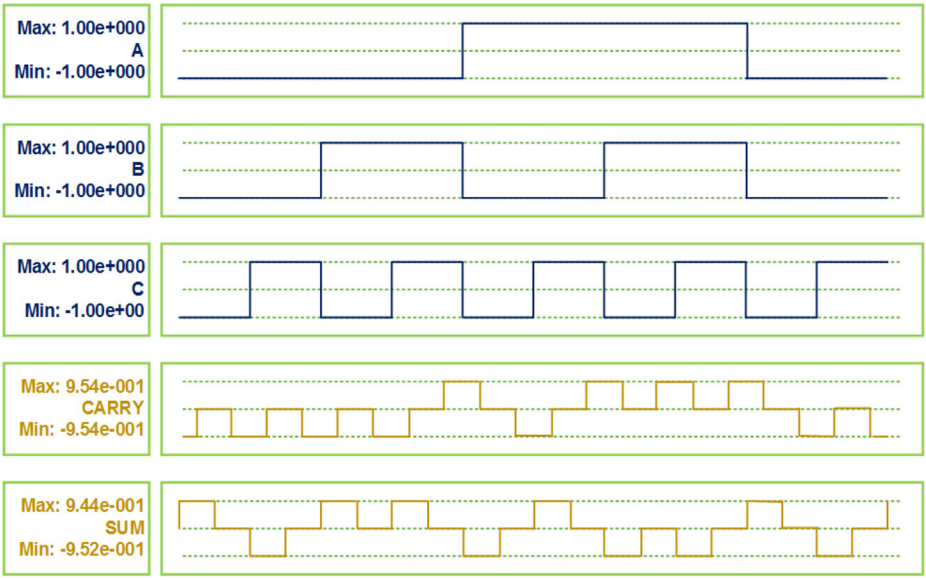


Fig. 17 Output waveform of QCA implementation of full adder using proposed SSG-QCA gate

Table 8 Performance parameters of full adder design using SSG-QCA gate

Parameters	Value
No. of cells	46
Cell area	0.0149 μm^2
Total area	0.0504 μm^2
Latency	1
Number of crossovers	0

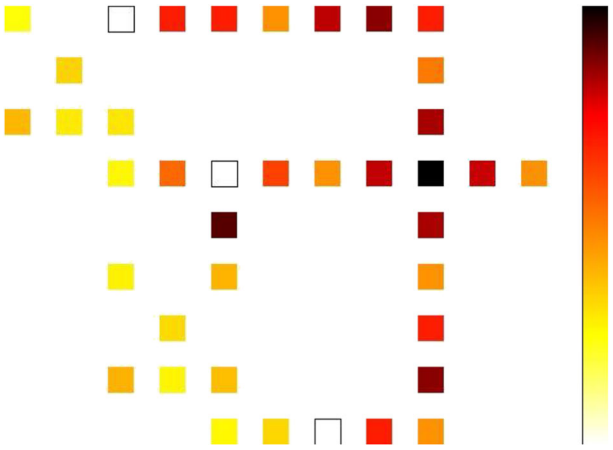


Fig. 18 Power dissipation map of the proposed SSG-QCA gate at T = 2 K temperature and 0.5 E_k tunneling energy level

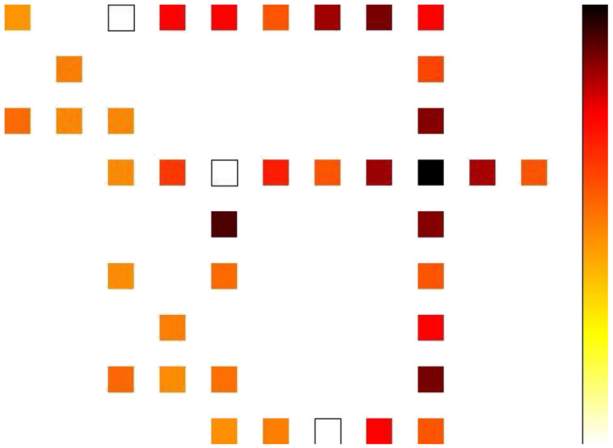


Fig. 19 Power dissipation map of the proposed SSG-QCA gate at T = 2 K temperature and 1.0 E_k tunneling energy level

10 Discussions

The efficiency of the proposed designs has been evaluated by drawing a number of comparisons with the existing designs in the literature. To begin with, a comparison of the number of gates required to implement all 13 boolean functions has been presented in Table 9 and it is observed that the proposed SSG-QCA gates requires minimum number of gates to implement all these functions.

Table 10 draws the comparisons between the existing 3 × 3 reversible gates and proposed SSG-QCA gate and it is observed that the SSG-QCA gate has the least cell count and hence lowest cell area.

The performance comparison of the full adder circuits designed using proposed 3 × 3 SSG-QCA gates with existing state-of-the-art designs is given in Table 11. It

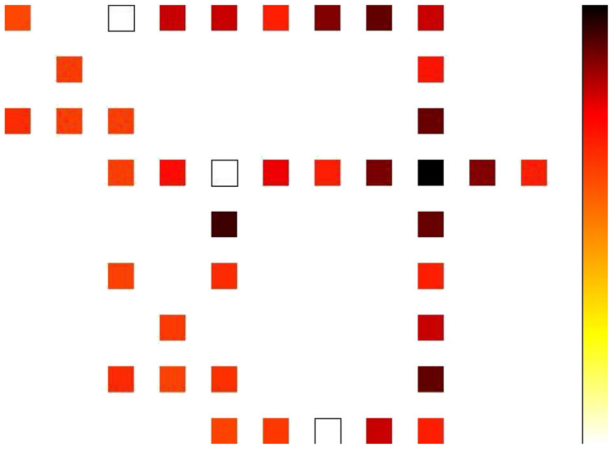


Fig. 20 Power dissipation map of the proposed SSG-QCA gate at T = 2 K temperature and 1.5 E_k tunneling energy level

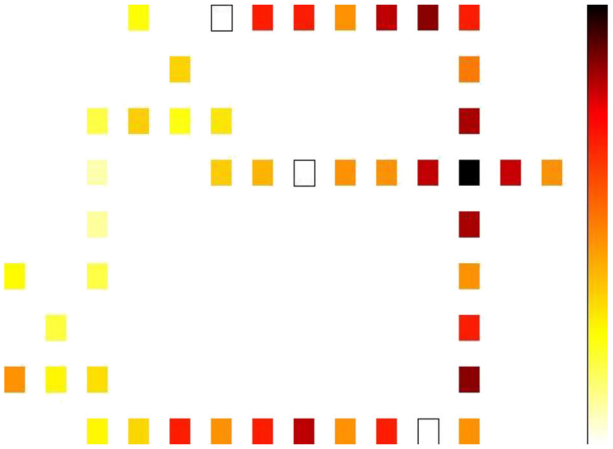


Fig. 21 Power dissipation map of the proposed reversible full adder using SSG-QCA gate at T = 2 K temperature and 0.5 E_k tunneling energy level

is seen that the proposed SSG-QCA based optimized full adder has least cell count and highest area usage. Table 12 depicts the energy dissipation analysis and comparison of the proposed 3 × 3 SSG-QCA reversible gate with other 3 × 3 reversible gates at three tunneling energy levels (0.5 E_k, 1 E_k, and 1.5 E_k) and a temperature of T = 2 K. In addition to this a comparison of energy dissipation (over all vector pairs) of the proposed full adder with other reversible full adders in the literature has been presented in Table 13. It is observed that the proposed designs have minimum average leakage and average switching energy dissipation because of the designing using 90-degree cell arrangements with 2 nm separation between cells which leads to the minimum total energy consumption of the proposed gate and adder. Figures 24, 25 and 26 present the graphical comparison of the average leakage, average switching and total energy dissipation of the full adder designed using the proposed 3 × 3 SSG-QCA gate.

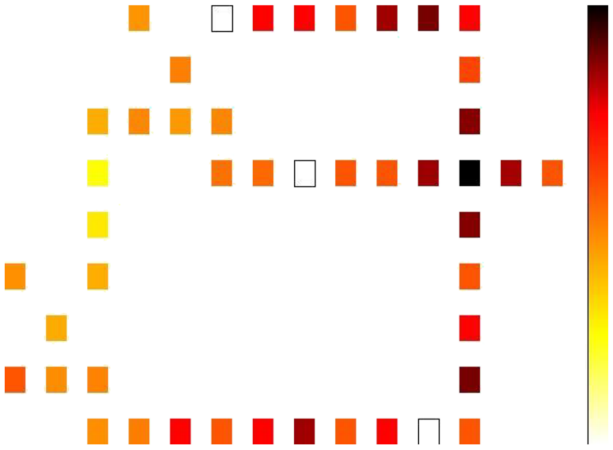


Fig. 22 Power dissipation map of the proposed reversible full adder using SSG-QCA gate at T = 2 K temperature and 1.0 E_k tunneling energy level

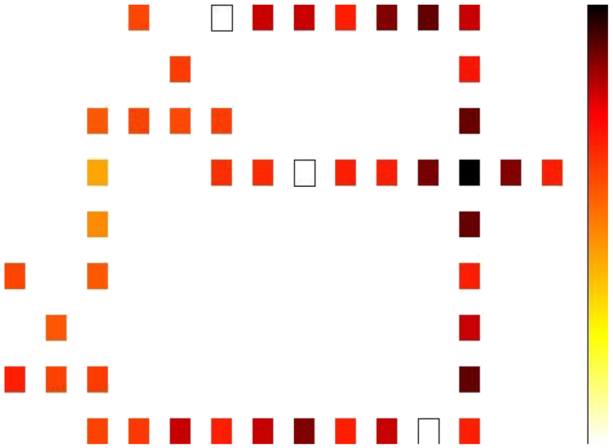


Fig. 23 Power dissipation map of the proposed reversible full adder using SSG-QCA gate at T = 2 K temperature and 1.5 E_k tunneling energy level

Hence based on the exhaustive performance evaluation and comparison of the proposed gate and adder, it is envisaged that the proposed designs are most suitable for designing of the combinational circuits with maximum efficiency.

11 Conclusion

In this paper, reversible logic and QCA as alternatives technologies are discussed to overcome the limitations that the CMOS technology is facing in the nano regime. A new 3 × 3 SSG-QCA reversible gate which has universality and multi-functionality capability, is first proposed and implemented in QCA using 3-input majority voter followed by the optimization of the gate using explicit interaction of cell which leads to an efficient design. This optimized design is

Table 9 Comparison of number of reversible gates required to implement 13 standard logic functions

S. No.	Function	CQCA [19]	Toffoli [20]	Fredkin [21]	RG-QCA [3]	RUG [22]	PROPOSED SSG-QCA
1	ABC	2	2	2	2	3	2
2	AB	1	1	1	1	1	1
3	AB+BC + AC	1	5	5	1	1	1
4	A	1	1	1	1	1	1
5	A’BC + A’B′	3	3	3	2	2	2
6	AB+A’B’	4	2	2	1	2	1
7	ABC’ + A’BC + A’B’C′	6	6	6	5	3	5
8	A’B’C + AB’C′+ A’BC’ + ABC	3	2	3	1	2	2
9	ABC + AB’C′	6	5	4	5	3	2
10	AB+B’C	3	3	1	3	3	3
11	AB+BC	2	2	2	2	3	2
12	AB+A’B’C	5	5	5	5	3	4
13	AB+BC + A’B’C′	6	5	6	5	4	4
Total		43	42	41	34	31	30

Table 10 Comparison of proposed SSG-QCA gate with existing 3 × 3 reversible gates in QCA

Parameter	Fredkin Gate [21]	RUG [22]	PPRG [23]	RQCA [24]	RM [24]	PRG [25]	RG-QCA [3]	PROPOSED SSG-QCA
N_{MG}	6	7	6	6	–	3	4	2
N_{INV}	8	2	6	4	–	–	2	0
Cell count	246	211	171	194	224	146	143	39
Cell area (μm^2)	0.079	0.068	0.055	0.062	0.072	0.047	0.046	0.0126
Total area (μm^2)	0.37	0.27	0.19	0.21	0.25	0.14	0.14	0.0396
Latency	4	3	3	3	4	5	1.75	0.75
Area delay product	1.48	0.81	0.57	0.63	1.0	0.7	0.245	0.0297
Area usage (%)	21.35	25.18	28.94	29.52	28.8	33.57	32.85	31.9

Table 11 Comparison of reversible full adder circuit designs in QCA

Parameter	Fredkin Gate [21]	RUG [22]	QCA 1 [26]	PPRG [23]	RQCA [24]	PRG [25]	RG-QCA [3]	PROPOSED SSG-QCA
Gate count	5	3	3	3	3	3	2	2
Cell count	955	594	438	513	582	562	375	46
Cell area (μm^2)	0.309	0.1924	0.1419	0.166	0.188	0.182	0.1215	0.0149
Total area (μm^2)	1.85	0.92	0.48	0.57	–	0.70	0.37	0.0504
Area usage (%)	16.7	20.91	29.56	29.12	–	26.012	32.83	29.57

Table 12 Energy consumption analysis of proposed 3 × 3 SSG-QCA gate

	Avg. leakage energy dissipation (eV)			Avg. switching energy dissipation (eV)			Total Energy Consumption (eV)		
Structure design	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek
RM [24]	0.117	0.318	0.534	0.309	0.251	0.205	0.426	0.569	0.739
Fredkin [21]	0.101	0.283	0.482	0.213	0.175	0.143	0.314	0.458	0.625
PRG [25]	0.042	0.131	0.237	0.227	0.197	0.168	0.269	0.328	0.405
Proposed design	0.0145	0.0396	0.0672	0.0419	0.0349	0.0289	0.0565	0.0745	0.0961

Table 13 Energy consumption analysis of proposed reversible full adder using SSG-QCA gate

	Avg. leakage energy dissipation (eV)			Avg. switching energy dissipation (eV)			Total energy consumption (eV)		
Design	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek
RM [24]	0.351	0.954	1.602	0.927	0.753	0.615	1.278	1.707	2.217
FG + RQCA [27]	0.202	0.566	0.964	0.426	0.35	0.286	0.628	0.916	1.25
QCA2 [28]	0.093	0.241	0.475	0.348	0.301	0.292	0.441	0.542	0.767
QCA1 [26]	0.085	0.235	0.452	0.342	0.285	0.259	0.427	0.52	0.711
RQG [29]	0.068	0.209	0.376	0.269	0.236	0.203	0.337	0.445	0.579
Proposed Design	0.017	0.047	0.0801	0.0448	0.0372	0.0306	0.0619	0.0842	0.1107

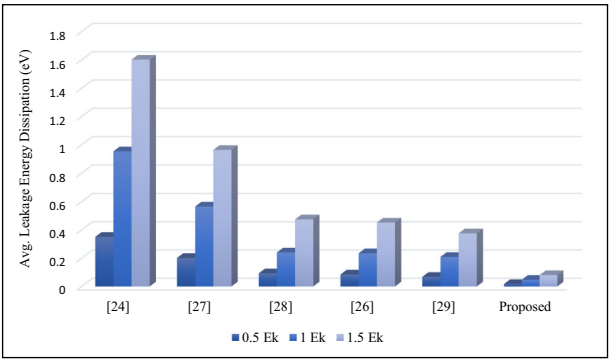


Fig. 24 Comparison of Average Leakage Energy Dissipation (eV) of proposed reversible full adder circuit

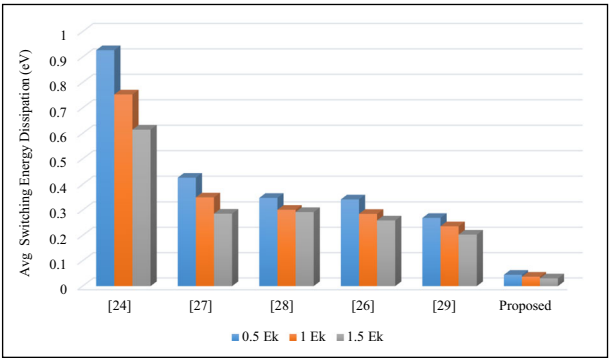


Fig. 25 Comparison of Average Switching Energy Dissipation (eV) of proposed reversible full adder circuit

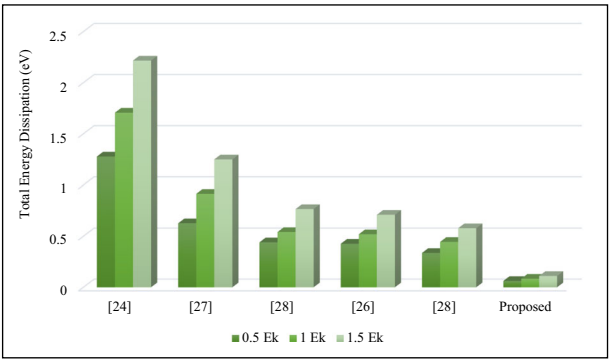


Fig. 26 Comparison of Total Energy Dissipation (eV) of proposed reversible full adder circuit

then used to design a reversible full adder circuit, which is the prime component of maximum digital circuits, in QCA. Exhaustive comparisons of the optimized proposed gate and full adder are drawn with the existing designs in the literature. It is envisaged that the proposed designs outperform the existing ones in terms of all the QCA parameters. In addition to this energy dissipation analysis for different scenarios is also done on all the designs and it is observed that the proposed designs dissipate minimum energy thereby making them suitable for ultra-low power designs.

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