International Journal of Theoretical Physics (2019) 58:2677–2691
https://doi.org/10.1007/s10773-019-04158-9

Design of Novel Coplanar Counter Circuit in Quantum Dot Cellular Automata Technology

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Received: 10 January 2019 / Accepted: 14 May 2019 / Published online: 3 June 2019

Abstract
One of the emerging technology that can be used for replacing CMOS technology is Quantum-dot Cellular Automata (QCA) technology. Counter circuits are widely used circuits in the design of digital circuits. This paper presents and evaluates circuits for 2-, 3-, 4-, and 5-bit coplanar counter in the QCA technology. The designed QCA coplanar counter circuits are based on the modified D-Flip-Flop (D-FF) circuit that is designed in this paper. The designed QCA circuits are implemented and verified by using QCADesigner tool version 2.0.3. The results show that the designed circuits for 2-, 3-, 4-, and 5-bit coplanar counter contain 44 (0.03 μm^2), 93 (0.07 μm^2), 160 (0.13 μm^2), and 245 (0.2 μm^2) quantum cells (area). The comparison results indicate that the designed circuits have advantages compared to other QCA circuits in terms of cost, area, and cell count.

Keywords Nanoelectronics · Digital electronics · Counters · D-Flip-Flop (D-FF) · Quantum-dot Cellular Automata (QCA)

1 Introduction

The typical technologies such as CMOS technology are faced with serious challenges such as short cannel effect [1, 2] and high fault tolerance at nano-scale [3]. Carbon-Nano-Tube Field Effect Transistors (CNTFETs), Spintronics, Silicon On Insulator (SOI) MOSFET and

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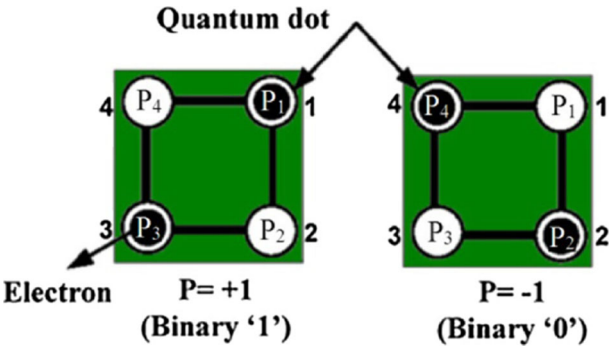

Fig. 1 A simplified QCA cell [24, 38]

Quantum-dot Cellular Automata (QCA) are considered as replaced technologies [3–14]. The QCA technology is an emerging technology designed as an appropriate alternative to CMOS technology [7].

In the QCA technology, data is transmitted through polarization based on binary information encoding in quantum dot cells [9]. In recent years, many arithmetic circuits such as counter circuits [15–23], flip-flop circuits [15, 17–19, 22, 23], shift register circuits [24], full-adder circuits [25–31], multiplexer circuits [32, 33], switched network circuits [34], number generator circuits [35] and Cellular comparator circuits [36, 37] have been designed in the QCA technology.

One of the most used circuits in arithmetic circuits is the counter circuit. Kong et al. [15] have developed a 5-bit QCA counter circuit. This designed QCA counter circuit consists of 490 cells and 0.7992 μm^2area.The authors of [16] have designed a 3-bit QCA counter circuit. This designed QCA counter circuit consists of 238 cells and 0.36 μm^2 area. Aghababa et al. [17] have designed a 4-bit QCA counter circuit that consists of 232 cells and 0.20 μm^2 area. Sarmadi et al. [18] have developed a 4-bit QCA counter circuit. This designed QCA counter circuit consists of 183 cells and 0.24 μm^2 area. Angizi et al. [19] have presented a 4-bit QCA counter circuit, which consists of 422 cells and 0.46 μm^2 area. Sheikhfaal et al. [20] have designed a 3-bit QCA counter circuit. This designed QCA counter circuit consists of 428 cells and 0.48 μm^2 area. Sangsefidi et al. [21] have proposed a 4-bit QCA counter circuit. This designed QCA counter circuit consists of 273 cells and 0.26 μm^2 area. Abutaleb [22] has designed a 3-bit QCA counter circuit. This designed QCA counter circuit consists of 196 cells and 0.22 μm^2 area. Yang et al. [23] have designed a 3-bit QCA counter circuit. This designed QCA counter circuit consists of 616 cells and 1.2 μm^2 area.

A common method to design a QCA counter circuit is mapping the circuits from CMOS technology to the QCA technology. Developing a building block circuit based on the QCA Flip-Flops (FFs) plays an important role in this method [19].

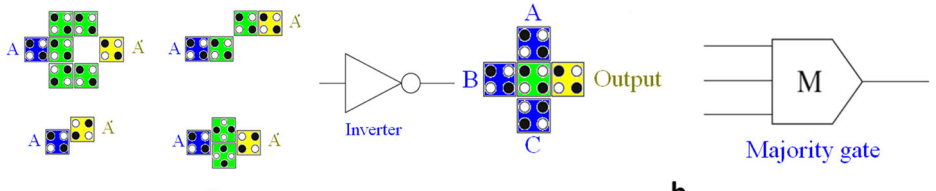

Fig. 2 The basic gates in the QCA technology: **a** inverter gates, **b** three-input majority gate [9, 39, 40]

Table 1 The truth table for the D-FF [42]

Clock pulse	Input	Output
1	0	0
1	1	1

In this paper, new circuits are designed for implementation of 2-, 3-, 4- and 5-bit QCA counter circuits. First, an efficient modified D-FF circuit is designed and then the 2-, 3-, 4- and 5-bit QCA counter circuits are designed using this modified D-FF circuit as building block. The designed counters are implemented in one layer. The functionality of the designed circuits are verified using QCADesigner tool version 2.0.3.The simulation results indicate that the designed modified D-FF circuit consists of 13 quantum cells and 0.01 μm^2 area. The 2-, 3-, 4-,

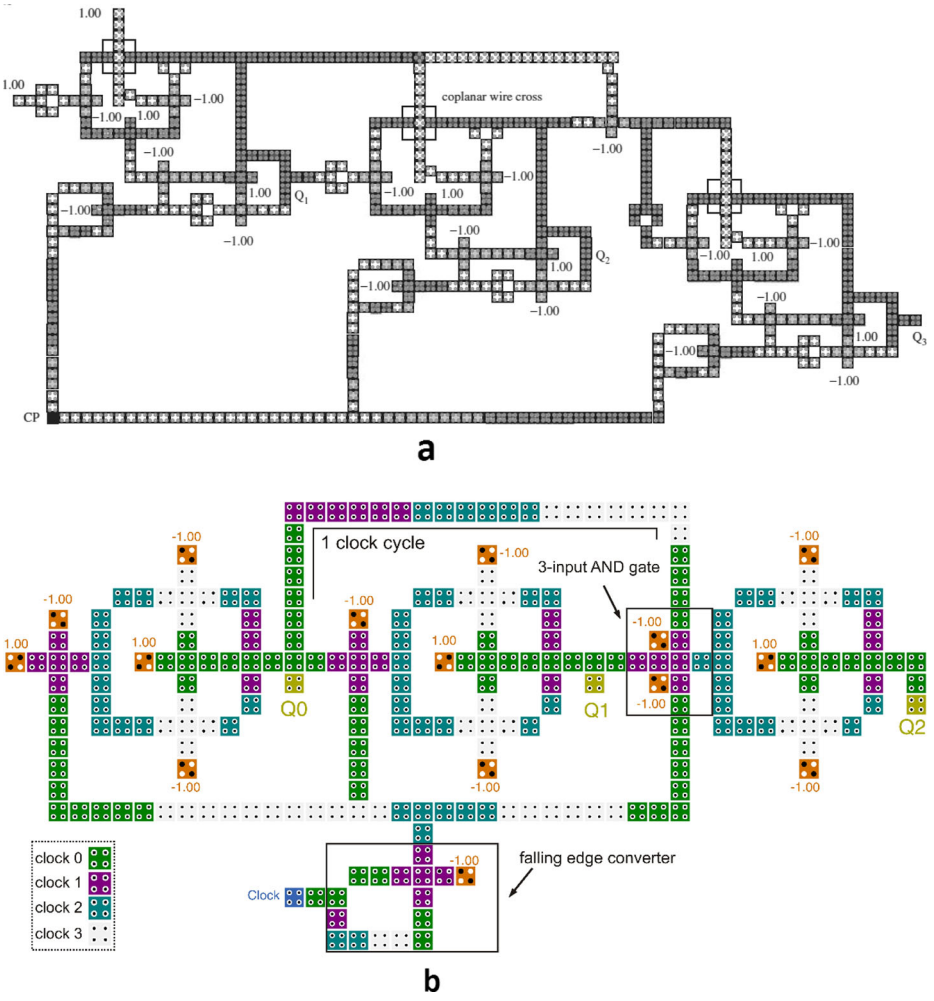

Fig. 3 The utilized QCA circuit for **a** 3-bit counter in [23], **b** 3-bit counter in [16], **c** 4-bit counter in [17], **d** 4-bit counter in [18], **e** 4-bit counter in [19], **f** 4-bit counter in [21], **g** 3-bit counter in [22], **h** 5-bit counter in [15]

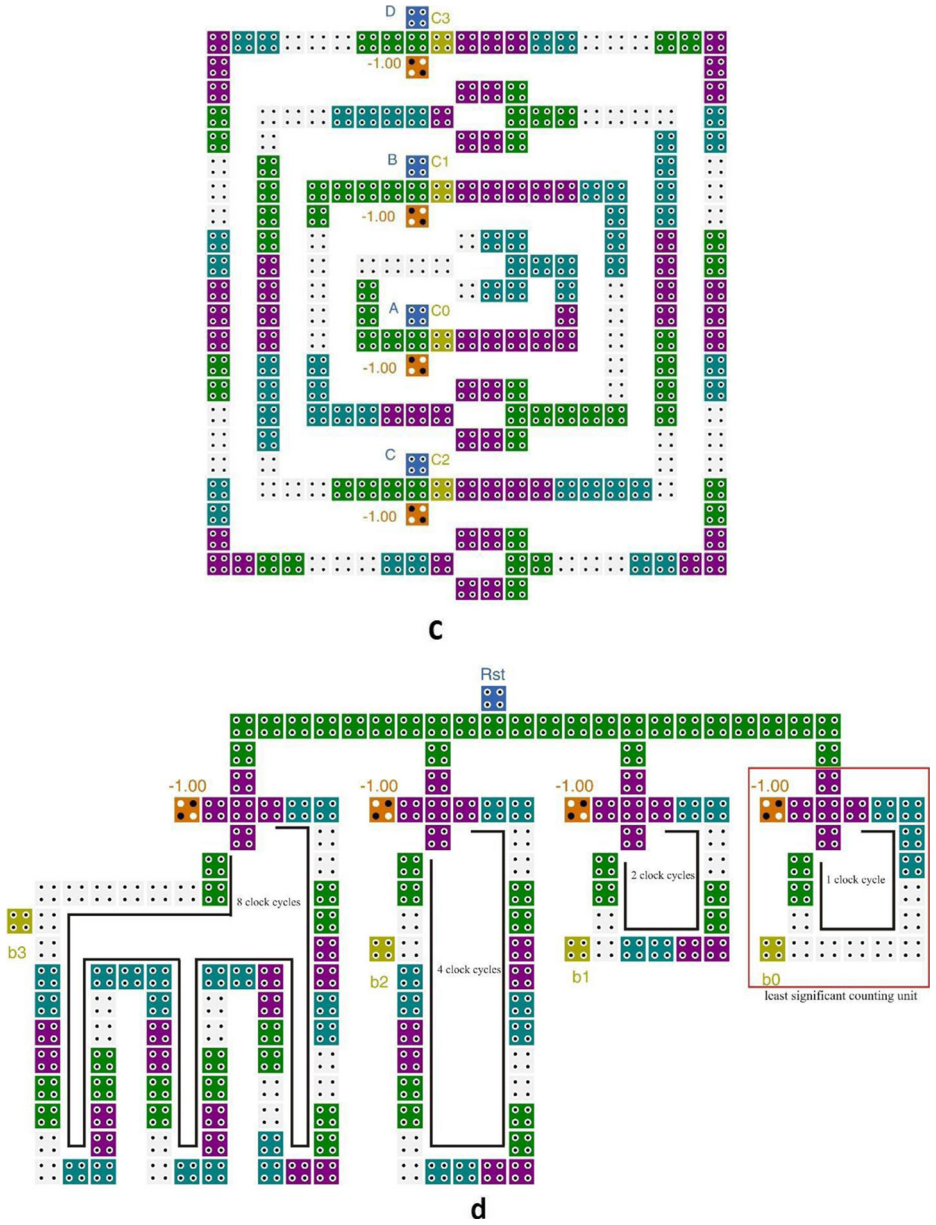

Fig. 3 continued.

and 5-bit QCA counter circuits contain 44 (0.03 μm^2), 93 (0.07 μm^2), 160 (0.13 μm^2), and 245 (0.2 μm^2) quantum cells (area). The comparison indicate that the designed circuits for the QCA counter have better performance compared to other QCA counter circuits in terms of cell count and area.

The rest of the paper is as follows: Section 2 provides a background of the QCA technology. Section 3 provides a general overview of the D-FF circuits and counter

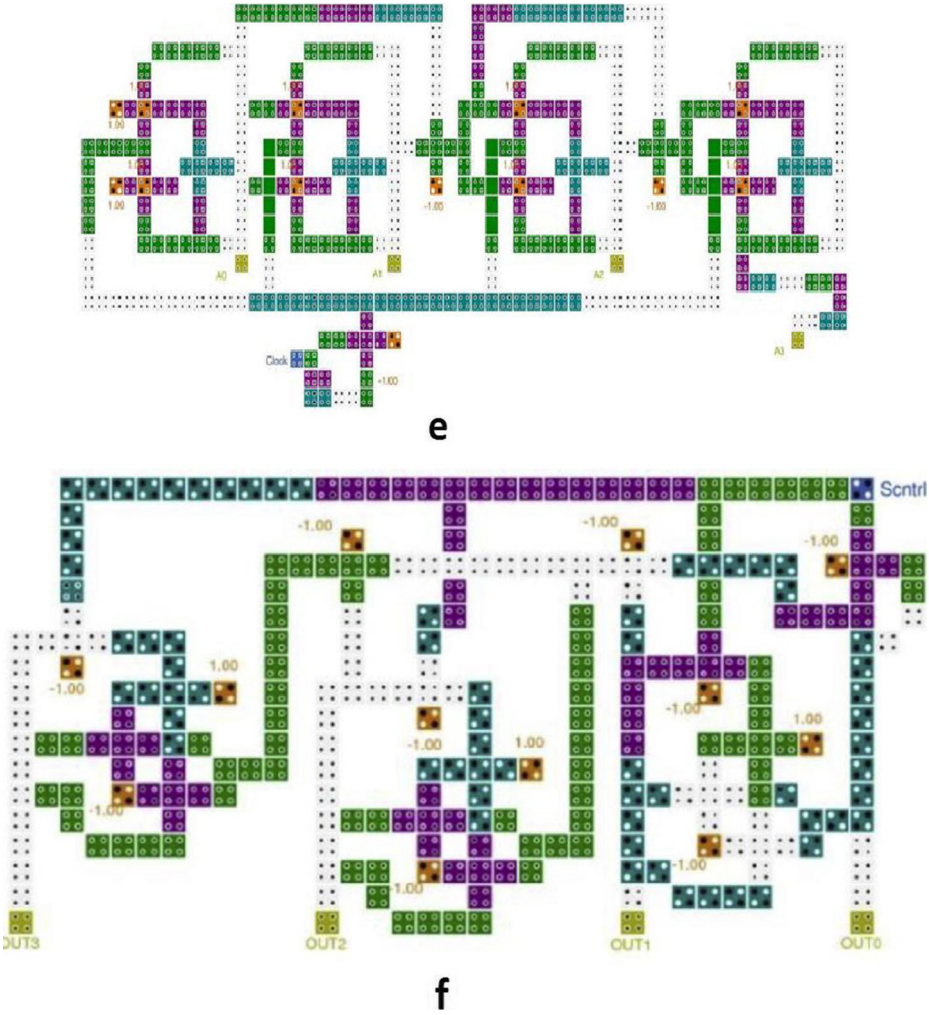

Fig. 3 continued.

circuits in the QCA technology. In section 4, the designed circuits are presented. In section 5, the implementation results of the designed circuits are presented and evaluated. Finally, the paper is concluded in section 6.

2 Background

2.1 Cells in the QCA Technology

Cells in the QCA technology include four cavities located in the square corners. These cells have two electrons, which can freely move in the cavities and create two stable states [38].

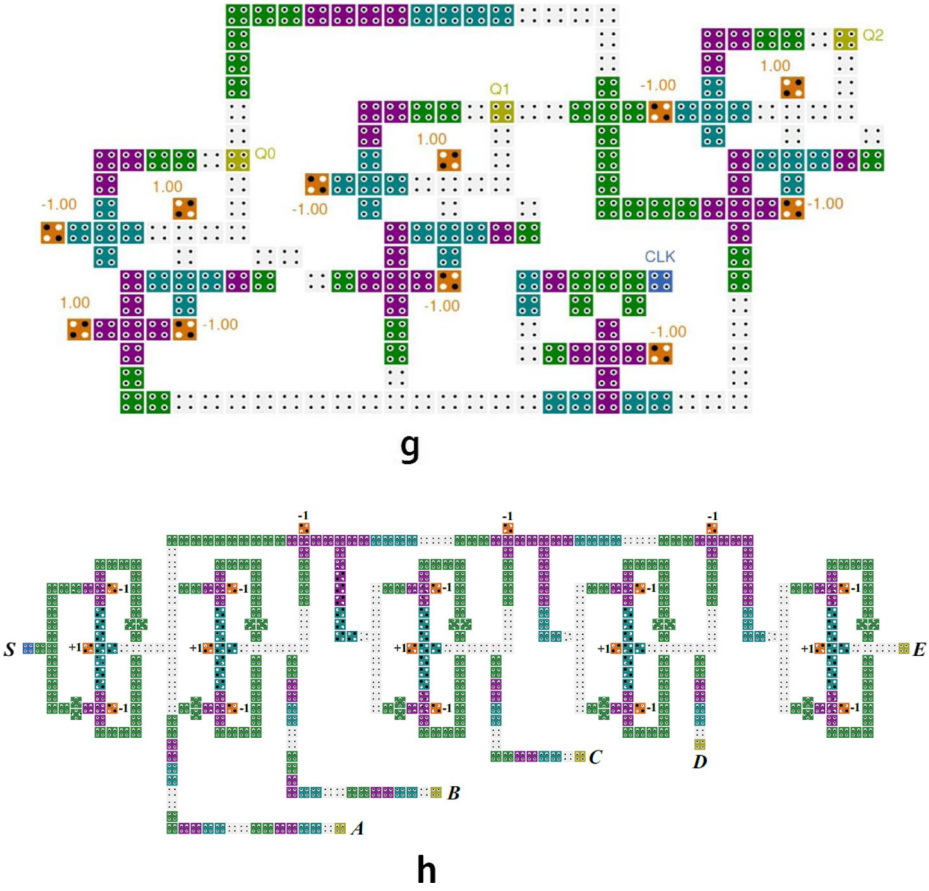

Fig. 3 continued.

These electrons are arranged in the diagonal manner. As a result, two poles of +1 (logic "1") and − 1 (logic "0") are created. Figure 1 shows these two stable states [24, 38].

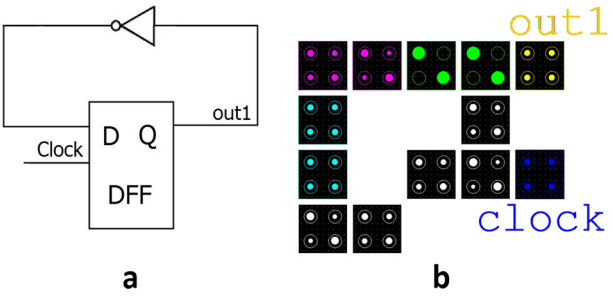

Fig. 4 The designed modified D-FF circuit **a** schematic design, **b** QCA layout

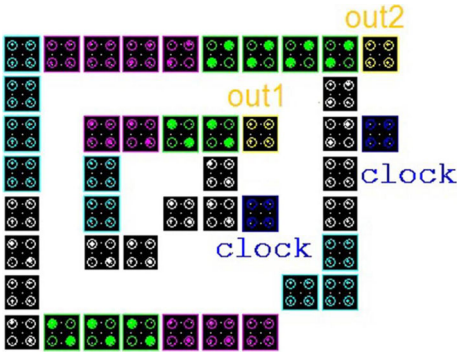

Fig. 5 The designed circuit for 2-bit QCA counter

Polarization of the cells is calculated as follows [16, 38]:

$$P = \frac{(P1 + P3) - (P2 + P4)}{P1 + P2 + P3 + P4} \tag{1}$$

Where Pi denotes the electric charge at ith point. Binary information is displayed using these electrons position in logical cells [9].

2.2 Gates in the QCA Technology

The basic QCA logic gates include the inverter gate and majority gate. Several types of inverter and majority gates are shown in Fig. 2 [9, 39, 40].

The output of the inverter gate is the inverse of the input [9, 24]. In addition, the three-input majority gate consists of at least five QCA cells [9, 39–41]. The output of the three-input majority gate is computed as follows [24]:

$$\mathrm{M}(\mathrm{A}, \mathrm{B}, \mathrm{C}) = \mathrm{AB} + \mathrm{CA} + \mathrm{CB} \tag{2}$$

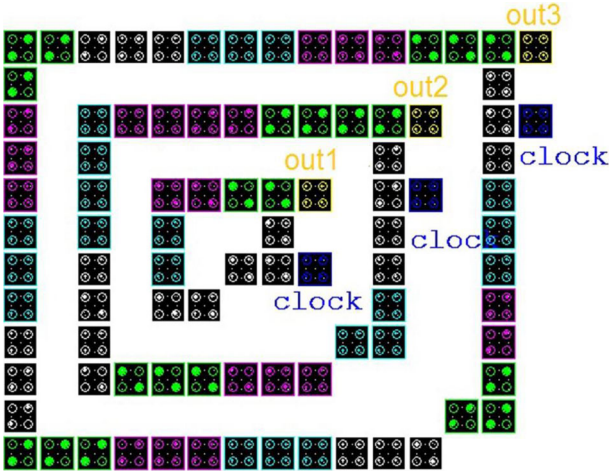

Fig. 6 The designed circuit for 3-bit QCA counter

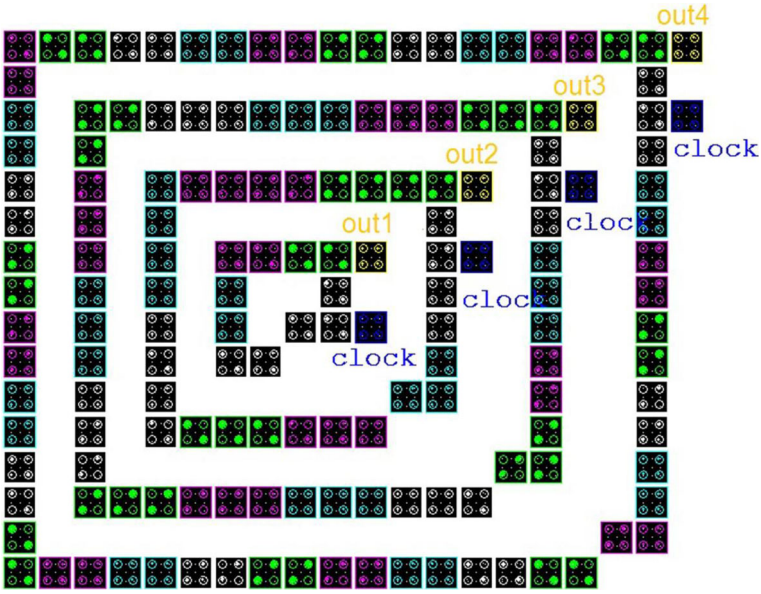

Fig. 7 The designed circuit for 4-bit QCA counter

3 Flip-Flop and Counter

3.1 Flip-Flop

The sequential circuits, which have two stable states output and can store at least one bit, are called flip-flops. Flip-flops can be categorized in 4 groups: T-FF, JK-FF, RS-FF and D-FF [35].

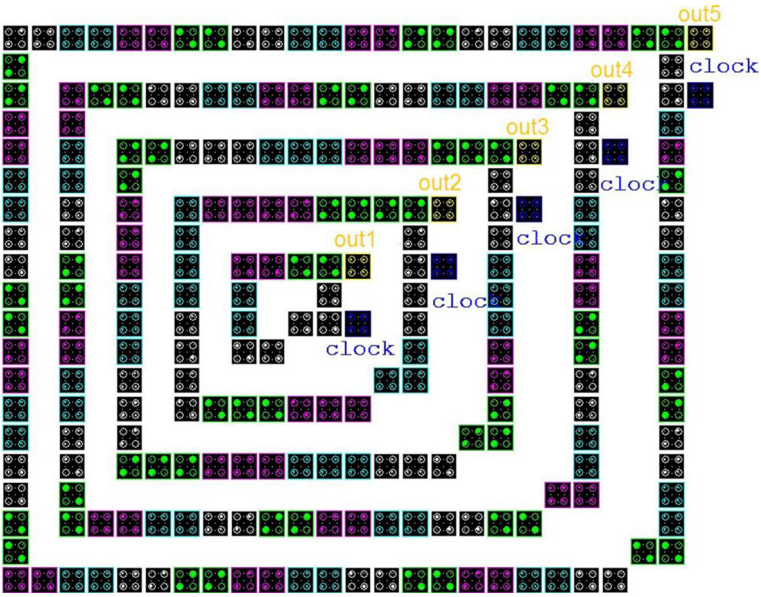

Fig. 8 The designed circuit for 5-bit QCA counter

Table 2 The utilized parameters for the simulation

Parameter	Value	Unit
Radius of Effect	65.00	Nm
Relative Permittivity	12.9000	
Clock High	9.800e-022	J
Clock Low	3.800e-23	J
Layer Separation	11.5000	Nm
Temperature	1–15	°K
Relaxation Time	1.000e-015	S
Time Step	1.000e-016	S
Total Simulation Time	7.000e-011	S

The D-FF is used as a register cell. It is because the D-FF can save its input data and shows this data in output after each clock cycle. The truth table for the D-FF is illustrated in Table 1 [42].

It should be noted that if the inverse of the D-FF output is used as the D-FF input, it can be used as a semi-oscillator circuit [17].

3.2 Counter

The counters are a class of sequential logics that are implemented using register-type circuits such as Flip-Flops. Counters can be categorized in several groups such as: asynchronous (ripple) counters, synchronous counters, cascaded counters and modulus counters [17]. The counter circuit plays an important role in the arithmetic circuits. As a result, several attempts have been done to implement efficient counter circuits especially in the QCA technology, which will be considered in the next section.

3.3 Previous QCA Counter Circuits

Figure 3 shows the previous designed counter [15–19, 21–23].

Yang et al. [23] have proposed a 3-bit synchronous counter that is illustrated in Fig. 3a. This designed counter consists of 616 cells and 1.2 μm^2 area. The authors of [16] have designed 3-bit synchronous counter, which is illustrated in Fig. 3b. This design consists of 238 cells and 0.36 μm^2 area. Aghababa et al. [17] have developed a 4-bit counter that is illustrated in Fig. 3c. This designed counter consists of 232 cells and 0.20 μm^2 area. Sarmadi et al. [18] have presented a 4-bit QCA counter, which is shown in Fig. 3d. This designed counter consists of 183 cells and 0.24 μm^2 area. Angizi et al. [19] have presented a 4-bit counter that is illustrated in Fig. 3e. This designed counter consists of 422 cells and 0.46 μm^2 area. Sangsefidi et al. [21] have developed 4-bit QCA synchronous counter, which is illustrated in Fig. 3f. This counter

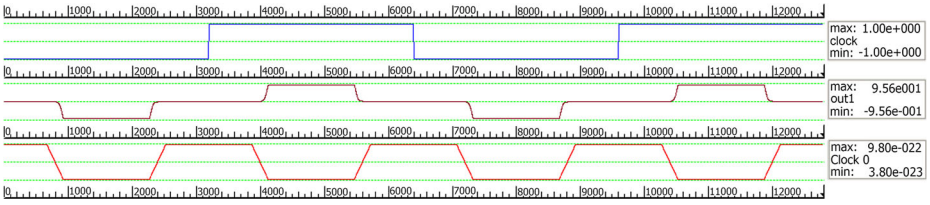

Fig. 9 The simulation results of the modified D-FF circuit

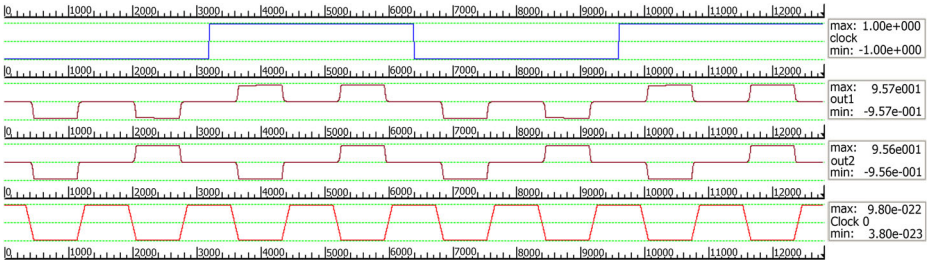

Fig. 10 The simulation results of the designed 2-bit QCA counter circuit

consists of 273 cells and 0.26 μm^2 area. The author of [22] have designed a 3-bit cascading three level-sensitive D-FFs, which is illustrated in Fig. 3g. This design consists of 196 cells and 0.22 μm^2 area. Kong et al. [15] have developed a 5-bit QCA counter that is illustrated in Fig. 3h. This designed counter consists of 490 cells and 0.7992 μm^2 area.

4 The Designed Circuits

In this section, we propose novel QCA circuits for the counter. The designed QCA counter circuits are based on the modified D-FF circuit that is developed in this paper.

4.1 The Modified D-FF Circuit

Figure 4 shows the designed modified D-FF circuit.

The designed modified D-FF circuit has an input and an output, which are shown by clock and out1, respectively. The designed circuit is composed of a new D-FF in which the inverse of the D-FF output is utilized as D-FF input. It contains 13 quantum cells and 0.01 μm^2 area. This modified D-FF circuit is used as the building block for design of QCA counter circuits.

4.2 The Designed Counter Circuit

Figure 5 shows the designed circuit for 2-bit QCA counter.

The designed 2-bit QCA counter circuit has clock input and two outputs, out1 and out2. The designed circuit for the 2-bit QCA counter has 44 quantum cells and 0.03 μm^2 area.

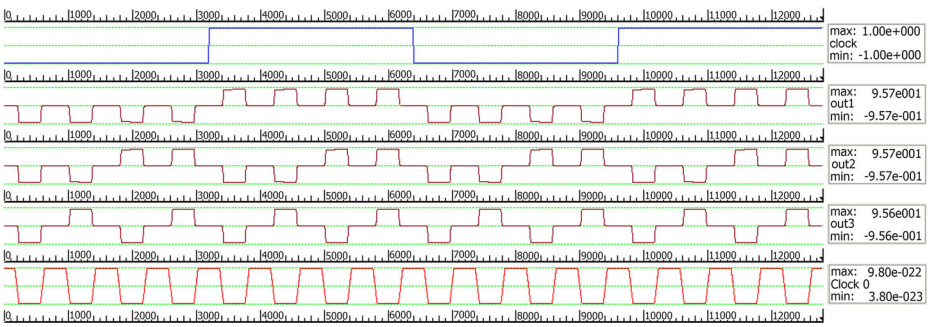

Fig. 11 The simulation results of the designed 3-bit QCA counter circuit

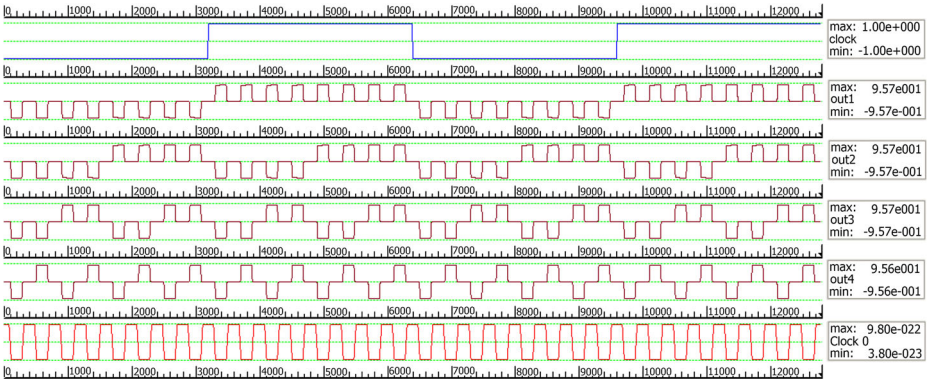

Fig. 12 The simulation results of the designed 4-bit QCA counter circuit

It should be noted that this counter can be easily extended to n-bit QCA counter. Figures 6, 7 and 8 shows the designed circuits for 3-, 4-, and 5-bit QCA counter based on designed modified D-FF circuit, respectively. These designed circuits have clock input and n outputs, out1, out2, out3, …, and outn corresponding to the n-bit counter circuits.

The designed circuits for the 3-, 4-, and 5-bit QCA counter have 93 (0.07 μm^2), 160 (0.13 μm^2) and 245 (0.20 μm^2) quantum cells (area), respectively.

5 The Simulation Results and Comparison

The QCADesigner tool version 2.0.3 is used to verify the functionality of the designed QCA circuits. The utilized parameters for the simulation is shown in Table 2.

5.1 The Modified D-FF Circuit

Figure 9 shows the simulation results of the modified D-FF circuit.

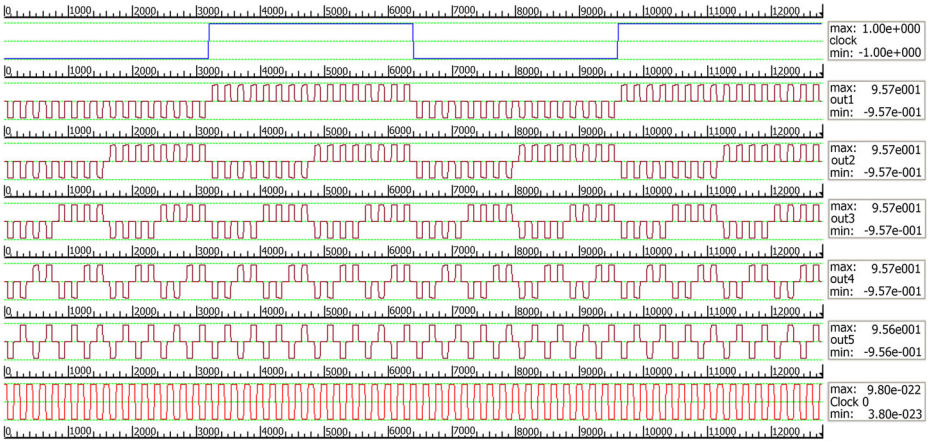

Fig. 13 The simulation results of the designed 5-bit QCA counter circuit

Table 3 Comparison table for the QCA counter circuits

Ref.		[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	This paper
	Layer	Coplanar	Coplanar	Coplanar	Multi-layer	Coplanar	Coplanar	Coplanar	Coplanar	Coplanar	Coplanar
2-bit counter	Cell count	328	–	78	240	169	–	–	141	112	44
	area (μm^2)	0.62	–	0.06	0.26	0.17	–	–	0.22	0.13	0.03
	Delay (clock cycle)	3	–	1	2	2	–	–	2.25	2	2
	Cost	1.86	–	0.06	0.52	0.34	–	–	0.495	0.26	0.06
3-bit counter	Cell count	616	196	171	428	287	–	–	238	273	93
	area (μm^2)	1.2	0.22	0.16	0.48	0.33	–	–	0.36	0.33	0.07
	Delay (clock cycle)	5	2	3	2	2	–	–	2.25	2	4
	Cost	6	0.44	0.48	0.96	0.66	–	–	0.81	0.66	0.28
4-bit counter	Cell count	1130	–	273	652	422	183	232	354	488	160
	area (μm^2)	2.2	–	0.26	0.74	0.46	0.24	0.20	0.49	0.54	0.13
	Delay (clock cycle)	7	–	4	2	2	8	8	2.25	3	8
	Cost	15.4	–	1.04	1.48	0.92	1.92	1.6	1.1025	1.62	1.04
5-bit counter	Cell count	–	–	–	–	–	–	–	–	490	245
	area (μm^2)	–	–	–	–	–	–	–	–	0.7992	0.20
	Delay (clock cycle)	–	–	–	–	–	–	–	–	8	11
	Cost	–	–	–	–	–	–	–	–	6.3936	2.2

Figures 10, 11, 12 and 13 show the simulation results of the designed 2-, 3-, 4-, and 5-bit QCA counter circuits.

The simulation results indicate that the outputs of the designed QCA counter circuits are correctly obtained. Table 3 shows the simulation results of the designed QCA counter circuits compared with other counter circuits in [15–23]. The cost is computed using Eq. (3) [30]:

$$\text{Cost} = \text{Area}\left(\mu m^2\right) \times \text{Delay}(\text{Cycle cycle}) \tag{3}$$

Based on the simulation results that are summarized in Table 3, the cell count, area and cost of the designed 2-bit QCA counter circuit are considerably improved compared to 2-bit QCA counter circuits in [15, 16, 19–23]. The only 2-bit QCA counter circuit that has the same cost compared to the developed 2-bit QCA counter circuit is the 2-bit QCA counter circuit in [21]. However, the area and cell count in this circuit are about 2 and 1.7 times bigger than the designed 2-bit QCA counter circuit.

Moreover, the cost, cell count, and area of the designed 3-bit QCA counter circuit are considerably improved compared to 3-bit QCA counter circuits in [15, 16, 19–23].

In addition, the cell count, area and cost of the designed 4-bit QCA counter circuit are considerably improved compared to 4-bit QCA counter circuits in [15–21, 23]. The only 4-bit QCA counter circuit that has a slightly better cost than the designed 4-bit QCA counter circuit is the 4-bit QCA counter circuit of [19]. However, the area and cell count in this circuit are about 3.5 and 2.6 times bigger than the designed 4-bit QCA counter circuit. In addition, the only 4-bit QCA counter circuit that has the same cost compared to the designed 4-bit QCA counter circuit is the 4-bit QCA counter circuit in [21]. However, the area and cell count in this circuit are about 2 and 1.7 times bigger than the designed 4-bit QCA counter circuit.

For 5-bit QCA counter circuit, the cell count, area and cost of the designed QCA counter circuit are considerably improved compared to QCA counter circuit in [15].

6 Conclusion

In the QCA circuits design, counters are the most used circuits. In this paper, 2-, 3-, 4- and 5-bit coplanar counter circuits were designed based on the modified QCA D-FF circuit designed in this paper. In the modified D-FF circuit, the inverse of the D-FF output was used as D-FF input. The designed circuits were simulated and verified by using the QCADesigner tool version 2.0.3. The developed coplanar counter circuits for the 2-, 3-, 4-, and 5-bit QCA counter have 44 (0.03 μm^2), 93 (0.07 μm^2), 160 (0.13 μm^2), and 245 (0.20 μm^2) quantum cells (area), respectively. The comparison results demonstrate that the designed QCA counter circuits have improvements compared with other counter circuits in [15–23] in terms of cell count, and area.

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