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Effective Designs of Reversible Vedic Multiplier

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Abstract
Power dissipation problem is one of the most challenging problems in designing conventional electronic circuits. One of the best approaches to overcome this problem is to design reversible circuits. Nowadays, reversible logic is considered as a new field of study that has various applications such as optical information processing, design of low power CMOS circuits, quantum computing, DNA computations, bioinformatics and nanotechnology. Due to the vulnerability of the digital circuits to different environmental factors, the design of circuits with error-detection capability is considered a necessity. Parity preserving technique is known as one of the most famous methods for providing error-detection ability. Multiplication operation is considered as one of the most important operations in computing systems, which can play a significant role in increasing the efficiency of such systems. In this paper, two efficient 4-bit reversible multipliers are proposed using the Vedic technique. The Vedic technique is able to increase the speed of multiplication operation by producing partial products and their sums simultaneously in a parallel manner. The first architecture lacks the parity preserving potential, while the second architecture has the ability parity preserving. Since a 4-bit Vedic multiplier includes 2-bit Vedic multipliers and 4-bit ripple carry adders (RCA), so in the first design, TG, PG and FG gates have been used to design an efficient 2-bit reversible Vedic multiplier, as well as PG gate and HNG block have been applied as a half-adder (HA) and full-adder (FA) in the 4-bit RCAs. Also, in the second design, 2-bit parity preserving reversible Vedic multiplier has been designed using FRG, DFG, ZCG and PPTG gates as well as ZCG and ZPLG blocks have been utilized as HA and FA in the 4-bit RCAs. Proposed designs are compared in terms of evaluation criteria of circuits such as gate count (GC), number of constant inputs (CI), number of garbage outputs (GO), quantum cost (QC), and hardware complexity. The results of the comparisons indicate that the proposed designs are more efficient compared to available counterparts.

Keywords Nanotechnology · Reversible logic · Vedic multiplier · Parity preserving · Quantum cost

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1 Introduction

One of the major challenges in conventional non-reversible circuits is the issue of internal energy dissipation, which becomes more evident with increasing the number of transistors per area unit. Landauer showed that in irreversible circuits, the loss of every bit of information would generate at least KTLn2 Jules of heat energy in which $K = 1.3806505 \times 10^{-23}$ (Joules/Kelvin) is Boltzmann constant and T is absolute temperature [1]. Afterwards, Bennett proved that the design of the circuits should be reversible to avoid energy dissipation, since the energy loss in the reversible circuits is zero. The reversible logic is considered as a new way to reduce the amount of physical entropy [2]. Hence, reversible logic is used in many areas such as low-power CMOS circuits, optical information processing, quantum processing, etc. [3, 4].

A circuit is reversible if any input is mapped to a unique output. In the reversible circuits, the number of inputs and outputs are equal. The design of reversible circuits is more complicated than irreversible ones because fan-out and feed back is not permitted in these circuits. In order to properly synthesize the reversible circuits, it is necessary to minimize the criteria such as the number of gate count (GC), number of constant inputs (CI), number of garbage outputs (GO) and hardware complexity (HC). One of the most important issues in the reversible circuits is the error-detection capability. Parity preserving is recognized as one of the low-cost approaches for creating error-detection potential in reversible circuits. A gate or block is called parity preserving gate (or block), if Ex-or of inputs equals to Ex-or of outputs.

So far, several reversible computing circuits have been presented, such as adders, multipliers, dividers, ALUs. Meanwhile, the multiplier circuit is considered as one of the most important computational units that comprises many calculations. In the following, some of the most important reversible multipliers will be reviewed.

In 2005, Thapliyal and Srinivas proposed a 4-bit Vedic multiplier using the FRG, NG and TG gates [5]. Also, in 2006, they introduced another design of 4-bit multiplier in which the partial product network consists of the FRG gates as well as TSG blocks is used as FA in the summation network [6].

In 2008, Shams et al. suggested a 4-bit multiplier in which PG gate is used for generating partial products and MKG block is utilized as FA in the summation network [7].

A 4-bit signed multiplier proposed by Pourali-akbar et al. in 2011 based on Wallace's technique. In its partial product network, the PG and TG gates are used, and in its summation network, the HNG block is used as FA [8].

In 2012, Babazadeh and Haghparast proposed a 4-bit parity preserving multiplier, which the FRG gate has been used in its partial product network and MIG gate in its summation network as FA [9].

A 5-bit parity preserving multiplier presented by Qi et al. based on Wallace's technique in 2012, which its partial product consists of the FRG, MNFT and F2G gates, as well as the MIG and F2PG blocks as FAs in the summation network [10].

In 2013, Saligram and Rakshith proposed a 4-bit parity preserving multiplier based on Vedic technique, which its multiplication partial network consisted of the FG, PG, BVPPG, and NFT gates, and in its summation network, the PG and HNG blocks have been used as FA [11].

In 2013, Haghparast and Shams proposed a 4-bit parity preserving reversible Vedic multiplier in which the FG, NFG and IG gates are used for designing 2-bit parity preserving Vedic multiplier and the IG gate is used as FA in the summation network [12].

In 2014, Panchal and Nayak provided a 4-bit parallel multiplier without parity preserving potential based on Wallace's technique, which the PG and TG gates have been used in its partial product network and the DPG and PG gates have been used in its summation network [13].

Parallel parity preserving multiplier provided in 2014 by Srikanth and Kumar based on the Vedic technique that the PG and FG gates have been used in its partial product network and the FRG gate has been used as FA in its summation network [14].

In 2014, Bhardwaj and Singh provided a parallel parity preserving multiplier based on Wallace's technique, that the FRG gate has been used in its partial product network and the IG and PG gates have been used as HA and FA in its summation network [15].

A 4-bit parity preserving multiplier presented by A. Sahu and A.K. Sahu in 2014 based on Vedic technique, that the NFT, DFG and IG gates have been used in its partial product network and the NFT and F2G gates have been used in its summation network [16]. In addition, 8-bit, 16-bit, 32-bit and 64-bit multipliers have been realized by them in 2015 [17].

Valinataj proposed a parity preserving multiplier based on array technique in 2017, that the FRG, F2G and LMH gates have been used in its partial product network and the ZCG, F2G and ZPLG blocks have been used in its summation network [18].

In 2017, Babu and Surendra provided a multiplier without parity preserving potential based on Vedic technique that the TG and PG gates have been used in its partial product network and the HNG block has been used in its summation network [19].

In this paper, two effective 4-bit reversible multipliers are presented based on the Vedic technique so that the first proposed design lacks error-detection capability, while the second proposed design has error-detection capability using the parity preserving technique. A 4-bit Vedic multiplier consists of four 2-bit Vedic multipliers and three 4-bitRCAs. In the first multiplier, we have utilized the TG, PG and FG gates for designing an effective 2-bit reversible Vedic multiplier as well as the PG gate and HNG block as HA and FA in the 4-bit RCAs. Also, in the second design, 2-bit parity preserving reversible Vedic multipliers have been designed using the FRG, DFG, ZCG and PPTG gates as well as ZCG and ZPLG blocks have been utilized as HA and FA in the4-bit RCAs. Moreover, in the proposed designs, the FG and DFG gates have been used as copy gates in the proposed multipliers.

This paper contains the following sections: in Section 2, primary definitions of the reversible logic as well as the basis of Vedic multipliers are presented. The proposed Vedic multipliers are presented in Section 3. In Section 4, the effectiveness of the proposed multipliers is compared with the existing ones. Finally, the paper ends with the conclusion section.

2 Preliminaries

2.1 An Introduction to Reversible Logic

A circuit is reversible if the number of inputs and outputs is equal and there is a one-to-one correspondence between inputs and outputs [20]. Not only can outputs be obtained in a unique way from inputs, but inputs can be obtained from the recovery of outputs. Reversible circuits are evaluated based on various criteria such as gate counts, number of constant inputs, number of garbage outputs, quantum cost, latency, and hardware complexity.

The total number of reversible gates required to analyze a reversible circuit is the number of gates. The constant inputs are equal to the input lines, which are represented as 0 or 1 at the input side of the circuit. Outputs that are not considered for further calculations are called garbage outputs. The linear quantum cost of a quantum circuit is defined as the sum of the initial quantum gates required for the analysis of a reversible circuit. The quantum cost of a 2 × 2 basic gate such as CNOT, Controlled-V, and Controlled-V + is all equal to one. In addition, $V \times V = V^+ \times V^+ = NOT$ and $V \times V^+ = V^+ \times V = I$, where I is a unitary matrix. The NOT gate is a basic 1 × 1 quantum gate and its quantum cost is equal to one. Latency or delay is considered as the maximum number of gates in the critical path from the input to the output.

The total number of logic operators in a reversible circuit is defined as the hardware complexity. In the hardware complexity, the parameters are as follows [21]:

α A 2-input XOR gate calculation
β A 2-input AND gate calculation
δ A NOT gate calculation

Therefore, computational complexity is introduced as follows:

$$\text{Hardware Complexity} = N(\alpha)\alpha + N(\beta)\beta + N(\delta)\delta \tag{1}$$

in which N (.) is equal to the number of operators in the reversible circuit.

So far, several reversible gates and blocks have been introduced that can be used to design reversible circuits. In the following, some of the most important of these gates and blocks will be investigated.

FG Gate The FG gate is a 2 × 2 reversible gate with I_v input and O_v output as follows:

I_v (A, B)
O_v ($P = A$, $Q = A \oplus B$)

The quantum realization and the circuit representation of the FG gate are shown in Fig. 1.

It should be noted, when the B input of FG gate is considered to be '0', it is used as copy gate (fan-out).

The quantum cost of the reversible FG gate is 1. Its hardware complexity is also as follows:

$$\text{Hardware Complexity}_{FG} = 1\alpha \tag{2}$$

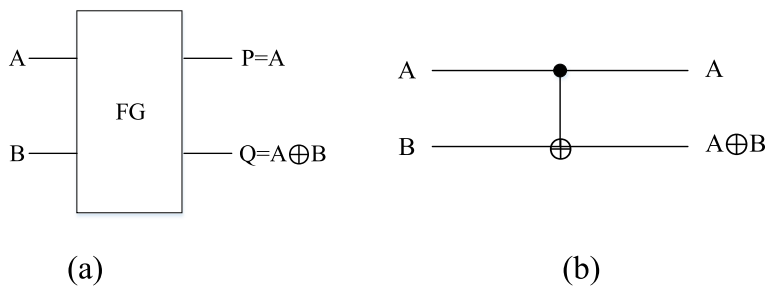


Fig. 1 FG gate (**a**) circuit display and **b** quantum realization

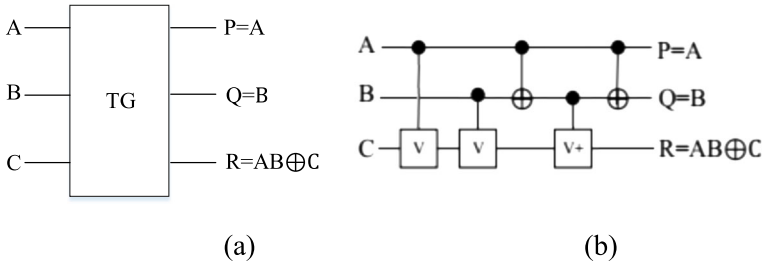


Fig. 2 TG gate (**a**) circuit display and **b** quantum realization

TG Gate The TG gate, also known as the CNOT gate, is a 3 × 3 reversible gate with I_v input and O_v output as follows [22]:

I_v (A, B, C)
O_v (P = A, Q = B, R = AB⊕C)

The quantum realization and the circuit representation of the TG gate are shown in Fig. 2.

As can be seen in Fig. 3, when the C input of TG gate is considered to be '0', the reversible AND gate is obtained.

The quantum cost of the reversible TG gate is five. Its hardware complexity is also as follows:

$$\text{Hardware Complexity}_{TG} = 1\alpha + 1\beta \tag{3}$$

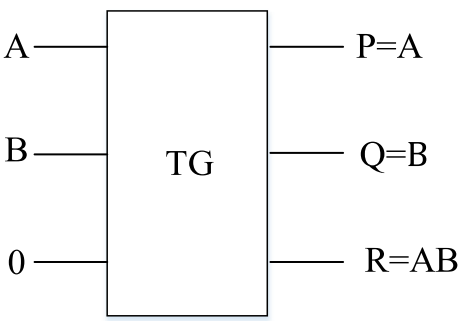
PG Gate The PG gate, also known as the new Toffoli gate (NTG), is a 3 × 3 reversible gate with I_v input and O_v output as follows [23]:

I_v (A, B, C)
O_v (P = A, Q = A⊕B, R = AB⊕C)

The circuit representation and quantum realization of the PG gate are shown in Fig. 4.

As shown in Fig. 5, the reversible PG gate can be used as a half-adder (HA) and AND gate in reversible circuits, when its input C is set to '0'.

Fig. 3 The generation of a reversible AND gate by TG gate



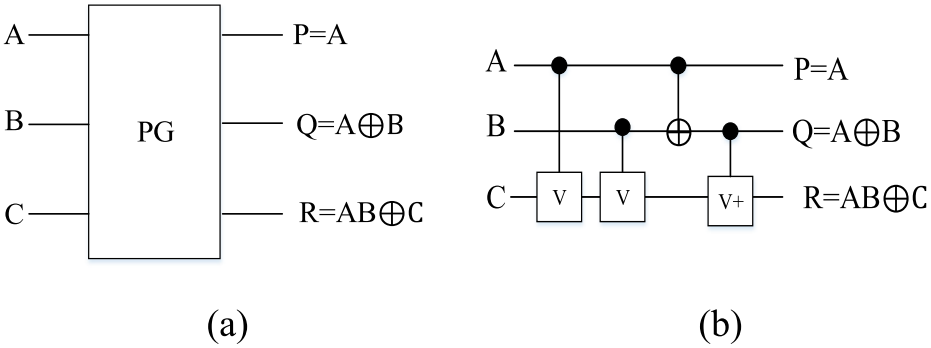


Fig. 4 PG gate (**a**) circuit display and **b** quantum realization

The quantum cost of a reversible PG gate is four. Also, its hardware complexity is expressed as:

$$\text{Hardware Complexity}_{PG} = 2\alpha + 1\beta \tag{4}$$

HNG Block The HNG block is a 4 × 4 reversible block with the input of the I_v and O_v output as follows [24]:

I_v (A, B, C, D)
O_v (P = A, Q = B, R = A ⊕ B ⊕ C, S = (A ⊕ B)C ⊕ AB⊕D)

The quantum realization and the circuit representation of the HNG gate are shown in Fig. 6.

The quantum cost of this block is six. The hardware complexity of this block is calculated from Eq. (4):

$$\text{Hardware Complexity}_{HNG} = 5\alpha + 2\beta \tag{5}$$

If the input D of the HNG block is set as '0', the HNG block will be used as a reversible full-adder (FA) (Fig. 7).

DFG Gate The DFG gate is a 3 × 3 parity preserving reversible gate with I_v input and O_v output as follows:

I_v (A, B, C)
O_v (P = A, Q = A⊕B, R = A⊕C)

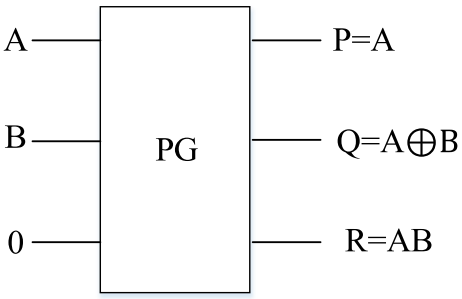


Fig. 5 Generate a reversible half-adder by the PG gate

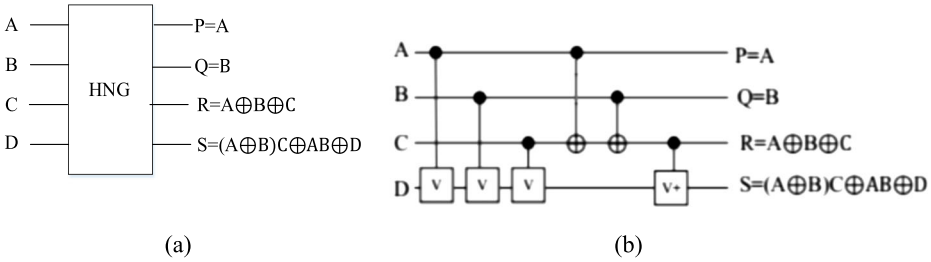


Fig. 6 HNG block (**a**) circuit display and **b** quantum realization

The quantum realization and the circuit representation of the DFG gate are shown in Fig. 8.

It should be noted, when the B or C inputs of DFG gate is considered to be '0', it is used as copy gate (fan-out).

The quantum cost of the parity preserving reversible DFG gate is 2. Its hardware complexity is also as follows:

$$\text{Hardware Complexity}_{\text{DFG}} = 2\alpha \tag{6}$$

FRG Gate The FRG gate is a 3 × 3 parity preserving reversible gate with the input of the I_v and O_v output as follows [25]:

I_v (A, B, C)
O_v (P = A, Q = AB⊕AC, R = AC ⊕ AB)

The quantum realization and the circuit representation of the FRG gate are shown in Fig. 9. The quantum cost of this gate is five and its hardware complexity is calculated from the following equation:

$$\text{Hardware Complexity}_{\text{FRG}} = 2\alpha + 4\beta + 2\gamma \tag{7}$$

As can be seen in Fig. 10, if the A input of FRG gate is considered to be '0', this gate can act as a buffer.

ZCG Gate The ZCG block is a 4 × 4 parity preserving reversible circuit with I_v input and O_v output as follows [26]:

I_v (A, B, C, D)
O_v (P = AB' ⊕ C, Q = A ⊕ B, R = AB⊕C, S = A ⊕ C ⊕ D)

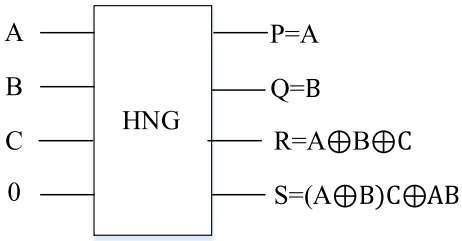


Fig. 7 HNG block as a reversible full-adder

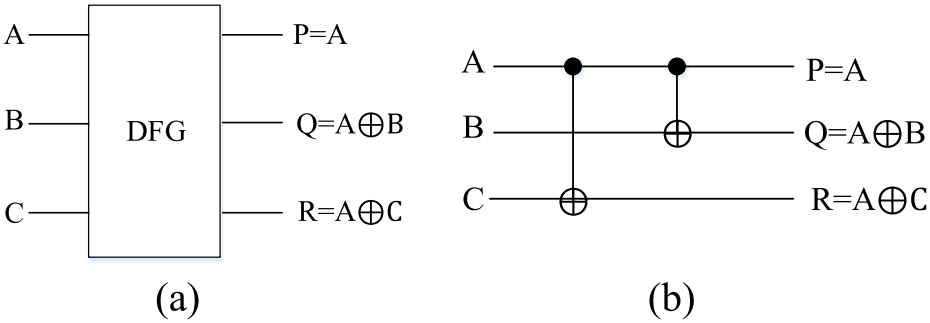


Fig. 8 DFG gate (**a**) circuit display and **b** quantum realization

The quantum realization and the circuit representation of the ZCG block are shown in Fig. 11.

The quantum cost of this gate is six and its hardware complexity is calculated from the following equation:

$$\text{Hardware Complexity}_{ZCG} = 5\alpha + 2\beta + 1\gamma \tag{8}$$

As can be seen in Fig. 12, by setting the C and D inputs as '0', it can be used to implement parity preserving reversible half-adder.

ZPLG Block The ZPLG block is a 5 × 5 parity preserving reversible gate with I_v input and O_v output as follows [26]:

I_v (A, B, C, D, E)
O_v (P = A ⊕ D, Q = A ⊕ B ⊕ D, R = A ⊕ B ⊕ C ⊕ D, S = (A ⊕ D)(B ⊕ C) ⊕ BC ⊕ D, T = (A ⊕ D)(B ⊕ C) ⊕ BC' ⊕ D ⊕ E)

The quantum realization and circuit representation of the ZPLG block is shown in Fig. 13.

The quantum cost of this gate is equal to eight, and its hardware complexity is calculated from the following equation:

$$\text{Hardware Complexity}_{ZPLG} = 9\alpha + 3\beta + 1\gamma \tag{9}$$

As shown in Fig. 14, by setting the D and E inputs as zero, it can be converted to a parity preserving reversible full-adder:

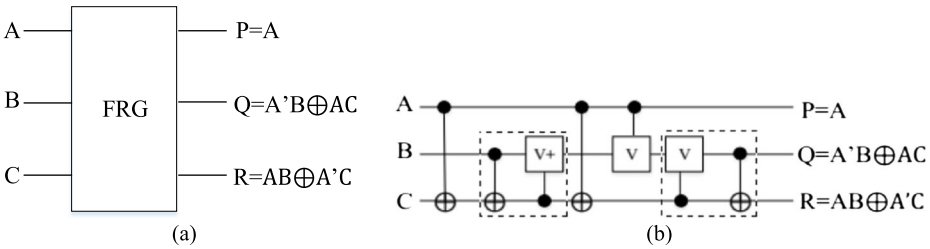


Fig. 9 FRG gate (**a**) circuit display and **b** quantum realization

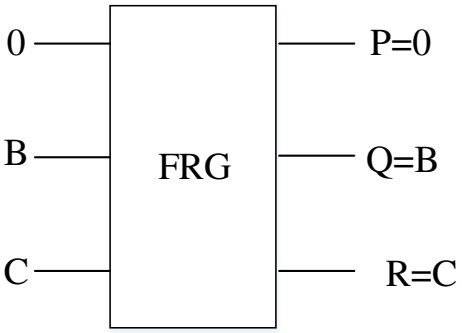


Fig. 10 FRG gate as a buffer

PPTG Gate The PPTG block is a 4 × 4 parity preserving reversible gate with I_v input and O_v output as follows [27]:

I_v (A, B, C, D)
O_v (P = A, Q = B, R = AB⊕C, S = AB⊕D)

The quantum realization and the circuit representation of the PPTG block are shown in Fig. 15.

The quantum cost of this gate is equal to seven, and its hardware complexity is calculated from the following equation:

$$\text{Hardware Complexity}_{\text{PPTG}} = 2\alpha + 1\beta \tag{10}$$

2.2 Vedic Multiplier

The Urdhva Tiryakbhayam (UM) algorithm is a method of multiplying numbers based on the old Vedic mathematics, which is suitable for multiplying the hexadecimal, decimal, and binary numbers [28]. The Sanskrit words of Urdhva and Tiryakbhayam are termed as "vertical" and "crossed" respectively. This algorithm is used to multiply two "vertical" and "crossed" operations. This method is based on the concept in which the production of partial product and summations is performed simultaneously, which increases the speed of the multiplication. This feature of UT algorithm is compatible with digital systems. The UT algorithm based multipliers are also called Vedic multipliers.

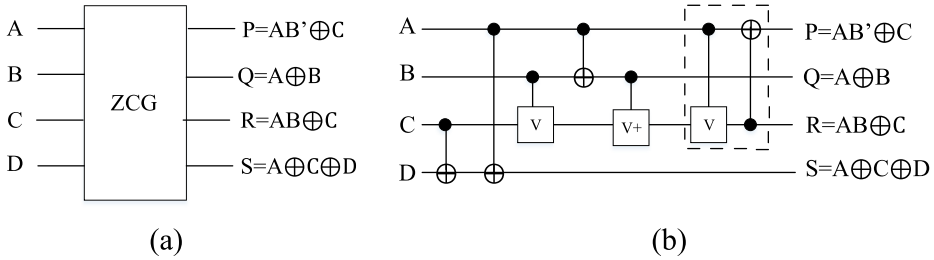


Fig. 11 ZCG block (**a**) circuit representation and **b** quantum realization

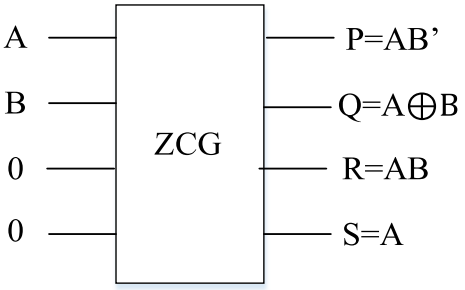


Fig. 12 Parity preserving reversible half-adder by the ZCG block

Consider two n-bit numbers of $A = (a_{n-1}, \ldots. a_1, a_0)$ and $B = (b_{n-1}, \ldots, b_1, b_0)$. The multiplication result of these two binary numbers can be expressed by the binary sequence of $P = (p_{2n-1},\ldots,p_1,p_0)$ so that we have:

$$p_j = \begin{cases} \sum_{i=0}^{j} a_i b_{j-1} & if\ j = 0, 1 \\ C_{j-1} + \sum_{i=0}^{j} a_i b_{j-i} & if\ j = 2.\cdots..n-1 \\ C_{j-1} + \sum_{i=0}^{2n-j-2} a_{i+j-n+1} b_{n-1-i} & if\ j = 2.\cdots..2n-2 \\ C_{j-1} & if\ j = 2n-1 \end{cases} \tag{11}$$

That C_j represents the carry of the j-th step.

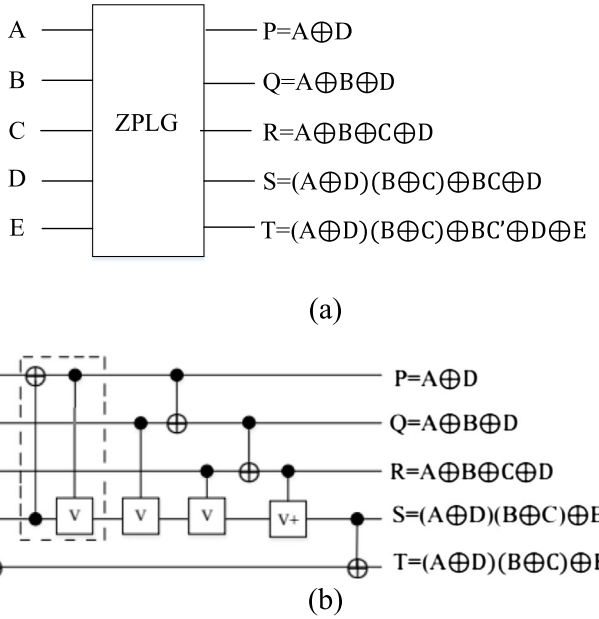


Fig. 13 ZPLG block (**a**) circuit representation and **b** quantum realization

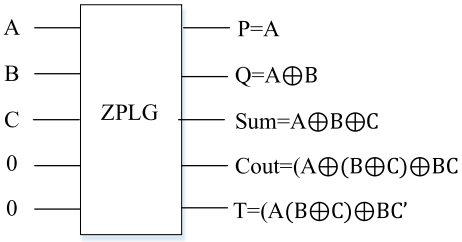


Fig. 14 parity preserving reversible full-adder by ZPLG block

According to the presented relations in Eq. (11), the operation of a 2-bit Vedic multiplier with $A = (a_1,a_0)$ and $B = (b_1,b_0)$ is as follows:

$$\begin{aligned} p_0 &= a_0 b_0 \\ p_1 &= a_0 b_1 \oplus a_1 b_0 \\ p_2 &= C_1 \oplus a_1 b_1 = a_0 b_1 a_1 b_0 \oplus a_1 b_1 \\ p_3 &= C_2 = a_0 b_1 a_1 b_0 \end{aligned} \tag{12}$$

Hardware implementation of 2-bit Vedic multiplier requires two half-adder (HA) and four AND gate, as shown in Fig. 16.

Moreover, block diagram of a 4-bit Vedic multiplier is shown in Fig. 17 [29].

3 Proposed Reversible Vedic Multipliers

As shown in Fig. 17, a modular design of a 4-bit Vedic multiplier is made up of three levels, in which four 2-bit Vedic multipliers have been used in the first level, two 4-bit RCAs in the second level, and one 4-bit RCA in the third level. In the following, two proposed 4-bit reversible Vedic multipliers are described.

3.1 Proposed 4-Bit Reversible Vedic Multiplier

In order to implement the reversible Vedic multiplier provided in Fig. 17, it is necessary to implement all the used modules in it with reversible circuits. The implementation of proposed reversible for the 2-bit Vedic multiplier module is shown in Fig. 18.

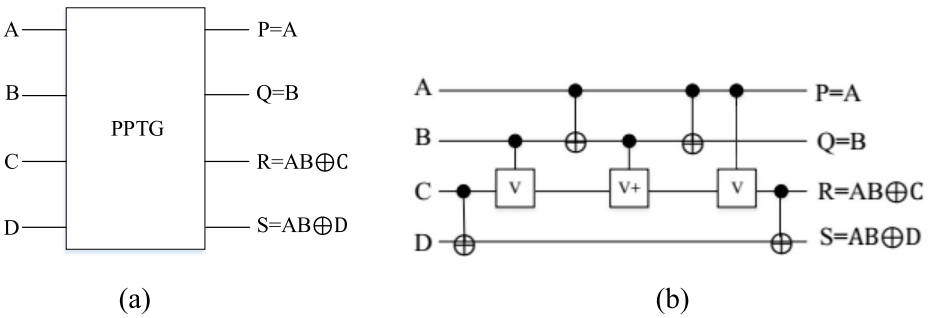


Fig. 15 PPTG block (**a**) circuit display and **b** quantum realization

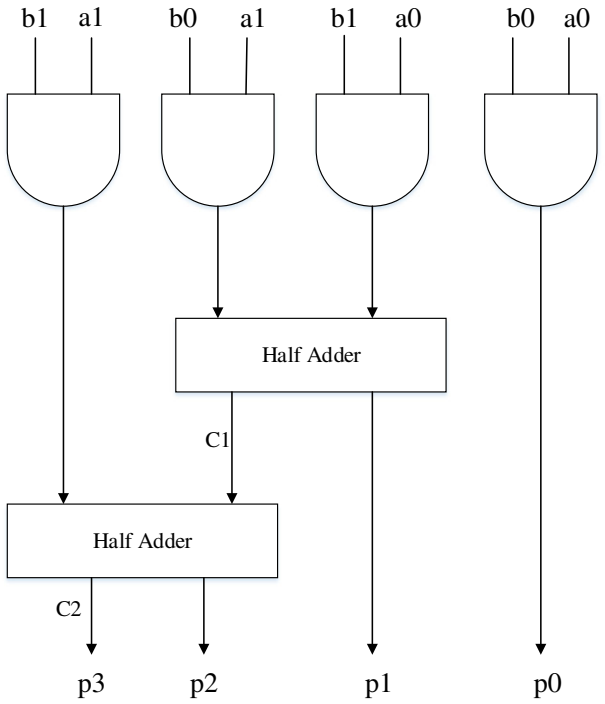


Fig. 16 The structure of 2-bit Vedic multiplier

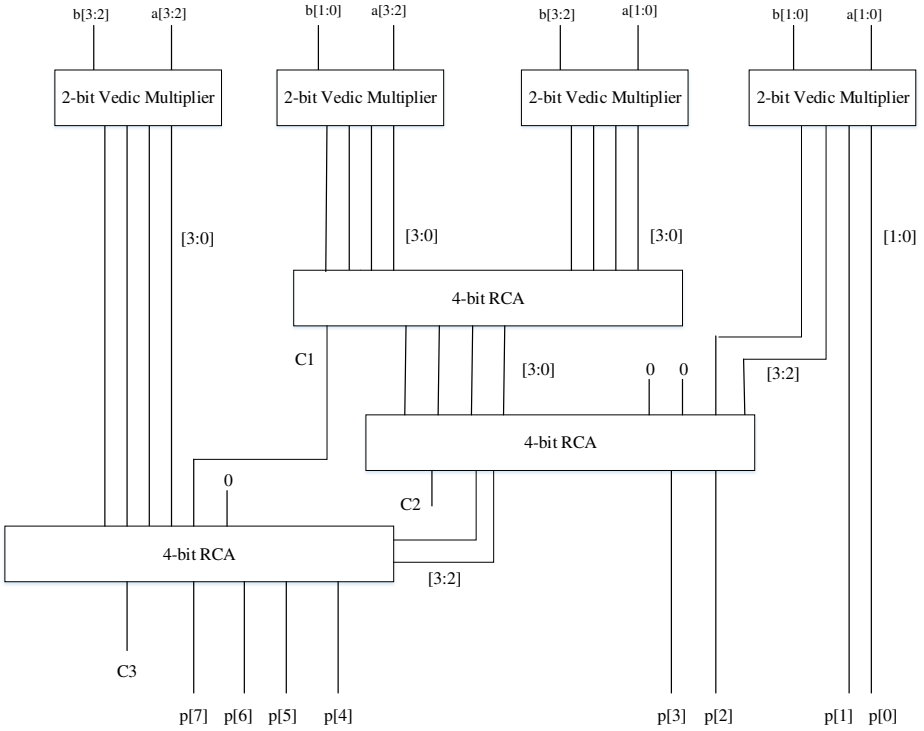


Fig. 17 Architecture of a 4-bit Vedic multiplier [29]

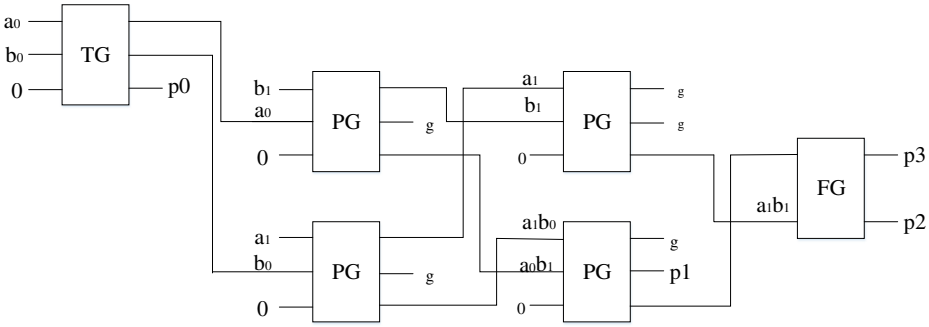


Fig. 18 The proposed reversible circuit for implementing 2-bit Vedic multiplier

As can be seen, the proposed circuit is composed of a reversible TG gate and five reversible PG gates. The number of its constant input and its garbage outputs is equal to 5. In addition, its quantum cost is 22.

Also, implementation of a reversible 4-bit RCA using the HNG block and PG gate is shown in Fig. 19.

Therefore, the 4-bit reversible RCA has constant input number equal to 4, the garbage output of 7 and the quantum cost of 22.

Block diagram of the proposed 4-bit reversible Vedic multiplier is shown in Fig. 20.

Therefore, the quantum cost of the proposed reversible Vedic multiplier is calculated as follows:

$$\begin{aligned} &QC(\text{proposed 4−bit reversible Vedic multiplier}) \\ &= 8QC(FG) + 4QC(\text{proposed 2−bit reversible Vedic multiplier}) \\ &\qquad + 3QC(\text{4−bit reversible RCA}) = \\ &= 8(1) + 4(22) + 3(22) = 162 \end{aligned}$$

3.2 Proposed Parity Preserving Reversible 4-Bit Vedic Multiplier

The proposed circuit is shown in Fig. 21 for implementing reversible 2-bit Vedic multiplier module with the parity preserving ability.

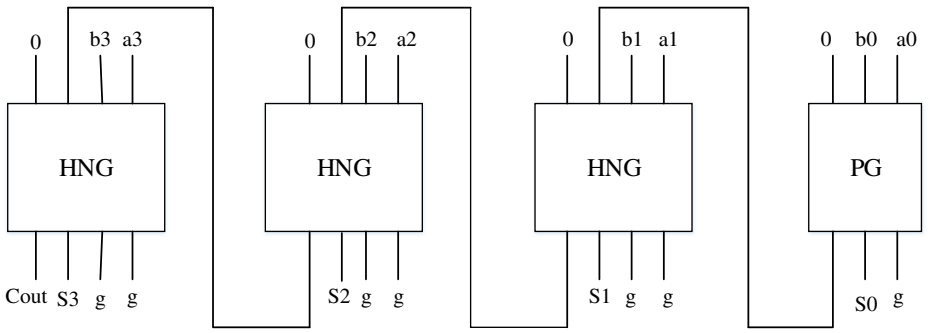


Fig. 19 Implementation of 4-bit reversible RCA using the HNG block and PG gate

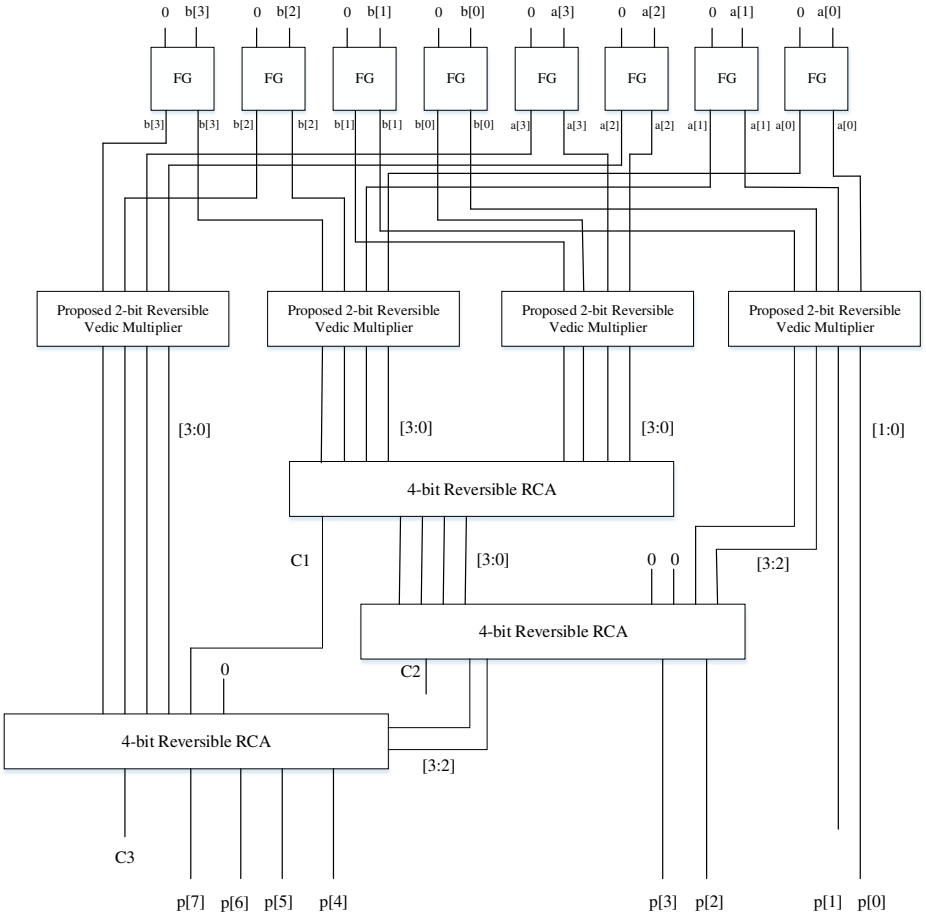


Fig. 20 Architecture of the proposed 4-bit reversible Vedic multiplier

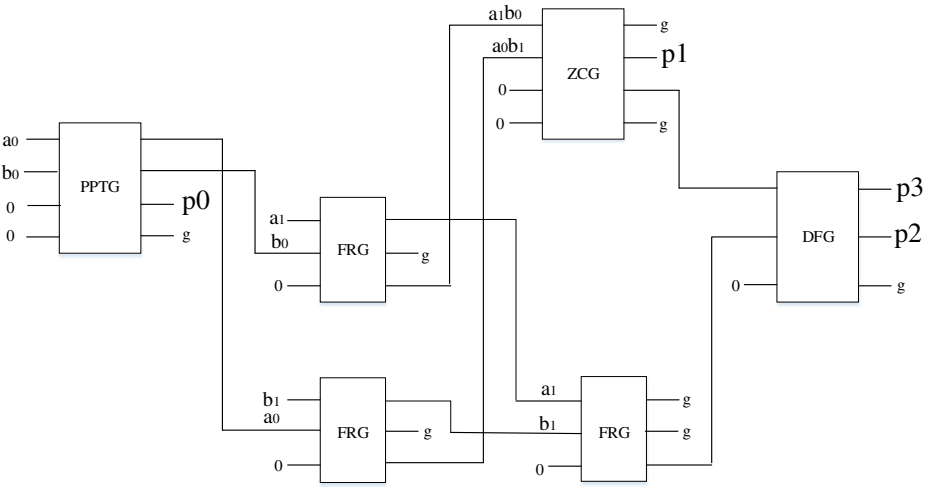


Fig. 21 The proposed reversible circuit to implement 2-bit parity preserving reversible Vedic multiplier

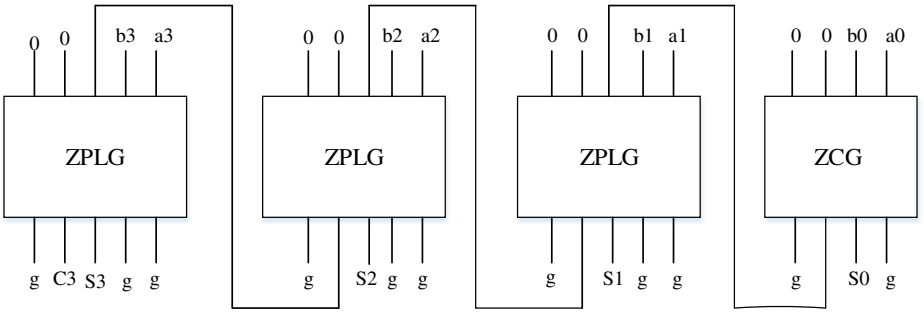


Fig. 22 The reversible implementation of a 4-bit parity preserving reversible RCA with ZCG and ZPLG blocks

The proposed circuit consists of a PPTG block, three FRG gates and two ZCG blocks, all of which are capable of parity preserving. The number of constant inputs as well as garbage outputs is equal to 8. In addition, the quantum cost is 30.

Also, the reversible implementation of a 4-bit RCA using ZCG and ZPLG blocks is shown in Fig. 22.

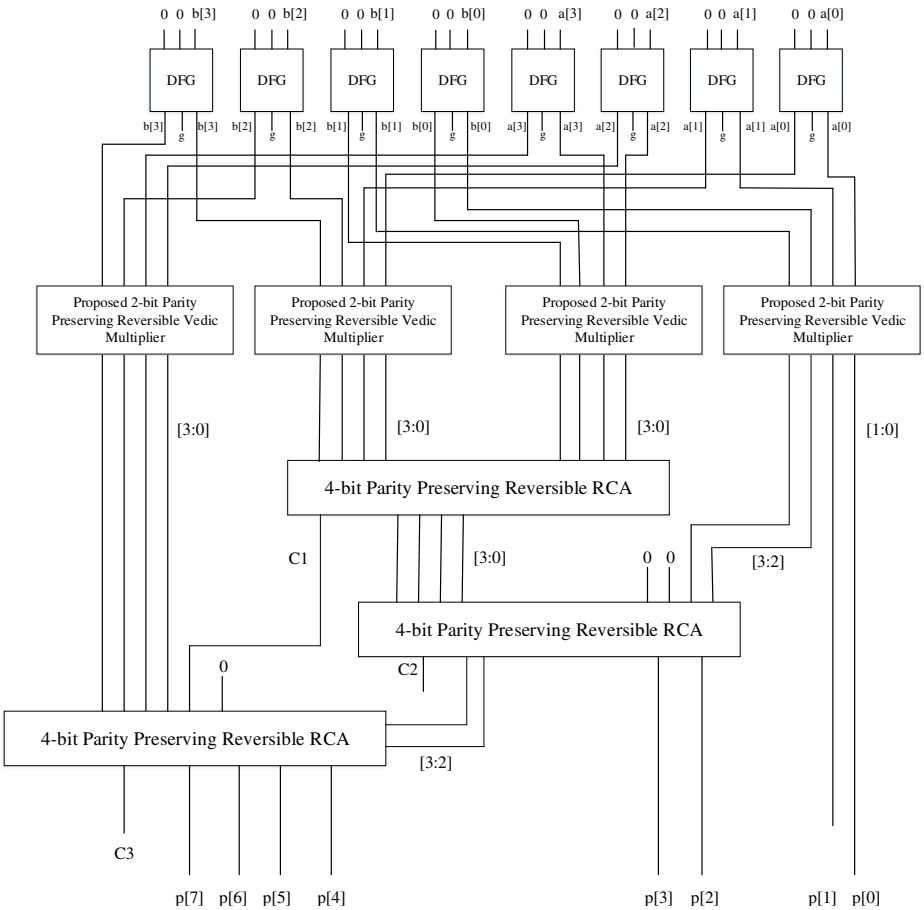


Fig. 23 Architecture of the proposed 4-bit parity preserving reversible Vedic multiplier

Table 1 The comparison results of the 4-bit reversible multipliers

Designs	GC	CI	GO	QC	HC
In [5]	12FG + 16FRG + 12NG + 12TG = 52	43	56	224	$92\alpha + 100\beta + 68\gamma$
In [6]	24FG + 16FRG + 13TSG = 53	58	58	286	$134\alpha + 103\beta + 71\gamma$
In [7]	24FG + 16PG + 12MKG = 52	56	56	244	$116\alpha + 52\beta + 36\gamma$
In [19]	8FG + 16TG + 8PG + 12HNG = 44	44	48	192	$100\alpha + 48\beta$
Proposed	12FG + 19PG + 4TG + 9HNG = 44	40	41	162	$99\alpha + 41\beta$

As can be inferred from Fig. 22, the number of constant inputs and garbage outputs of the 4-bit parity preserving reversible RCA are equal to 8 and 11, respectively. Moreover, its quantum cost is $[(3 \times 8) + 6] = 30$.

Block diagram of the proposed 4-bit parity preserving reversible Vedic multiplier is shown in Fig. 23.

Therefore, the quantum cost of the proposed 4-bit parity preserving reversible Vedic multiplier is calculated as follows:

$$\begin{aligned} &\mathrm{QC}(\text{proposed 4−bit parity preserving reversible Vedic multiplier}) \\ &= 8\mathrm{QC}(\mathrm{DFG}) + 4\mathrm{QC}(\text{proposed 2−bit Vedic}) \\ &\qquad + 3\mathrm{QC}(\text{4−bit parity preserving reversible RCA}) = \\ &= 8(2) + 4(30) + 3(30) = 226 \end{aligned}$$

4 Evaluation and Comparison Results

In this section, the proposed 4-bit reversible Vedic multipliers are compared with previous works in terms of gate counts, number of constant inputs, number of garbage outputs, quantum cost and hardware complexity.

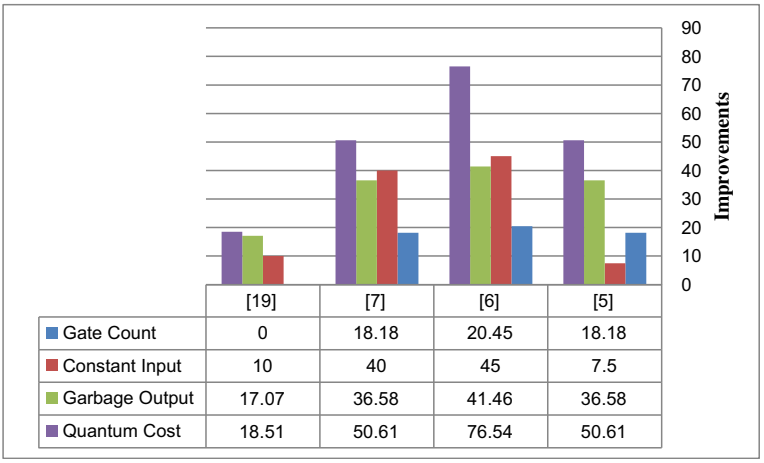


Fig. 24 Improvement of the proposed reversible Vedic multiplier compared to other designs

Table 2 Comparison results of 4-bit parity preserving reversible multipliers

Designs	GC	CI	GO	QC	HC
In [9]	12DFG + 16FRG + 20MIG = 48	64	68	244	$116\alpha + 104\beta + 52\gamma$
In [12]	24DFG + 32IG + 16NFT = 72	102	110	352	$224\alpha + 144\beta + 64\gamma$
Proposed	12DFG + 12FRG + 4PPTG + 7ZCG + 9ZPLG = 44	72	73	226	$172\alpha + 93\beta + 40\gamma$

The evaluation results of the proposed 4-bit reversible multiplier in comparison with previous designs are provided in Table 1. It should be noted that in the most of the previous designs, the issue of copying of the inputs (fan out) is not met. Therefore, in order to make a fair comparison, the designs which this issue has not been seen in them, have been modified using the FG gate and, accordingly, the results of the evaluations, have been reported which in some cases, the results are different from the presented values in their papers.

As shown in Table 1, the proposed reversible Vedic multiplier is superior to the other available designs in terms of the number of gates, number of constant inputs, the number of garbage outputs and quantum cost. In addition, the improvement percentage of proposed reversible Vedic multiplier is shown in Fig. 24.

Moreover, the evaluation results of the proposed 4-bit parity preserving reversible multiplier in comparison with the existing designs are shown in Table 2.

As can be seen in Table 2, although the proposed parity preserving reversible multiplier is close to the proposed designs in [9, 12] in terms of number of constant inputs and garbage output, however, is superior to all designs in terms of the gate counts and quantum cost (Fig. 25).

5 Conclusion

In this paper, two efficient 4-bit reversible Vedic multipliers were presented. The first multiplier was a reversible multiplier without parity preserving capability in which the FG, TG and PG gates were used to design 2-bit reversible Vedic multiplier as well as the PG gate

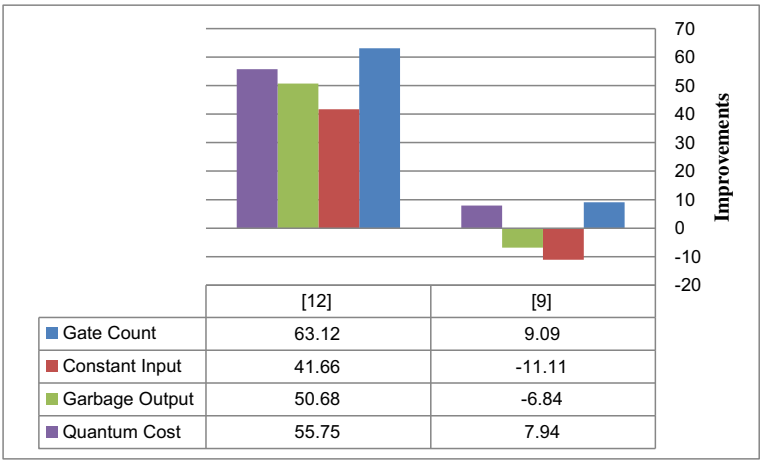


Fig. 25 Improvement of the 4-bit proposed parity preserving reversible Vedic multiplier in comparison with existing design

and HNG block were used as HA and FA in the summation network. The second design was a 4-bit parity preserving reversible Vedic multiplier, in which the DFG, FRG and PPTG gates were utilized to design 2-bit parity preserving reversible Vedic multiplier and the ZCG and ZPLG blocks were used as HA and FA in the summation network. The comparison results show that the proposed reversible multipliers are superior in term of criteria such as gate count, number of constant inputs, number of garbage output and quantum cost compared to other existing designs. In the future, we plan to develop efficient designs of signed reversible multipliers and then apply them in the more complex reversible circuits such as adaptive digital filter and ALU.

References

1. Landauer, R.: Irreversibility and heat generation in the computing process. IBM J. Res. Dev. **5**(3), 183–191 (1961)
2. Bennett, C.H.: Logical reversibility of computation. IBM J. Res. Dev. **17**(6), 525–532 (1973)
3. Biswas, A.K., Hasan, M.M., Chowdhury, A.R., Hasan Babu, H.M.: Efficient approaches for designing reversible binary coded decimal adders. Microelectron. J. **39**(12), 1693–1703 (2008)
4. M. Noorallahzadeh, and M. Mosleh, "Efficient designs of reversible latches with low quantum cost," IET Circ Device Syst, vol. In Press, (2019)
5. Thapliyal, H., Srinivas, M., Arabnia, H.R.: A reversible version of 4 x 4 bit Array multiplier with minimum gates and garbage outputs. In: ESA, pp. 106–116 (2005)
6. Thapliyal, H., Srinivas, M.: Novel reversible multiplier architecture using reversible TSG gate. In: in the 4th ACS/IEEE international conference on computer systems and applications, Dubai, UAE (2006)
7. Shams, M., Haghparast, M., Navi, K.: Novel reversible multiplier circuit in nanotechnology. World Appl. Sci. J. **3**(5), 806–810 (2008)
8. Akbar, E.P.A., Haghparast, M., Navi, K.: Novel design of a fast reversible Wallace sign multiplier circuit in nanotechnology. Microelectron. J. **42**(8), 973–981 (2011)
9. Babazadeh, S., Haghparast, M.: Design of a nanometric fault tolerant reversible multiplier circuit. JBASR. **2**(2), 1355–1361 (2012)
10. Qi, X., et al.: Design of fast fault tolerant reversible signed multiplier. International Journal of Physical Sciences. **7**(17), 2506–2514 (2012)
11. Saligram, R., Rakshith, T.: Optimized reversible vedic multipliers for high speed low power operations. In: IEEE Conference on Information & Communication Technologies (ICT), pp. 809–814 (2013)
12. Haghparast, M., Shams, M.: A novel nanometric parity preserving reversible Vedic multiplier. JBASR. **3**(8), 771–776 (2013)
13. Panchal, V.K., Nayak, V.H.: Analysis of multiplier circuit using reversible logic. International Journal for Innovative Resaerch in Science & Technology. **1**(6), 279–284 (2014)
14. Srikanth, G., Kumar, N.S.: Design of High speed low power reversible Vedic multiplier and reversible divider. Int. J. Eng. Res. Appl. **4**(9), 70–74 (2014)
15. Bhardwaj, P., Singh, M.: An improved design of a fault tolerant reversible binary parallel multiplier. International (IJETR). **2**(9), 72–76 (2014)
16. Sahu, A., Sahu, A.K.: High speed fault tolerant reversible vedic multiplier. International Journal of Innovative Research in Advanced Engineering (IJIRAE) ISSN. **2**(6), 2349–2163 (2014)
17. Sahu, A., Sahu, A.K.: Design of high speed 64x64 bit fault tolerant reversible Vedic multiplier. International Reseach Journal of Engineering and Technology. **2**(3), 880–887 (2015)
18. Valinataj, M.: Design of parity-preserving reversible logic signed array multipliers. World Academy of Science, Engineering and Technology, International Journal of Mathematical, Computational, Physical, Electrical and Computer Engineering. **11**(7), 250–257 (2017)
19. Babu, K.S., Surendra, S.: Reversible ALU design using low power Vedic multiplier. International Journal of Research and Engineering. **4**(4), 107–113 (2017)
20. Haghparast, M., et al.: Optimized reversible multiplier circuit. J Circuit Syst Comp. **18**(02), 311–323 (2009)
21. E. PourAliAkbar, and M. Mosleh, "An efficient design for reversible wallace unsigned multiplier," Theor. Comput. Sci., 773 ,43-52 (2018)
22. Toffoli, T.: Reversible computing. In: International colloquium on automata, languages, and programming, pp. 632–644 (1980)

23. Peres, A.: Reversible logic and quantum computers. Phys. Rev. A. **32**(6), 3266–3276 (1985)
24. Haghparast, M., et al.: Design of a novel reversible multiplier circuit using HNG gate in nanotechnology. World Appl. Sci. J. **3**(6), 974–978 (2008)
25. Fredkin, E., Toffoli, T.: Conservative logic. Int. J. Theor. Phys. **21**(3–4), 219–253 (1982)
26. Zhou, R.-G., Li, Y.-C., Zhang, M.-Q.: Novel designs for fault tolerant reversible binary coded decimal adders. Int. J. Electron. **101**(10), 1336–1356 (2014)
27. A. Jain, and S. C. Jain, "Towards implementation of fault tolerant reversible circuits," in 1st international conference on emerging trends and applications in computer science, pp. 86–91 (2013)
28. Vijeyakumar, K., Elango, S., Kalaiselvi, S.: VLSI implementation of high speed energy-efficient truncated multiplier. Journal of Circuits Systems and Computers. **27**(05), 1850077 (2018)
29. Jais, A., Palsodkar, P.: Design and implementation of 64 bit multiplier using vedic algorithm. In: 2016 International Conference on Communication and Signal Processing (ICCSP), pp. 0775–0779 (2016)