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An Improved Design of *n*-Bit Universal Reversible Gate Library

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Abstract
Reversible logic has been considered as an important solution to the power dissipation problem in the existing electronic devices. Many universal reversible libraries that include more than one type of gates have been proposed in the literature. This paper proposes a novel reversible *n*-bit gate that is proved to be universal for synthesizing reversible circuits. Reducing the reversible circuit synthesis problem to permutation group allows Schreier-Sims Algorithm for the strong generating set-finding problem to be used in the synthesize of reversible circuits using the proposed gate. A novel optimization rules will be proposed to further optimize the synthesized circuits in terms of the number of gates, the quantum cost and the utilization of library to achieve better results than that shown in the literature.

Keywords Networks (circuits) · Universal Gate · Synthesis · Logic Gates · Group Theory

1 Introduction

Research in reversible logic circuits [1, 2] is motivated by the advances in quantum computation [3, 4] , low-power design CMOS [5, 6] and many more. Landauer [7] proved that any

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conventional, irreversible gate dissipates a certain amount of energy per operation. Bennett [1] shows that the power dissipation can be avoided in a circuit if and only if the circuit is synthesized using reversible gates.

Recently, the study of reversible logic synthesis problem using group theory is rising rapidly. Investigation on the universality of the basic building blocks of reversible circuits has been presented [8, 9]. A relation between the reversible logic synthesis problem and Young subgroups has been discussed [10]. A difference between the decomposition of a quantum circuit and a reversible circuit using group theory has been shown [11]. GAP-based algorithms that is used to synthesize reversible circuits for various types of gates, and with various gate costs have been proposed [12–14, 22]. GAP-based algorithms that is used to synthesize reversible circuits for one type of gates have been proposed [15, 25].

The aim of the paper is to propose a novel reversible n-bit gate that is proved to be universal for reversible circuit synthesis. The proposed gate is extendable according to the number of bits in the circuit design. The proposed gate is important as it is a single type of gate and using this technology might be cheaper to implement. All results shown in this paper have been implemented and tested using the group theory algebraic software GAP [16]. The experimental results using the proposed gate library show better quantum cost and utilization of the gate library compared to the existing work in [15, 25]. Some obtained results matches the results obtained by other methods such as [12, 17, 18, 22].

The paper is organized as follows: Section 2 reviews the required background for the synthesis of reversible circuit problem. In addition, it shows that the problem can be reduced to permutation group, and gives an analysis about the universality properties of the common universal reversible libraries in the literature. Section 3 presents the proposed gate library and its properties. Section 4 discusses the experimental results and shows a comparison with relevant results obtained by others in the literature. The paper ends up with a summary and conclusion in Section 5.

2 Preliminaries

This section will review the basic concepts of reversible circuits, terminologies used for reversible circuit synthesis and the relationship between reversible logic circuits and permutation group theory.

Let $X = \{0,1\}$ and define a Boolean function f with n input variables $x_1,\ldots,x_n$ and n output variables $y_1,\ldots,y_n$, to be a function $f : X^n \rightarrow X^n$, where $(x_1,\ldots,x_n) \in X^n$ is called the input vector and $(y_1,\ldots,y_n) \in X^n$ is called the output vector. An n-input n-output Boolean function is reversible ($n \times n$ function) if it maps each input vector to a unique output vector, i.e. bijection. There are $2^n!$ reversible $n \times n$ Boolean functions. For $n = 3$, there are 40320 3-in/out reversible functions.

An n-input n-output (n-in/out) reversible gate (or circuit) is a gate that realizes an $n \times n$ reversible function. A set of reversible gates that can be used to build a reversible circuit is called a gate library L [15]. A universal reversible gate library L_n is a set of reversible gates such that a cascading of gates in L_n can be used to synthesize any reversible circuit with n-in/out [15]. A universal reversible gate sub library SL_n is a set of reversible gates such that $SL_n \subseteq L_n$ that can be used to build any reversible circuit with n-in/out [15]. Let $|L_n|$ be the number of gates in L_n and $|SL_n|$ be the number of gates in SL_n, then the ratio $2^{|SL_n|}/2^{|L_n|}$ represents the *utilization of gates* in a universal sub library and the ratio $2^{\min(|SL_n|)}/2^{|L_n|}$ represents the utilization of gates in the smallest universal sub libraries from a universal library [15].

Let a finite set $A = \{1,2,\ldots,2^n\}$ and a bijection $\delta : A \rightarrow A$, then can be written as, $\begin{pmatrix} 1 & 2 & 3 & \cdots & 2^n \\ \delta(1)\delta(2)\delta(3)\cdots\delta(2^n) \end{pmatrix}$, i.e. δ is a permutation of A. Let A be an ordered set, then the top row can be eliminated and δ can be written as,

$$\left(\delta(1)\delta(2)\delta(3)\cdots\delta(2^n)\right). \tag{1}$$

Any reversible circuit with n-in/out can be considered as a permutation and Eq..1 is called the specification of this reversible circuit [15]. The set of all permutations on A forms a symmetric group on A under composition of mappings [18], denoted by S_{2^n} [19]. A permutation group G is a subgroup of the symmetric group S_{2^n} [18]. A universal reversible gate library L_n is called the generators of the group. Another important notation of a permutation is the product of disjoint cycles [19]. For example, $\begin{pmatrix} 1,2,3,4,5,6,7,8 \\ 8,2,6,4,5,3,1,7 \end{pmatrix}$ will be written as (1,8,7)(3,6). The identity mapping "()" is called the unit element in a permutation group. A product $p * q$ of two permutations p and q means applying mapping p then q, which is equivalent to cascading p and q [20].

2.1 Reversible Circuits

The C^nNOT gate is a reversible gate that can be used to build any n-in/out reversible circuits. It is denoted in [13] as,

$$C^n\text{NOT}(x_1, x_2, \cdots, x_{n-1}; f),$$

with n inputs:x_1,x_2,$\cdots$,x_{n-1} (named control bits) and f_{in} (named target bit), and n outputs:y_1,y_2,$\cdots$,y_{n-1} and f_{out}. The operation of the C^nNOT gate is defined as follows,

$$y_i = x_i, \text{for} 1 \leq i \leq n-1,\ f_{\text{out}} = f_{\text{in}} \oplus x_1, x_2 \cdots x_{n-1},$$

i.e. if the control bits are set to 1 then the target bit is flipped, otherwise the target bit is left unchanged. The C^nNOT gate is represented by the circuit shown in Fig. 1.

There exist three special cases of the C^nNOT gate and are defined as, C^1NOT gate with no control bit is called *NOT* gate. C^2NOT gate with one control bit is called *CNOT*. C^3NOT gate with two control bits is called Toffile gate. For the ease of readability C^1NOT, C^2NOT and C^3NOT can be written as *N*, *C* and *T* respectively where the control and/or target bits will be shown in the subscript of the gate and the total number of bits will be shown in the superscript. Many quantum gates have been studied but we focus on the elementary quantum gates *NOT*, *CNOT*, Controlled-V (v) and Controlled-V^+ (u), also known as quantum primitives. These gates have been widely used to synthesize reversible circuits [26]. The Controlled-V (v) and the Controlled-V^+ (u) gates are represented by the matrices as follows, $v = \frac{1+i}{2}\begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}$ and $u = \frac{1-i}{2}\begin{pmatrix} 1i \\ i1 \end{pmatrix}$, where $vu = uv = I$, $vv = uu = N$ and I is the identity gate [26].

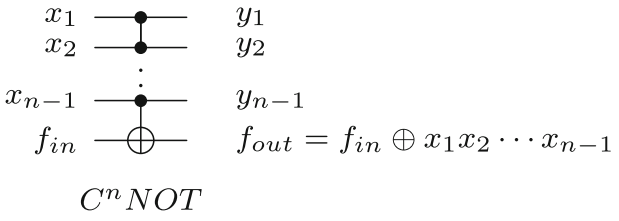


Fig. 1 C^nNOT gate.The control bit is denoted by , and the target bit is denoted by $\oplus$

The quantum cost of a reversible circuit is measured by the number of elementary gates required to build the C^nNOT gate [26], which are considered as the number of 2-qubit gates used in its implementation as a circuit. In this paper, we use the cost015 metric [12], the quantum cost of *NOT* gate is 0 (zero), the quantum cost of any 2-qubit gate is 1 and the quantum cost of the T^3 gate is 5.

The *NOT* (*N*) gate acts on a 1-bit and it is defined as follows, it flips the input bit unconditionally with quantum cost equal zero [12]. A gate library with N^3 gates is not universal for 3-in/out reversible circuits since it can realize 8 circuits from the 40320 circuits [15]. There are 3 possible N^3 gates for the 3-in/out reversible circuits as shown in Fig. 2, that perform as follows:

$$\begin{aligned} N_1^3 &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus 1, x_2, x_3) \equiv (1,5)(2,6)(3,7)(4,8), \\ N_2^3 &: (x_1, x_2, x_3) \rightarrow (x_1, x_2 \oplus 1, x_3) \equiv (1,3)(2,4)(5,7)(6,8), \\ N_3^3 &: (x_1, x_2, x_3) \rightarrow (x_1, x_2, x_3 \oplus 1) \equiv (1,2)(3,4)(5,6)(7,8). \end{aligned} \tag{2}$$

The Feynman (*C*) gate acts on two-bits and it is defined as follows, if the control bit is set to 1 then the target bit line is flipped. A gate library with C^3 gates is not universal for 3-in/out reversible circuits, since it can realize 168 circuits from the 40320 reversible circuits [15]. There are 6 possible C^3 gates for the 3-in/out reversible circuits as shown in Fig. 3, that perform as follows:

$$\begin{aligned} C_{12}^3 &: (x_1, x_2, x_3) \rightarrow (x_1, x_2 \oplus x_1, x_3) \equiv (5,7)(6,8), \\ C_{13}^3 &: (x_1, x_2, x_3) \rightarrow (x_1, x_2, x_3 \oplus x_1) \equiv (5,6)(7,8), \\ C_{23}^3 &: (x_1, x_2, x_3) \rightarrow (x_1, x_2, x_3 \oplus x_2) \equiv (3,4)(7,8), \\ C_{21}^3 &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_2, x_2, x_3) \equiv (3,7)(4,8), \\ C_{32}^3 &: (x_1, x_2, x_3) \rightarrow (x_1, x_2 \oplus x_3, x_3) \equiv (2,7)(6,8), \\ C_{31}^3 &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_3, x_2, x_3) \equiv (2,6)(4,8). \end{aligned} \tag{3}$$

The Toffile (T^3) gate acts on three-bits and it is defined as follows, if the two control bits are set to 1 then the third target bit line is flipped. The T^3 gate is the smallest reversible gate that is proved to be universal for non-reversible computation as it is proved to function as

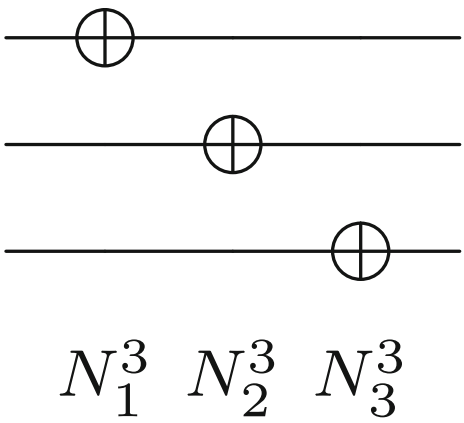


Fig. 2 The 3 possible *N* gates for 3-bit reversible circuits

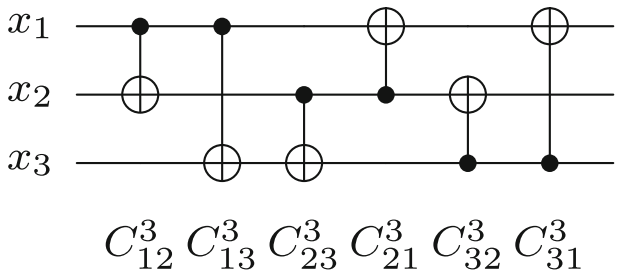


Fig. 3 The 6 possible C gates for 3-bit reversible circuits

NAND gate by initializing the target bit to 1 [21]. A gate library with T^3 gate is not universal for 3-in/out reversible circuits, since it can realize 24 circuits from 40320 reversible circuits [15]. There are three possible T^3 gates for the 3-in/out reversible circuits as shown in Fig. 4, that perform as follows:

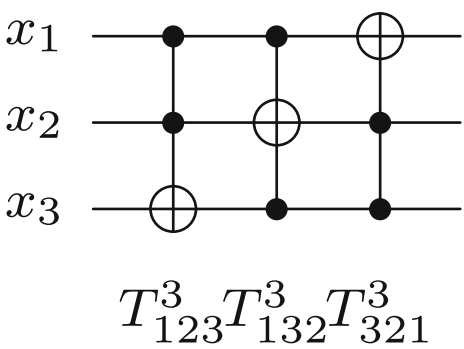
$$\begin{aligned} T^3_{123} &: (x_1, x_2, x_3) \rightarrow (x_1, x_2, x_3 \oplus x_1x_2) \equiv (7, 8), \\ T^3_{132} &: (x_1, x_2, x_3) \rightarrow (x_1, x_2 \oplus x_1x_3, x_3) \equiv (6, 8), \\ T^3_{321} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_2x_3, x_2, x_3) \equiv (4, 8). \end{aligned} \tag{4}$$

The Fredkin (F) gate acts on three-bits and it is defined as follows, it performs a conditional swap on two of its inputs if the third input is set to 1. A gate library of F^3 gates is not universal for 3-in/out reversible circuits, since it can realize 6 circuits from the 40320 reversible circuits [15]. There are three possible F^3 gates for 3-in/out reversible circuits as shown in Fig. 5, that perform as follows:

$$\begin{aligned} F^3_{123} &: (x_1, x_2, x_3) \rightarrow (x_1, x_3, x_2) \equiv (6, 7), \\ F^3_{132} &: (x_1, x_2, x_3) \rightarrow (x_3, x_2, x_1) \equiv (4, 7), \\ F^3_{321} &: (x_1, x_2, x_3) \rightarrow (x_2, x_1, x_3) \equiv (4, 6). \end{aligned} \tag{5}$$

The Peres (P) gate acts on three-bits and it is defined as follows, it combines the function of T gate and C gate in a one gate. A gate library of P^3 gates is not universal for 3-in/out reversible circuits, since it can realize 5040 circuits from the 40320 reversible circuits [15].

Fig. 4 The 3 possible T^3 gates for 3-bit reversible circuits



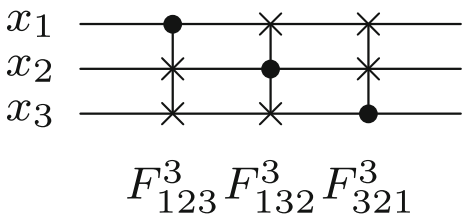


Fig. 5 The 3 possible F^3 gates for 3-bit reversible circuits

There are six possible P^3 gates for 3-in/out reversible circuits as shown in Fig. 6, that perform as follows:

$$\begin{aligned}
P^3_{23} &: (x_1, x_2, x_3) \rightarrow (x_1, x_2 \oplus x_1, x_3 \oplus x_1x_2) \equiv (5, 7, 6, 8),\\
P^3_{32} &: (x_1, x_2, x_3) \rightarrow (x_1, x_2 \oplus x_1x_3, x_3 \oplus x_1) \equiv (5, 6, 7, 8),\\
P^3_{13} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_2, x_2, x_3 \oplus x_1x_2) \equiv (3, 7, 4, 8),\\
P^3_{31} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_2x_3, x_2, x_3 \oplus x_2) \equiv (3, 4, 7, 8),\\
P^3_{12} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_3, x_2 \oplus x_1x_3, x_3) \equiv (2, 6, 4, 8),\\
P^3_{21} &: (x_1, x_2, x_3) \rightarrow (x_1 \oplus x_2x_3, x_2 \oplus x_3, x_3) \equiv (2, 4, 6, 8).
\end{aligned} \tag{6}$$

The (R^3) gate acts on three-bits and it is defined as follows, it combines the action of N, C and T^3 in a single gate. A gate library of R^3 gates is universal for 3-in/out reversible circuits, since it can realize all the 40320 reversible circuits [25]. There are six possible R^3 gates for 3-in/out reversible circuits as shown in Fig. 7, that perform as follows:

$$\begin{aligned}
R^3_{j,k,l} &: y_i = x_j \oplus x_k \oplus x_j \cdot x_l \oplus 1,\\
&\quad\ y_k = x_k \oplus x_j \cdot x_l \oplus 1,\\
&\quad\ y_l = x_l \oplus x_j,\\
R^3_{123} &: (x_1, x_2, x_3) \rightarrow (1, 7, 6, 5, 4, 2, 8, 3),\\
R^3_{321} &: (x_1, x_2, x_3) \rightarrow (1, 4, 6, 2, 7, 5, 8, 3),\\
R^3_{312} &: (x_1, x_2, x_3) \rightarrow (1, 4, 7, 3, 6, 5, 8, 2),\\
R^3_{132} &: (x_1, x_2, x_3) \rightarrow (1, 6, 7, 5, 4, 3, 8, 2),\\
R^3_{231} &: (x_1, x_2, x_3) \rightarrow (1, 6, 4, 2, 7, 3, 8, 5),\\
R^3_{213} &: (x_1, x_2, x_3) \rightarrow (1, 7, 4, 3, 6, 2, 8, 5).
\end{aligned} \tag{7}$$

where j,k and $l \in \{1, 2, 3\}$ in any order.

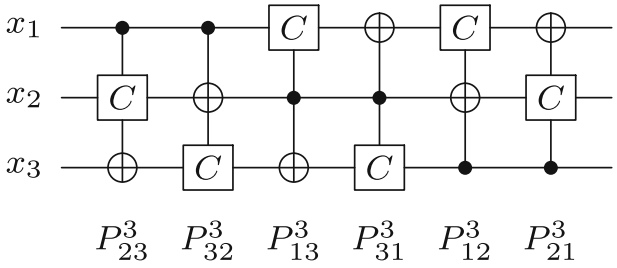


Fig. 6 The 6 possible P^3 gates for 3-bit reversible circuits

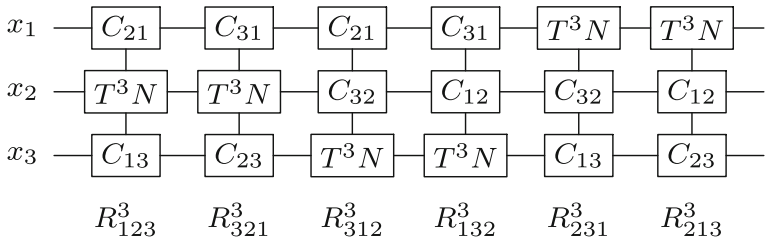


Fig. 7 The 6 possible R^3 gates for 3-bit reversible circuits

Many suggested universal reversible libraries consist of more than one type of gates such as NOT(*N*), Feynman(*C*), Toffoli(T^3), Fredkin(*F*) and Peres(*P*) gates. Different combinations of universal reversible libraries have been studied [12, 14, 17, 23]. For examples, there exist 6-universal reversible libraries *NCT*, *NCP*, *NCF*, *NCPT*, *NCTF* and *NCPF*. Recently some universal reversible libraries consist of one type of gate such as *G* gate and *R* gate have been proposed [15, 25].

3 The Proposed *M*-Gate Library

This section proposes a reversible *n*-bit gate M^n for *n*-bits input/output reversible circuits. The proposed *M*-gate is extendable according to the number of bits in the circuit design.

3.1 Single-Bit Gate

M^1 gate performs as *N* gate which inverts the input bit unconditionally. For 1-bit reversible circuits built using *M*-gate library, there is one M^1 gate with quantum cost equal zero as shown in Fig. 8, that perform as follows:

$$M^1_1 : (x_1) \rightarrow (x_1 \oplus 1) \equiv (1, 2). \tag{8}$$

3.2 Two-Bit Gate

M^2 gate performs as a combination of *N* gate and *C* gate. For 2-bit reversible circuits built using *M* gate library, there are two possible M^2 gates with quantum cost equal 1 as shown in Fig. 9, that perform as follows:

$$\begin{aligned} M^2_{i,j} &: y_i = x_i \oplus 1, \\ &\quad y_j = x_j \oplus y_i = x_j \oplus x_i \oplus 1, \\ M^2_{1,2} &: (x_1, x_2) \rightarrow (1, 4, 2, 3), \\ M^2_{2,1} &: (x_1, x_2) \rightarrow (1, 4, 3, 2). \end{aligned} \tag{9}$$

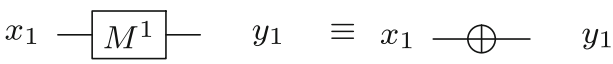


Fig. 8 The one possible M^1 gate for 1-bit reversible circuit

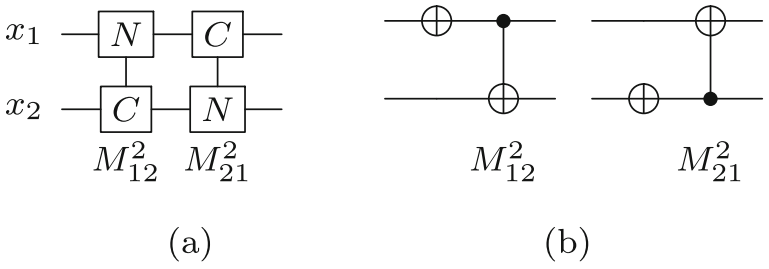


Fig. 9 The two possible M^2 gate for 2-bit reversible circuit

3.3 Three-Bit Gate

M^3 gate combines the action of the three gates N, C and T^3. It acts on an arbitrary 3-bits x_i, x_j and x_k in any order. For 3-bit reversible circuits built using M-gate library, there are six possible M^3 gates with quantum cost equal 5 as shown in Fig. 10, that perform as follows:

$$\begin{aligned}
M^3_{i,j,k} &: y_i = x_i \oplus (x_k \oplus x_j),\\
&\quad y_j = (x_j \oplus 1) \oplus (x_k \oplus x_j) \cdot (x_i \oplus (x_k \oplus x_j)),\\
&\quad y_k = x_k \oplus x_j,\\
M^3_{1,2,3} &: (x_1, x_2, x_3) \rightarrow (1, 3, 8, 5, 7, 2, 6, 4),\\
M^3_{1,3,2} &: (x_1, x_2, x_3) \rightarrow (1, 2, 8, 5, 6, 3, 7, 4),\\
M^3_{2,1,3} &: (x_1, x_2, x_3) \rightarrow (1, 5, 8, 3, 7, 2, 4, 6),\\
M^3_{2,3,1} &: (x_1, x_2, x_3) \rightarrow (1, 2, 8, 3, 4, 5, 7, 6),\\
M^3_{3,1,2} &: (x_1, x_2, x_3) \rightarrow (1, 5, 8, 2, 6, 3, 4, 7),\\
M^3_{3,2,1} &: (x_1, x_2, x_3) \rightarrow (1, 3, 8, 2, 4, 5, 6, 7).
\end{aligned} \tag{10}$$

where i,j and $k \in \{1, 2, 3\}$ in any order.

The quantum cost of the M^3_{123} gate is 4, Fig. 11 shows the decomposition of the gate. Figure 11a shows the gate representation of gate, Fig. 11b shows the four component gates of M^3_{123}, and Fig. 11c shows the representation of the M^3_{123} gate into its five elementary gates (one of them with cost zero). The optimization is done by applying new Toffoli decomposition techniques [24] and applying the moving rules in [22]. The first gate $[C_{23}v_{32}]$, which is merging gate between C_{23} and v_{32} in order, as shown in Fig. 12. To improve the

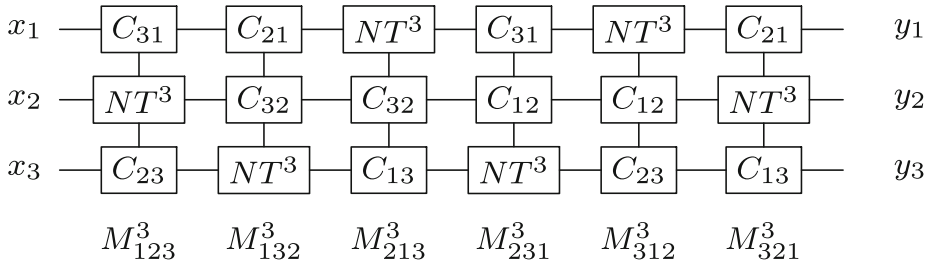


Fig. 10 The 6 possible M^3 gates for 3-bit reversible circuits

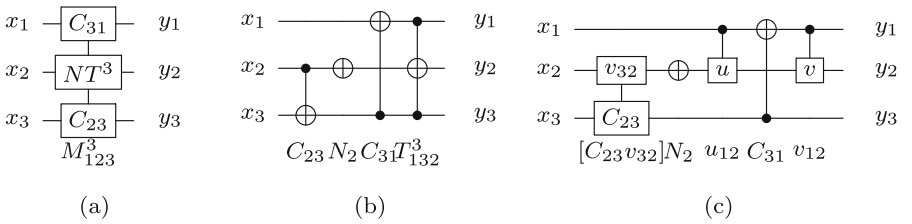


Fig. 11 The circuit representation for the decomposition of M^3_{123} gate, where: **a** The gate representation, **b** The decomposition of the M^3_{123} gate into its four components and **c** The optimized decomposition of M^3_{123} gate into its five elementary quantum gates

quantum cost of the circuits synthesized with M^3 gate, N gate added to form a new library called NM^3 which is also universal. The main NM^3 library consist of nine gates (generators) as shown in Figs. 13 and 14.

3.4 Four-Bit Gate

M^4 gate combines the action of the four gates N,C,T^3 and T^4. It acts on an arbitrary 4-bits x_i,x_j,x_k and x_l in any order. Figure 15 shows the decomposition of the gate, Fig. 15a shows the representation of the M^4_{1234}, and Fig. 15b shows the decomposition of the M^4_{1234} gate into its five components. There 24 gates are sufficient to realize the $(2^4)!$ reversible circuits. For 4-bits reversible circuits built using M-gate library, there are 24 possible M^4 gate, that perform as follows:

$$\begin{aligned} M^4_{i,j,k,l} : y_i &= x_i \oplus (x_k \oplus x_j),\\ y_j &= (x_j \oplus 1) \oplus (x_k \oplus x_j) \cdot (x_i \oplus (x_k \oplus x_j)),\\ y_k &= x_k \oplus x_j,\\ y_l &= x_l \oplus y_i \cdot y_j \cdot y_k, \end{aligned} \tag{11}$$

$$\begin{aligned} M^4_{1,2,3,4} &: (x_1, x_2, x_3, x_4) \rightarrow (1, 5, 16, 10, 14, 4, 12, 8, 2, 6, 15, 9, 13, 3, 11, 7),\\ M^4_{1,3,2,4} &: (x_1, x_2, x_3, x_4) \rightarrow (1, 3, 16, 10, 12, 6, 14, 8, 2, 4, 15, 9, 11, 5, 13, 7),\\ M^4_{2,1,3,4} &: (x_1, x_2, x_3, x_4) \rightarrow (1, 9, 16, 6, 14, 4, 8, 12, 2, 10, 15, 5, 13, 3, 7, 11),\\ M^4_{2,3,1,4} &: (x_1, x_2, x_3, x_4) \rightarrow (1, 3, 16, 6, 8, 10, 14, 12, 2, 4, 15, 5, 7, 9, 13, 11), \end{aligned}$$

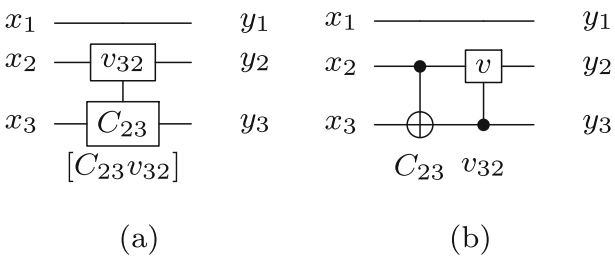


Fig. 12 The circuit representation for the decomposition of $[C_{23}v_{32}]$ gate [25], where: **a** The gate representation, and **b** The decomposition of the gate into its two component C_{23} gate and v_{32} gate

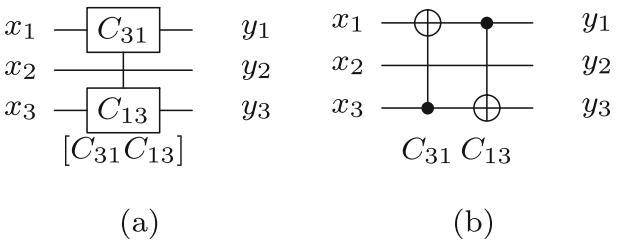


Fig. 13 The circuit representation for the decomposition of $[C_{31}C_{13}]$ gate [25], where: **a** The gate representation, and **b** The decomposition of the gate into its two component C_{13} gate and C_{31} gate

$$M^4_{3,1,2,4} : (x_1, x_2, x_3, x_4) \rightarrow (1, 9, 16, 4, 12, 6, 8, 14, 2, 10, 15, 3, 11, 5, 7, 13),$$
$$M^4_{3,2,1,4} : (x_1, x_2, x_3, x_4) \rightarrow (1, 5, 16, 4, 8, 10, 12, 14, 2, 6, 15, 3, 7, 9, 11, 13),$$
$$M^4_{1,2,4,3} : (x_1, x_2, x_3, x_4) \rightarrow (1, 5, 16, 11, 15, 4, 12, 8, 3, 7, 14, 9, 13, 2, 10, 6),$$
$$M^4_{1,3,4,2} : (x_1, x_2, x_3, x_4) \rightarrow (1, 3, 16, 13, 15, 6, 14, 8, 5, 7, 12, 9, 11, 2, 10, 4),$$
$$M^4_{2,1,4,3} : (x_1, x_2, x_3, x_4) \rightarrow (1, 9, 16, 7, 15, 4, 8, 12, 3, 11, 14, 5, 13, 2, 6, 10),$$
$$M^4_{2,3,4,1} : (x_1, x_2, x_3, x_4) \rightarrow (1, 3, 16, 13, 15, 10, 14, 12, 9, 11, 8, 5, 7, 2, 6, 4),$$
$$M^4_{3,1,4,2} : (x_1, x_2, x_3, x_4) \rightarrow (1, 9, 16, 7, 15, 6, 8, 14, 5, 13, 12, 3, 11, 2, 4, 10),$$
$$M^4_{3,2,4,1} : (x_1, x_2, x_3, x_4) \rightarrow (1, 5, 16, 11, 15, 10, 12, 14, 9, 13, 8, 3, 7, 2, 4, 6),$$
$$M^4_{1,4,2,3} : (x_1, x_2, x_3, x_4) \rightarrow (1, 2, 16, 11, 12, 7, 15, 8, 3, 4, 14, 9, 10, 5, 13, 6),$$
$$M^4_{1,4,3,2} : (x_1, x_2, x_3, x_4) \rightarrow (1, 2, 16, 13, 14, 7, 15, 8, 5, 6, 12, 9, 10, 3, 11, 4),$$
$$M^4_{2,4,1,3} : (x_1, x_2, x_3, x_4) \rightarrow (1, 2, 16, 7, 8, 11, 15, 12, 3, 4, 14, 5, 6, 9, 13, 10),$$
$$M^4_{2,4,3,1} : (x_1, x_2, x_3, x_4) \rightarrow (1, 2, 16, 13, 14, 11, 15, 12, 9, 10, 8, 5, 6, 3, 7, 4),$$
$$M^4_{3,4,1,2} : (x_1, x_2, x_3, x_4) \rightarrow (1, 2, 16, 7, 8, 13, 15, 14, 5, 6, 12, 3, 4, 9, 11, 10),$$
$$M^4_{3,4,2,1} : (x_1, x_2, x_3, x_4) \rightarrow (1, 2, 16, 11, 12, 13, 15, 14, 9, 10, 8, 3, 4, 5, 7, 6),$$
$$M^4_{4,1,2,3} : (x_1, x_2, x_3, x_4) \rightarrow (1, 9, 16, 4, 12, 7, 8, 15, 3, 11, 14, 2, 10, 5, 6, 13),$$
$$M^4_{4,1,3,2} : (x_1, x_2, x_3, x_4) \rightarrow (1, 9, 16, 6, 14, 7, 8, 15, 5, 13, 12, 2, 10, 3, 4, 11),$$
$$M^4_{4,2,1,3} : (x_1, x_2, x_3, x_4) \rightarrow (1, 5, 16, 4, 8, 11, 12, 15, 3, 7, 14, 2, 6, 9, 10, 13),$$
$$M^4_{4,2,3,1} : (x_1, x_2, x_3, x_4) \rightarrow (1, 5, 16, 10, 14, 11, 12, 15, 9, 13, 8, 2, 6, 3, 4, 7),$$

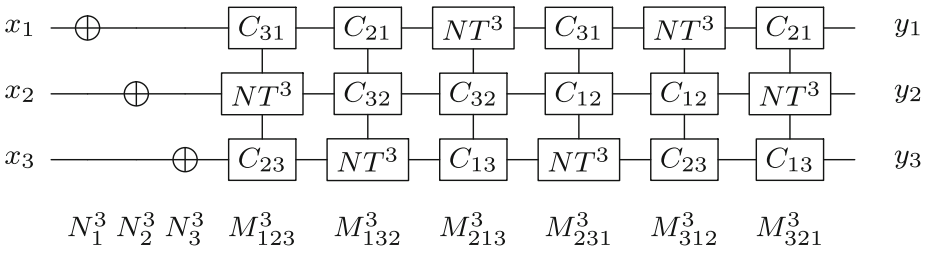


Fig. 14 The main NM^3 library consist of 9 gates (generators)

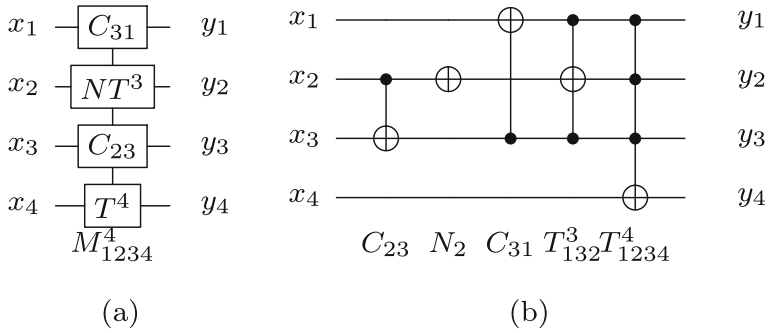


Fig. 15 The circuit representation for the decomposition of M^4_{1234} gate, where: **a** The gate representation, **b** The decomposition of the M^4_{1234} gate into its five components

$$M^4_{4,3,1,2} : (x_1, x_2, x_3, x_4) \rightarrow (1, 3, 16, 6, 8, 13, 14, 15, 5, 7, 12, 2, 4, 9, 10, 11),$$
$$M^4_{4,3,2,1} : (x_1, x_2, x_3, x_4) \rightarrow (1, 3, 16, 10, 12, 13, 14, 15, 9, 11, 8, 2, 4, 5, 6, 7).$$

where i,j,k and $l \in \{1, 2, 3, 4\}$ in any order.

3.5 *n*-Bit Gate

It can be shown using GAP that a permutation group with two generators M^2_{12} and M^2_{21} is of size 24, i.e. a cascade of these two gates are sufficient to implement any of the 24 2-in/out reversible circuits. It can be shown using GAP that a permutation group with the six generators of M^3 is of size 40320, i.e. a cascade of these six gates are sufficient to implement any of the 40320 3-in/out reversible circuits. Extending the M gate for n-bits is trivial as shown in Fig. 16. It can be shown using GAP that a permutation group with the $n!$ of M^n is of size $2^n!$, i.e. a cascade of these $n!$ gates are sufficient to implement any of the $2^n!$ n-in/out reversible circuits. The M^n gate is universal of n-bit gate.

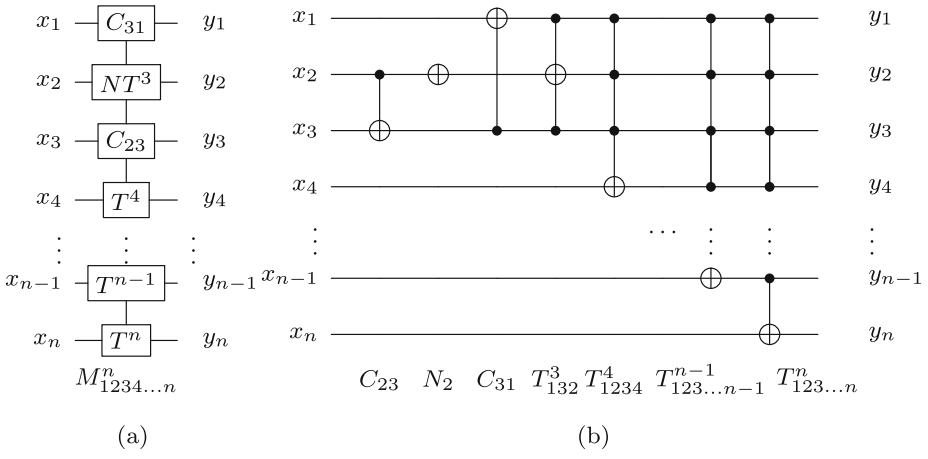


Fig. 16 The circuit representation for the decomposition of $M^n_{1234\ldots n}$ gate, where: **a** The gate representation, **b** The decomposition of the $M^n_{1234\ldots n}$ gate into its main components

For $n \geq 3$, M^n combines the action of the n-gate N,C,T^3,T^4,...,T^{n-1},T^n as shown in Fig. 16. The total number of possible gates for the general T^n is computed in [15] as follows:

$$n \sum_{r=0}^{n-1} \left(\frac{n-1}{r} \right) \tag{12}$$

where n is the number of bits and $r \geq 0$ is the number of controls per gate. There are $n!$ possible M^n gates which are sufficient to realize any n-bits reversible circuit, that perform as follows:

$$\begin{aligned}
M^n_{a_1,a_2,a_3,a_4,a_5,\ldots,a_{n-1},a_n} : y_{a_1} &= x_{a_1} \oplus (x_{a_3} \oplus x_{a_2}), \\
y_{a_2} &= (x_{a_2} \oplus 1) \oplus (x_{a_3} \oplus x_{a_2}) \cdot (x_{a_1} \oplus (x_{a_3} \oplus x_{a_2}), \\
y_{a_3} &= x_{a_3} \oplus x_{a_2}, \\
y_{a_4} &= x_{a_4} \oplus y_{a_1} \cdot y_{a_2} \cdot y_{a_3}, \\
y_{a_5} &= x_{a_5} \oplus y_{a_1} \cdot y_{a_2} \cdot y_{a_3} \cdot y_{a_4}, \\
&\ldots \\
&\ldots \\
y_{a_{n-1}} &= x_{a_{n-1}} \oplus y_{a_1} \cdot y_{a_2} \cdot y_{a_3} \cdot y_{a_4} \ldots y_{a_{n-2}}, \\
y_{a_n} &= x_{a_n} \oplus y_{a_1} \cdot y_{a_2} \cdot y_{a_3} \cdot y_{a_4} \cdot y_{a_5} \ldots y_{a_{n-1}},
\end{aligned} \tag{13}$$

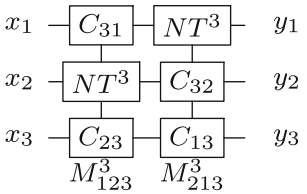
where a_1,a_2,a_3,... and $a_n \in \{1,2,3,\ldots,n\}$ in any order.

Algorithm 1 Generate all 3-bit reversible circuits.

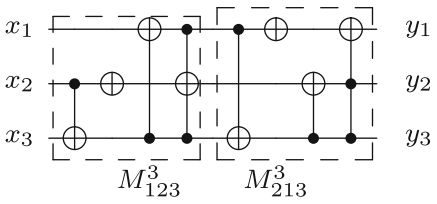
Input: X is the set of all sub libraries to be generated
and Y is the set of all specification for 3-in/out reversible circuits.
Output: $Circ$ is the set of all possible specifications to be represented as reversible circuits.

```
A ← length(X)
B ← length(Y)
for i ← 1 to A do
    for j ← 1 to B do
        if Specs[j] ∈ G[i] then
            Circ[i][j] = SchreierSims(G[i], Specs[j])
        else
            Circ[i][j] = []
        end if
    end for
end for
```

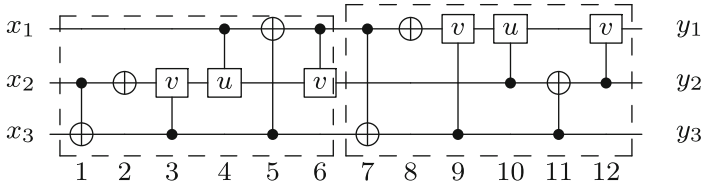
Given the proposed NM^3 gate library with nine generators as shown in Fig. 14 and the 40320 specifications for all 3-in/out reversible circuits. All sub-libraries of NM^3 gate library are generated, that is 511 sub-libraries after excluding the identity mapping. Using each sub-library to attempt to synthsize a reversible circuit for the 40320 specifications, if possible, using Schreier-Sims Algorithm. The term "if possible" here means that if a specification does not belong to the group generated by a sub-library, then it is impossible for this specification to be represented as a reversible circuit using this sub-library. The process



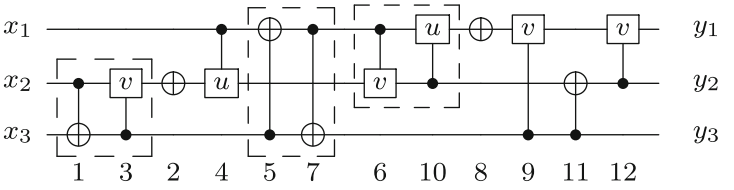
(a)



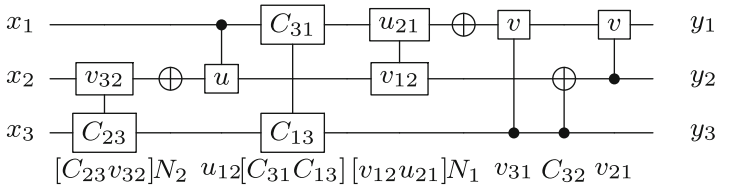
(b)



(c)



(d)



(e)

Fig. 17 **a** The circuit representation for [M^3_{123}, M^3_{213}], **b** Decompose the circuit into Toffoli gates, **c** Decompose the circuit into its elementary quantum gates, **d** Optimization is done by applying moving rules, **e** The optimized decomposition of the circuit[M^3_{123}, M^3_{213}] into its 9 elementary gates with QC equal 7

Table 1 Utilization of the different universal libraries

Lib	Lib size	Num of sub lib	Num of universal sub lib	Utilization
NT	6	64	4	6.250%
NP	9	512	333	65.039%
NCT	12	4096	1960	47.852%
NCF	12	4096	2460	60.059%
NCP	15	32768	26064	79.541%
NCTF	15	32768	23132	70.593%
NCPT	18	262144	217384	82.925%
NCPF	18	262144	220188	83.995%
G^3	6	64	51	79.688%
R^3	6	64	55	85.938%
M^3	6	64	55	85.938%
NR^3	9	512	340	66.406%
NM^3	9	512	475	92.773%

of synthesizing all possible 3-bit reversible circuits using the proposed NM^3 gate is shown in Algorithm 1.

4 Experimental Results

This section discusses and compares the performance of the proposed two gate libraries M^3 and NM^3, with the known libraries in [12–15, 18, 25]. It can be shown using GAP [17] that a permutation group of M^3 generators is of size 40320, thus the six generators in M^3 gate library are universal. There are 64 possible sub libraries from the main M^3 gate library, 55 of them are universal for the 3-bits reversible circuits. It can be shown using GAP [17] that a permutation group of NM^3 generators is of size 40320, thus the nine generators in NM^3 gate library are universal. There are 512 possible sub libraries from the main NM^3 gate library, 475 of them are universal for the 3-bits reversible circuits (Fig. 17).

Table 1 compares the utilization of the different libraries, it can be seen that the NM^3 gate library gives the utilization of 92.773%, which is better than the utilization of libraries *NT*, *NP*, *NCT*, *NCF*, *NCP*, *NCTF*, *NCPT*, *NCPF*, G^3, M^3, R^3 and NR^3. The size of the minimum universal sub libraries from the main M^3 gate library and NM^3 gate library

Table 2 Utilization of gates in the smallest universal sub libraries

Lib	Size of min universal sub lib	Num of universal sub lib	Num of universal sub lib with min size	Utilization
NT	5	6	3	50%
NP	3	84	18	21.429%
NCT	4	495	21	4.242%
NCF	4	495	60	12.121%
NCP	3	455	30	6.593%
NCTF	4	1365	105	7.692%
NCPT	3	816	36	4.412%
NCPF	3	816	42	5.147%
G^3	2	15	9	60%
R^3	2	15	13	86.667%
M^3	2	15	13	86.667%
NR^3	2	36	8	22.222%
NM^3	2	36	17	47.222%

Table 3 The proposed Rules of decomposing 3-bit M-reversible circuits

Rule No	Gate	Adjacent Gate	3-bit M-circuits decomposition	Quantum cost
R_1	M^3_{123}	M^3_{213}	$[C^3_{23}v^3_{32}]N^3_2u^3_{12}[C^3_{31}C^3_{13}][v^3_{12}u^3_{21}]N^3_1v^3_{31}C^3_{32}v^3_{21}$	7
R_2	M^3_{132}	M^3_{312}	$[C^3_{32}v^3_{23}]N^3_3u^3_{13}[C^3_{21}C^3_{12}][v^3_{13}v^3_{31}]N^3_1u^3_{21}C^3_{32}v^3_{21}$	7
R_3	M^3_{312}	M^3_{132}	$[C^3_{12}v^3_{21}]N^3_1u^3_{31}[C^3_{23}C^3_{32}][v^3_{31}u^3_{13}]N^3_3v^3_{23}C^3_{21}v^3_{13}$	7
R_4	M^3_{213}	M^3_{123}	$[C^3_{13}v^3_{31}]N^3_1u^3_{21}[C^3_{32}C^3_{23}][v^3_{21}u^3_{12}]N^3_2v^3_{32}C^3_{31}v^3_{12}$	7
R_5	M^3_{321}	M^3_{231}	$[C^3_{21}v^3_{12}]N^3_2u^3_{32}[C^3_{13}C^3_{31}][v^3_{32}u^3_{23}]N^3_3v^3_{13}C^3_{12}v^3_{23}$	7
R_6	M^3_{231}	M^3_{321}	$[C^3_{31}v^3_{13}]N^3_3u^3_{23}[C^3_{12}C^3_{21}][v^3_{23}u^3_{32}]N^3_2v^3_{12}C^3_{13}v^3_{32}$	7

is two. For M^3 gate library, there are 12 universal sub libraries of size two, such as $\{M^3_{123}, M^3_{213}\}$, $\{M^3_{132}, M^3_{231}\}$ and $\{M^3_{213}, M^3_{321}\}$. For NM^3 gate library, there are 16 universal sub libraries of size two, such as $\{M^3_{132}, M^3_{321}\}$, $\{M^3_{123}, M^3_{213}\}$ and $\{M^3_{231}, M^3_{312}\}$.

Table 2 compares the utilization of gates in the smallest universal sub libraries. The utilization of the universal sub libraries with minimum size for M^3 is 86.667%, while for NM^3 is 47.222%. It shows that NM^3 gives a utilization better than NP, NCT, NCF, NCP, $NCTF$, $NCPT$, $NCPF$ and NR^3. Table 4 compares the minimum length for the 3-bits reversible circuits using different libraries. It shows that the average minimum length for M^3 is 6.425, while for NM^3 the average minimum length is 5.325, which is better than NT,NCT,NCF,$NCTF$,G^3,R^3 and M^3 (Table 3).

Table 4 shows that the minimum length for M^3 is 6.42 and the minimum length for NM^3 is 5.32. These results are identical with the minimum length for R^3 and NR^3, but our results are different with the minimum quantum cost. For example, it can be shown using GAP [17] that a cyclic permutation equal (5, 8, 7, 6) can be realized by NR^3-based reversible circuit $[N^3_1, R^3_{231}, R^3_{123}, N^3_3, R^3_{231}, N^3_1]$ with minimum quantum cost equal 12 and minimum length equal 6 as shown in Fig. 18, while the same cyclic permutation equal (5, 8, 7, 6) can be realized by NM^3-based reversible circuit $[M^3_{231}, N^3_1, M^3_{123}, M^3_{213}, N^3_1, N^3_3]$ with minimum quantum cost equal 11 and minimum length equal 6 as shown in Fig. 19.

The optimization rules will be used to identify and classify similarity of gates among a circuit when decomposed to a sequence of quantum gates. Decomposition of 3-bit reversible circuits can be used to decrease the quantum cost. Optimization is done by removing and/or

Table 4 Minimum length of 3-bits reversible circuits using using the proposed M^3-gate library and the existing work in [25]

Min Len	NT	NP	NCT	NCP	$NCTF$	$NCPT$	$NCPF$	G^3	R^3	NR^3	M^3	NM^3
0	1	1	1	1	1	1	1	1	1	1	1	1
1	6	9	12	15	15	18	18	6	6	9	6	9
2	24	69	102	174	143	228	248	36	33	72	33	72
3	88	502	625	1528	1006	1993	2356	207	180	541	180	541
4	296	3060	2780	8968	5021	10503	12797	1097	960	3774	960	3774
5	870	13432	8921	23534	15083	23204	22794	4946	4686	18027	4686	18027
6	2262	21360	17049	6100	17261	4373	2106	13819	14611	17556	14611	17556
7	5097	1887	10253	0	1790	0	0	14824	15257	340	15257	340
8	9339	0	577	0	0	0	0	5208	4555	0	4555	0
9	12237	0	0	0	0	0	0	0	31	0	31	0
10	8363	0	0	0	0	0	0	0	0	0	0	0
11	1690	0	0	0	0	0	0	0	0	0	0	0
12	47	0	0	0	0	0	0	0	0	0	0	0
Avg Size	8.50 6	5.51 9	5.86 12	4.83 15	5.33 15	4.73 18	4.59 18	6.40 6	6.42 6	5.32 9	6.42 6	5.32 9

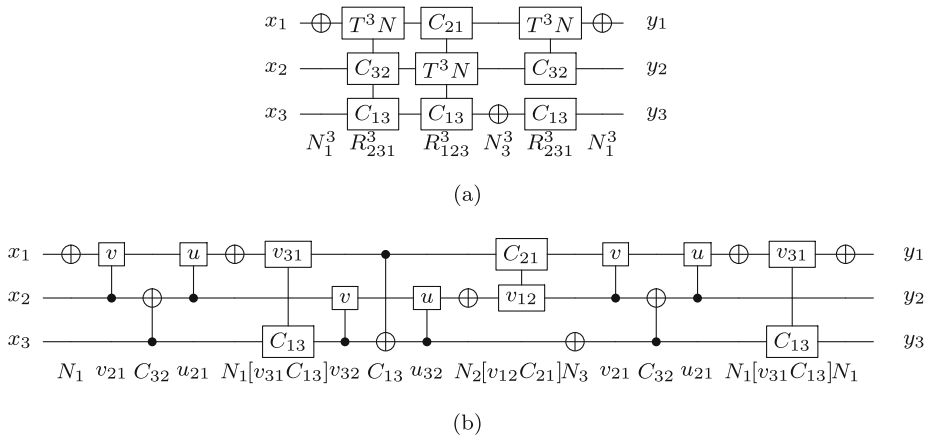


Fig. 18 The circuit representation for the cyclic permutation equal (5, 8, 7, 6), where: **a** The NR^3-based reversible circuit realize the cyclic permutation **b** The optimized decomposition of the NR^3-based reversible circuit into its 18 elementary quantum gates with QC equal 12

combing (merging) adjacent gates act on same qubit [23] and applying new decomposition techniques defined in [24]. For example, the cost of the sequence of reversible gates $[M^3_{123}, M^3_{213}]$ is 7 instead of 8 as shown in Fig. 17. The first gate is $[C_{23}v_{32}]$, which is merging gate between C_{23} and v_{32} in order, as shown in Fig. 12. The fourth gate is$[C_{31}C_{13}]$, which is merging gate between C_{31} and C_{13} in order, as shown in Fig. 13. Applying the novel optimization rules as shown in Table 3 to reduce the quantum cost of 3-bit reversible circuits built using M^3 gate library.

The quantum cost of all the 40320 3-bit reversible circuits synthesized by the M^3 and NM^3 gate libraries are calculated and compared with different universal libraries as shown in Table 5. For 3-bits reversible circuits built using M^3-gate library, the maximum quantum cost is 36 and average quantum cost is 25.70 before optimization. After adding the N gate

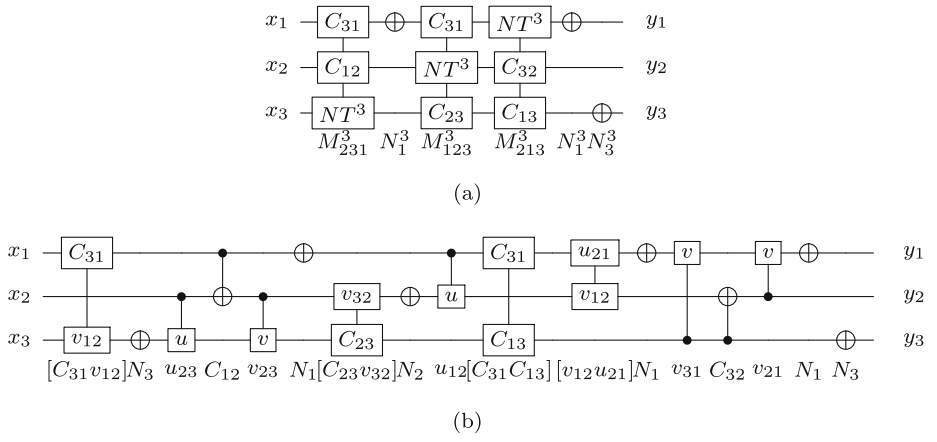


Fig. 19 The circuit representation for the cyclic permutation equal (5, 8, 7, 6), where: **a** The NM^3-based reversible circuit realize the cyclic permutation **b** The optimized decomposition of the NM^3-based reversible circuit into its 17 elementary quantum gates with QC equal 11

Table 5 Minimum cost of 3-bits reversible circuits using the proposed M^3-gate library and the existing work in [25]

Min Cost	Spc# R^3	Spc# M^3	Spc# *NT*	Spc# *NT* aft optm	Spc# NR^3	Spc# NR^3 aft optm	Spc# NM^3	Spc# NM^3 aft optm
0	1	1	8	8	8	8	8	8
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	6	6	0	0	192	192	192	192
5	0	0	96	94	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	851	0	2136
8	33	33	0	16	3442	2591	3436	1300
9	0	0	0	340	0	0	0	0
10	0	0	648	288	0	636	0	0
11	0	0	0	32	0	6050	0	11916
12	180	180	0	179	16040	9354	15980	4064
13	0	0	0	790	0	396	0	0
14	0	0	0	1487	0	2829	0	3294
15	0	0	2694	324	0	7175	0	7242
16	960	960	0	574	16676	6331	16673	6137
17	0	0	0	2052	0	344	0	0
18	0	0	0	3616	0	1200	0	1117
19	0	0	0	1462	0	1278	0	1484
20	4686	4686	7640	1041	3928	1053	3988	1387
21	0	0	0	3405	0	9	0	0
22	0	0	0	5357	0	14	0	0
23	0	0	0	2894	0	2	0	0
24	14611	14611	0	1435	34	7	43	43
25	0	0	12881	3191	0	0	0	0
26	0	0	0	4369	0	0	0	0
27	0	0	0	2436	0	0	0	0
28	15257	15257	0	806	0	0	0	0
29	0	0	0	1444	0	0	0	0
30	0	0	11502	1482	0	0	0	0
31	0	0	0	761	0	0	0	0
32	4555	4555	0	125	0	0	0	0
33	0	0	0	126	0	0	0	0
34	0	0	0	109	0	0	0	0
35	0	0	4489	60	0	0	0	0
36	31	31	0	6	0	0	0	0
37	0	0	0	0	0	0	0	0
Min Cost	Spc# R^3	Spc# M^3	Spc# *NT*	Spc# *NT* aft optm	Spc# NR^3	Spc# NR^3 aft optm	Spc# NM^3	Spc# NM^3 aft optm
38	0	0	0	0	0	0	0	0
39	0	0	0	0	0	0	0	0
40	0	0	362	0	0	0	0	0
Avg	25.70	25.70	22.77	22.32	14.06	13.39	14.07	13.29

to the M^3-gate library, the maximum quantum quantum cost has been reduced to 24, having an average cost 13.29 after apply optimization rules are shown in Table 3, giving 48.3% of improvement. The quantum cost of the circuits built using NR^3-gate library have improved

by 44.1% and the quantum cost of the circuits built using *NT*-gate library have improved by 13.4% [25].

5 Conclusion

The paper proposed a novel reversible *n*-bit gate that is proved to be universal for synthesizing reversible circuits using the algebraic software GAP. The proposed gate is extendable according to the number of bits in the circuit design and is important as it a single type of gate and using this technology might be cheaper to implement. All experimental results shown in this paper have been obtained using GAP. For 3-bits reversible circuits built using the proposed M^3-gate library, it shown that:

- The average minimum quantum cost for reversible circuits based on M^3 library is 25.70 with minimum length is 6.403.
- The average minimum quantum cost for reversible circuits based on NM^3 library is **13.29** with the minimum length is 5.325. (adding the *N* gate to the M^3-gate library giving 48.3% of improvment).

The reversible circuits based on NM^3 library give better results than that the reversible circuits based on NR^3 library and NT^3 library with respect to the quantum cost. The reversible circuits based on NM^3 library give the utilization of **92.773**%, which is better than the utilization of different libraries achieved by other in the literature. The analysis of universal sub libraries for the proposed gate to find the optimal sub library with exact minimal number of gates that generate an efficient quantum circuit is an extension to this work.

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