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Novel Efficient Circuit Design for Multilayer QCA RCA

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Abstract
The novel emerging technology, QCA technology, is a candidate for replacing CMOS technology. Full Adder (FA) circuits are also widely used circuits in arithmetic circuits design. In this paper, two new multilayer QCA architectures are presented: one-bit FA and 4-bit Ripple Carry Adder (RCA). The designed one-bit multilayer FA architecture is based on a new XOR gate architecture. The designed 4-bit multilayer QCA RCA is also developed based on the designed one-bit multilayer QCA FA. The functionality of the designed architectures are verified using QCADesigner tool. The results indicate that the designed architecture for 4-bit multilayer QCA RCA requires 5 clock phases, 125 QCA cells, and 0.17 μm^2 area. The comparison results confirm that the designed architectures provide improvements compared with other adder architectures in terms of cost, cell count, and area.

Keywords Ripple carry adder · Full adder · Quantum-dot cellular automata · Multilayer design, XOR gate

1 Introduction

The novel technology, Quantum-dot Cellular Automata (QCA) technology, is a new emerging technology, which is utilized to achieve higher speed and scaling compared to CMOS technology [1]. Logic states are encoded according to the positions of electrons in this technology [2, 3]. The XOR gate, majority gate and inverter gate are typical logic gates in the QCA technology [4, 5]. Using these QCA gates, the logic circuits can be constructed [6]. The logic circuits in this technology can be implemented in coplanar or multilayer.

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On the other hand, Full Adder (FA) circuits are widely used circuits for implementation of complex logic circuits such as Arithmetic Logic Units (ALU) [6, 7]. As a result, the implementation of high-performance FA circuits has a great deal of attention. So, many researchers designed FA circuits to increase the efficiency of FA circuit in this technology [8–12]. Balali et al. [8] have designed one-bit QCA FA architecture using a new XOR gate, which requires $0.02\mu m^2$ area and 29 cells. Mohamadi et al. [9] have developed multilayer one-bit FA architecture that requires $0.02\mu m^2$ area and 38 cells. Roohi et al. [10] have developed multilayer one-bit QCA FA architecture that requires $0.01\mu m^2$ area and 23 cells. Navi et al. [11] have developed one-bit QCA FA, which requires $0.04\mu m^2$ area and 73 cells. Hashemi et al. [12] have proposed multilayer one-bit QCA FA, which requires $0.05\mu m^2$ area and 79 cells.

We develop a novel QCA XOR gate architecture in this paper and use this novel QCA XOR gate in sum structure for construct a multilayer one-bit QCA FA. Moreover, the novel robust efficient multilayer 4-bit QCA Ripple Carry Adder (RCA) architecture is developed using the designed one-bit QCA FA architecture. The functionality of the designed architectures are verified using QCADesigner tool version 2.0.3. The achieved results demonstrated that the developed architectures provide improvements compared to other QCA architectures in terms of delay time, and area.

The remainder of this study is arranged as follows. In section 2, the background of the QCA technology is presented. The developed architectures are demonstrated in section 3. The simulation results and comparison of the developed architectures are described in section 4, and finally, this study is concluded in section 5.

2 Background

2.1 QCA Cell

Logic design using quantum cells is one of the most recent trends, which allows the scaling is continued to atomistic dimensions [8, 13]. In the QCA technology, quantum cells are arranged to define the logic. Quantum cells are composed of 4 dots and 2 electrons that are arranged in a square. These 2 electrons can tunnel between these 4 dots [3, 5, 13, 14]. Based on coulomb repulsion, two electrons always take up the diagonal positions as shown in Fig. 1.

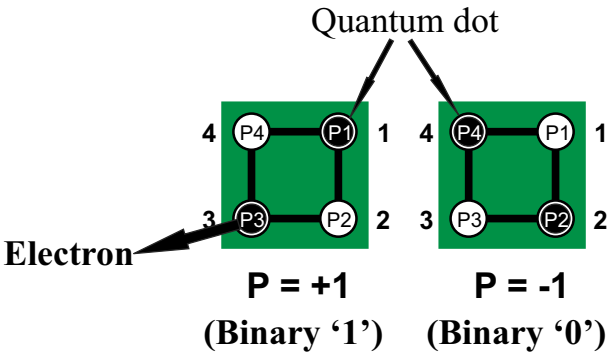

Fig. 1 The QCA cell structure [3, 14, 15]

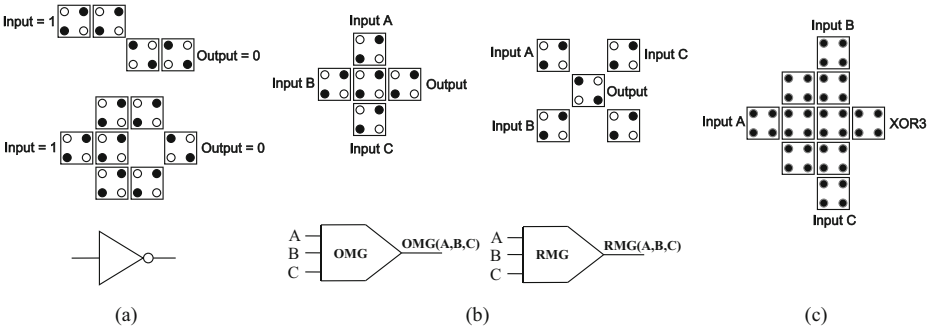

Fig. 2 QCA gates (**a**) two inverter gates, **b** two three-input majority gates and **c** 3-input XOR gate [3–5, 8, 13]

The positions of 2 electrons inside the cell determines the binary levels [3, 8, 13, 15]. The state of the cell is shown by polarization P that is computed as follows.

$$P = \frac{(p_1 + p_3) - (p_2 + p_4)}{p_1 + p_2 + p_3 + p_4} \tag{1}$$

In this technology, P = -1 is utilized to show state "0" and P = +1 is utilized to show state "1" [3, 8, 13, 15].

2.2 QCA Gates

QCA architectures are created based on three basic gates: The inverter gate, majority gate and XOR gate. Figure 2 shows the QCA majority gate, inverter gate, and XOR gate [3, 4, 8].

The output of majority gate is shown as follows [3, 4, 14, 16]:

$$M\,(A, B, C) = CA + BA + BC \tag{2}$$

Where A, B and C denote the inputs of this gate.

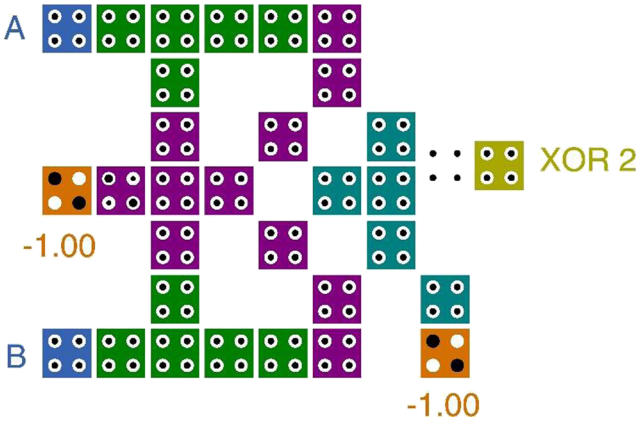

Fig. 3 The utilized two inputs QCA XOR gate in [19]

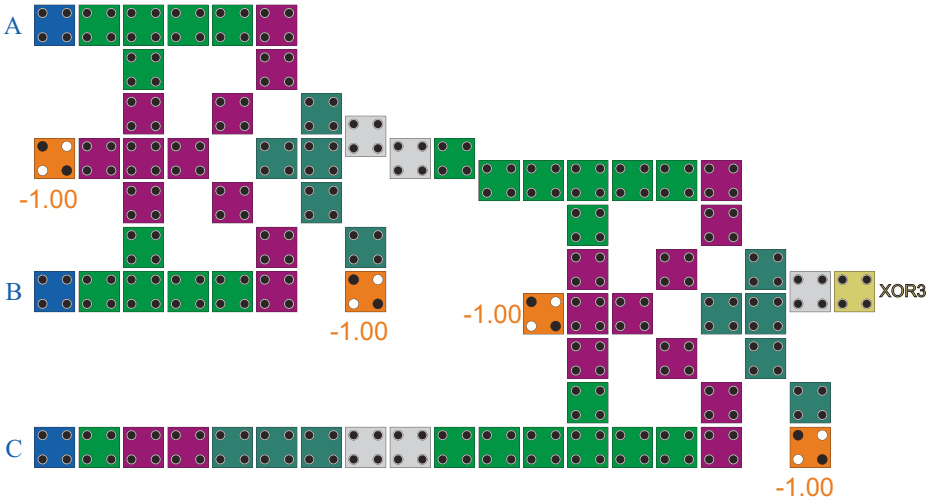

Fig. 4 The utilized three inputs XOR gate in [17]

The OR and AND gates are constructed by fixing one input of this gate to 1 or 0, respectively. The XOR gate is also a widely used logic gate in digital architectures design. The output of XOR gate is computed as follows [4, 8, 17]:

$$XOR\ (A, B, C) = A \oplus B \oplus C \tag{3}$$

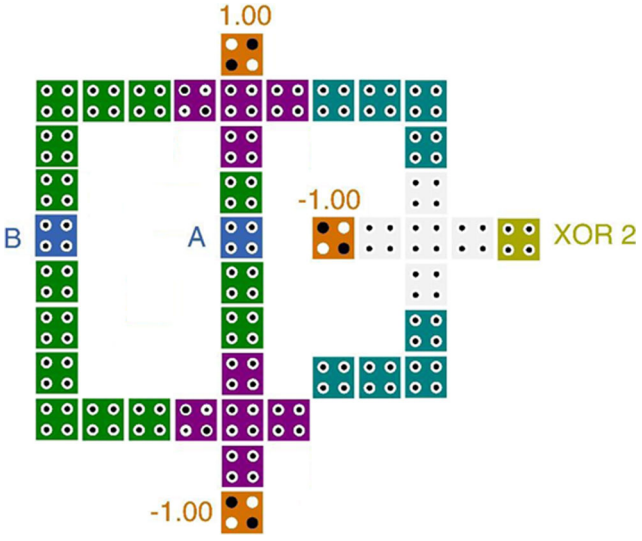

Fig. 5 The two inputs XOR gate in [20]

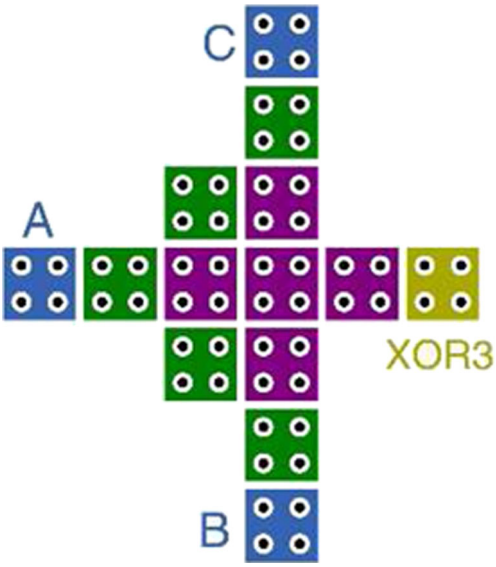

Fig. 6 The utilized QCA XOR gate in [17]

2.3 Full Adder

A one-bit QCA FA is an architecture that can add three one-bit inputs. Suppose that A, B and C_{in} are three inputs of the FA, the sum, and carry output for the one-bit QCA FA are computed as follows [6–8]:

$$S = A \oplus B \oplus C_{in} \tag{4}$$

$$C_{out} = AB + AC_{in} + BC_{in} \tag{5}$$

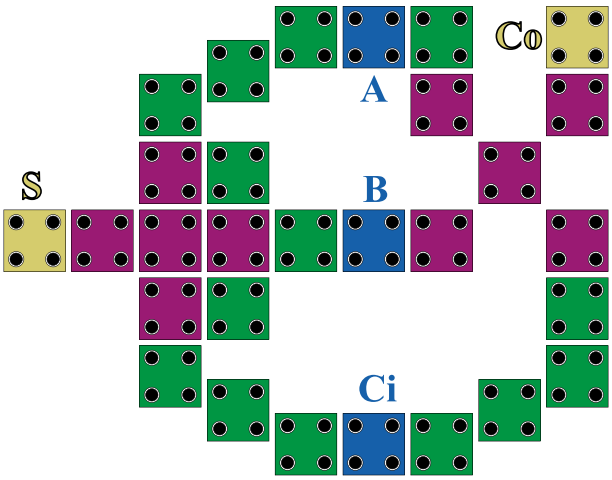

Fig. 7 The utilized QCA FA in [8]

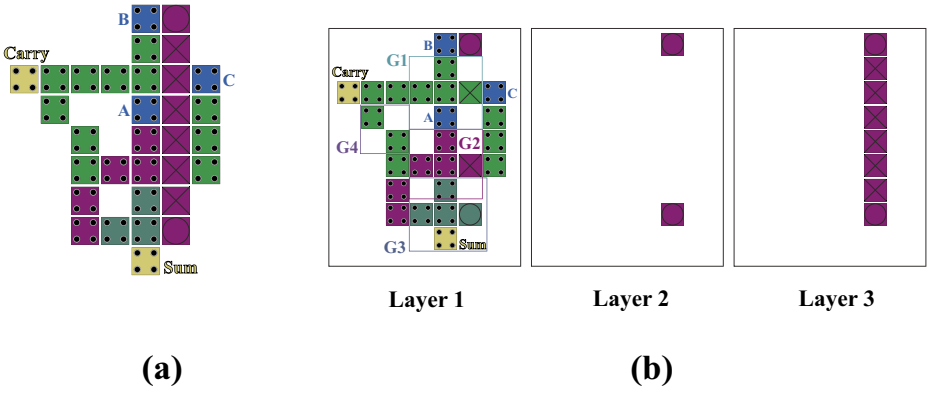

Fig. 8 Multilayer one-bit QCA FA in [9] (**a**) layout, **b** layers

The expression for C_{out} can be reformulated in the QCA technology as follows [8, 18]:

$$C_{out} = M\ (A, B, C_{in}) \tag{6}$$

As a result, the adder architectures are implemented using XOR gate and majority gate [8].

2.4 Related QCA Works

In this section, we review and compare the related articles in two main parts.

2.4.1 QCA XOR Gate

Sheikhfaal et al. [19] have designed a QCA XOR gate, which has two inputs. It is constructed based on QCA primary gates, which is shown in Fig. 3. It has four clock phases latency and consists of 32 cells with $0.02\mu m^2$area.

Ahmad et al. [17] have developed a three inputs QCA XOR gate by connecting two inputs XOR gates, which is shown in Fig. 4.

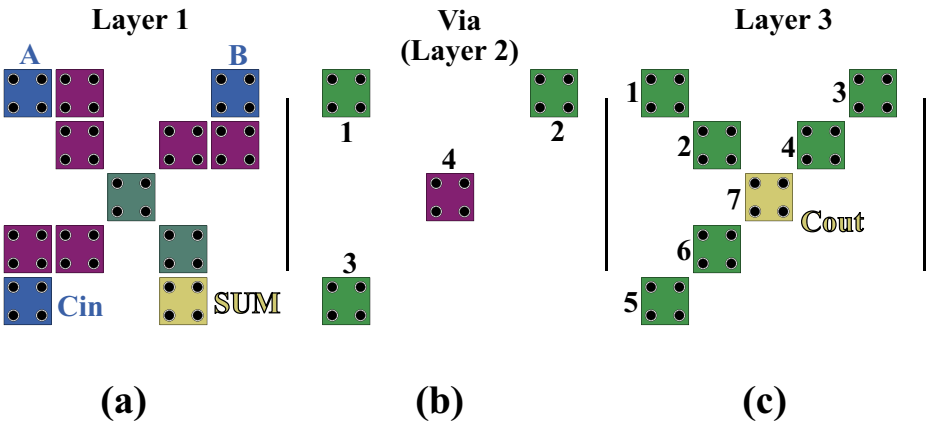

Fig. 9 The utilized one-bit QCA FA in [10], **a** sum generator architecture, **b** via layer, **c** carry generator architecture

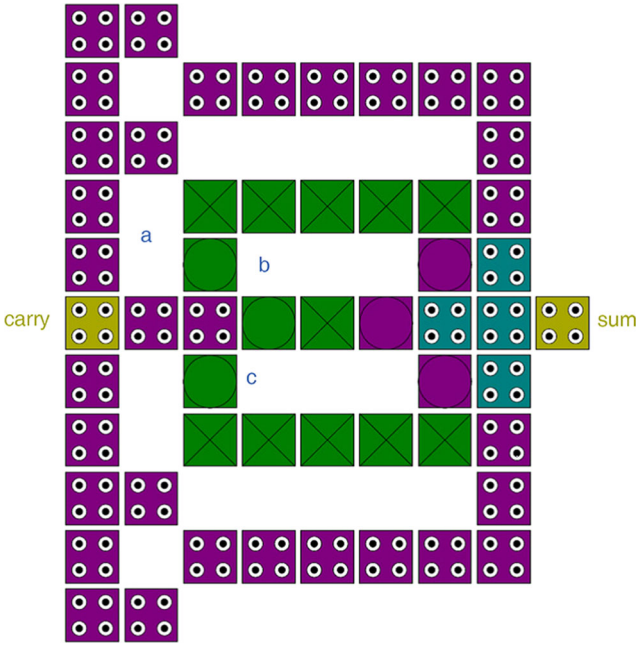

Fig. 10 The utilized multilayer one-bit QCA FA in [11]

This design has eight clock phases latency and contains 75 cells with $0.08\mu m^2$area. Mustafa and Beigh [20] have developed a 2-input XOR gate, which is illustrated in Fig. 5.

This design is implemented with 44 cells and it requires $0.07\mu m^2$area . It has latency of four clock phases.

Ahmad et al. [17] have also presented a three inputs QCA XOR gate. Figure 6 shows this design.

This gate requires area of $0.02\mu m^2$ and 14 cells. It has latency of two clock phases. However, these XOR gates are suitable, but the performance of the XOR gates can be improved as described in this paper.

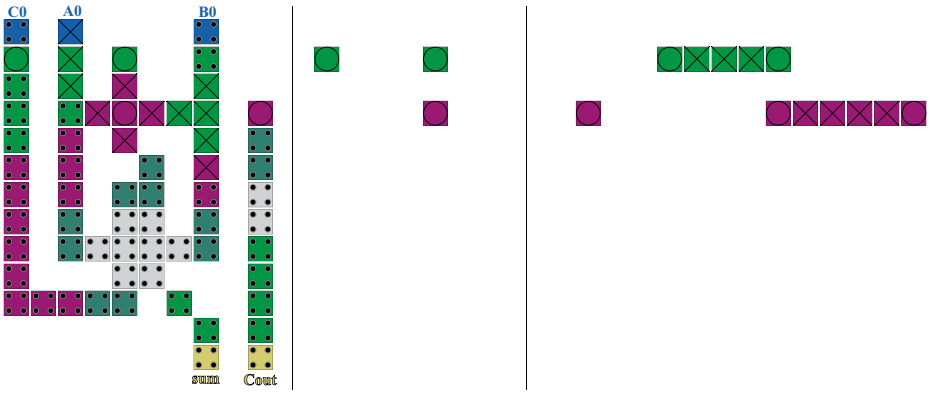

Fig. 11 The utilized QCA FA in [12] (**a**) first layer, **b** via layer, **c** crossover cells

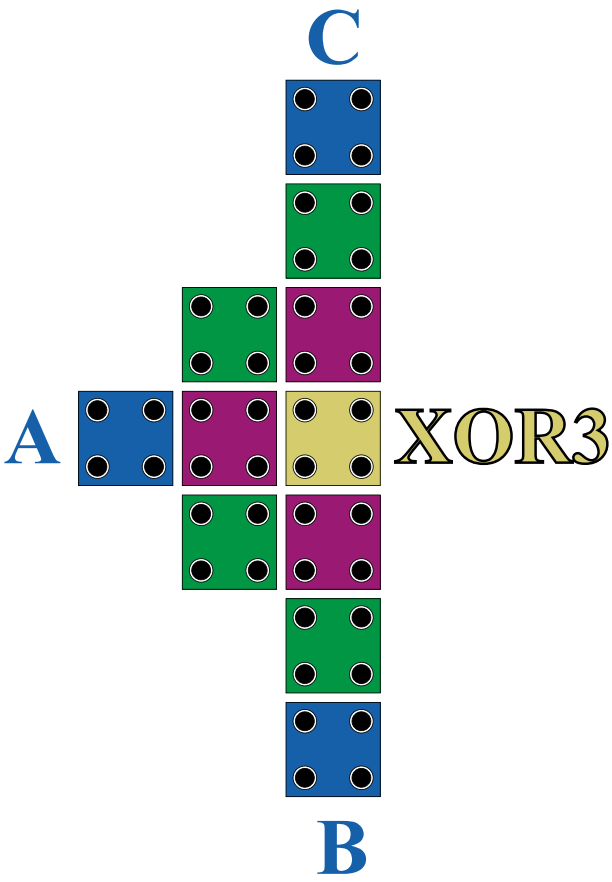

Fig. 12 The designed three inputs QCA XOR gate

2.4.2 The One-Bit QCA FA

Balali et al. [8] have designed one-bit QCA FA, which is shown in Fig. 7. They enhanced three inputs QCA XOR by employing half distance in XOR gate. This FA architecture is requires $0.02\mu m^2$ area and 29 cells. It also has latency of two clock phases.

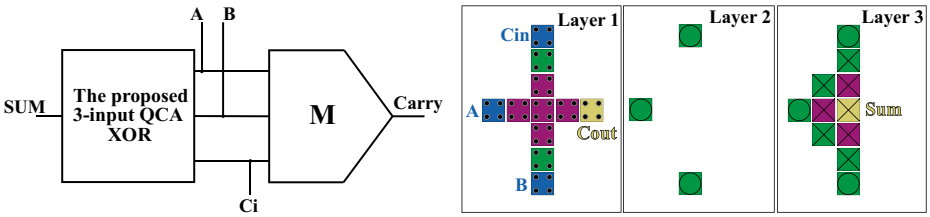

Fig. 13 The designed multilayer one-bit QCA FA (**a**) logic diagram, **b** three layers

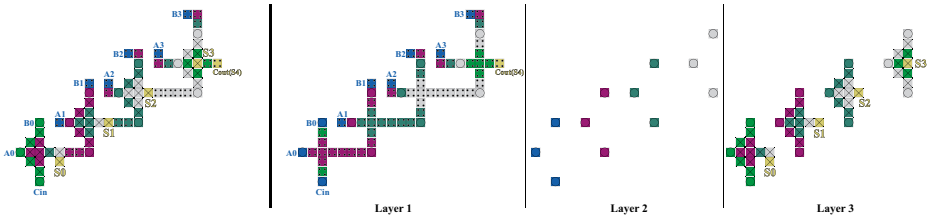

Fig. 14 The designed 4-bit RCA, **a** QCA layout, **b** three layers

Mohammadi et al. [9] have developed a multilayer one-bit QCA FA that is illustrated in Fig. 8.

In this FA, 38 cells are used with area of $0.02\mu m^2$ and latency of 3 clock phases.

The authors of [10] used MG with control cell to develop one-bit QCA FA. Figure 9 illustrates this design in three layers.

The number of cells in the utilized architecture in [10] is 23.The required area is $0.01\mu m^2$ and the latency is 3 clock phases. The designed multilayer one-bit QCA FA in [11] is illustrated in Fig. 10. This FA requires $0.04\mu m^2$ area, and 73 cells. It also has 3 clock phases latency.

Hashemi et al. [12] have developed a multilayer one-bit QCA FA. Figure 11 depicts this architecture.

This FA requires 0.05 μm^2 area and 79 cells. It also has 5 clock phases latency. Although, these QCA FA architectures are suitable, the performance of these architectures can be improved as described in the next section.

3 The Designed Architectures

We design a new three inputs QCA XOR gate in this section, then, we design an efficient multilayer one-bit QCA FA architecture based on this new QCA XOR gate. In addition, a novel multilayer 4-bit QCA RCA architecture is developed using the designed multilayer QCA FA.

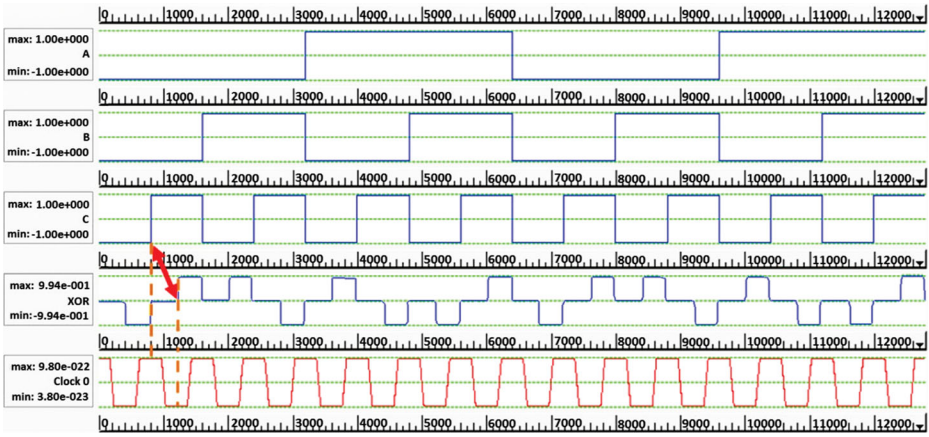

Fig. 15 The simulation result of the developed 3-input QCA XOR gate

Table 1 Comparison table for 3-input QCA XOR gate

Ref.	Cell count	Area (μm^2)	Latency(clock phase)	Cost
[17] (Design 1)	75	0.08	8	0.64
[17] (Design 2)	14	0.02	2	0.04
[8]	14	0.01	2	0.02
This paper	11	0.01	2	0.02

3.1 The Designed Three Inputs QCA XOR Gate

Figure 12 illustrates the designed novel 3-input QCA XOR gate.

The architecture of the designed QCA XOR gate requires 0.01 μm^2(=8004nm^2) area and 11 cells.

3.2 The Designed Multilayer One-Bit QCA FA Architecture

Figure 13 depicts the designed multilayer one-bit QCA FA.

This FA is developed in two layers and one via layer. The output Sum is designed in third layer and the output carry, Cout, is designed in first layer. The proposed architecture requires 0.01 μm^2 area and 25 cells.

3.3 The Designed Multilayer 4-Bit RCA

The developed multilayer 4-bit RCA is displayed in Fig. 14.

The designed novel multilayer 4-bit RCA is based on the designed multilayer one-bit QCA FA architecture. It requires 0.17μm^2(=171545nm^2) area and 125 cells.

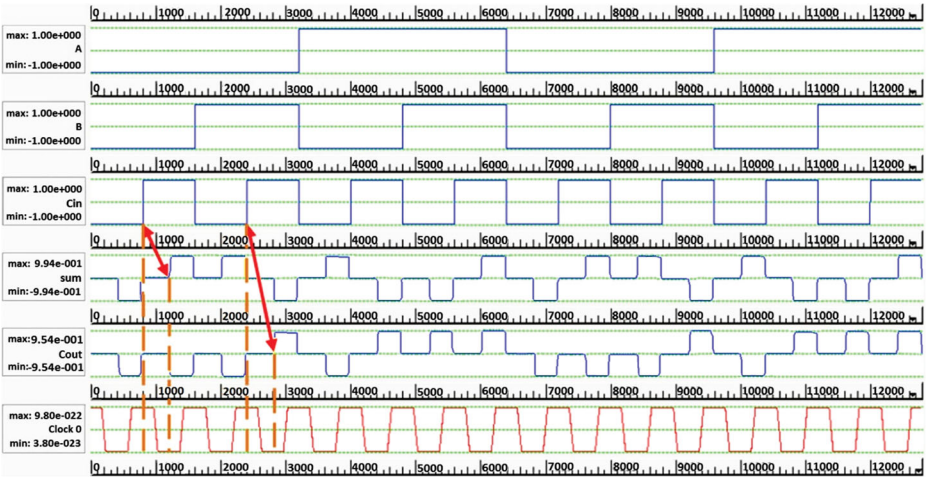

Fig. 16 The simulation results of the developed QCA FA

Table 2 Comparison table for one-bit FA

Ref.	Cell count	Area (μm^2)	Latency(clock phase)	Cost
[12]	79	0.05	5	0.25
[11]	73	0.04	3	0.12
[10]	23	0.01	3	0.03
[9]	38	0.02	3	0.06
[8]	29	0.02	2	0.04
This paper	25	0.01	2	0.02

4 Simulation Results and Comparison

The results of the developed architectures are presented and compared with previous architectures in this section. The cost is determined as follows:

$$Cost = Area \times Latency \tag{7}$$

Where latency is determined based on clock phase and area is calculated based on μm^2.

4.1 The Developed Three Inputs QCA XOR Gate

Figure 15 illustrates the simulation results of the developed three-input XOR gate.

These results confirm the accuracy of the functionality of the designed three-input QCA XOR gate. The latency of the developed three inputs QCA XOR gate is two clock phases. Table 1 compares the developed three-input XOR gate with XOR gates in [8, 17].

Based on Table 1, our designed 3-input QCA XOR gate has improvements in terms of cost, cell count, and area in comparison with other QCA XOR gate architectures in [8, 17]. For instant, it has 97%, 85%, 87%, and 75% improvements in terms of cost, cell count, area, and latency, respectively, in comparison with [17] (design 1). It also has 50%, 50%, and 21.4% improvements in terms of cost, area and cell count, respectively, in comparison with [17] (design 2).

4.2 The Developed Multilayer QCA FA

Figure 16 depicts the simulation results of the designed multilayer QCA FA.

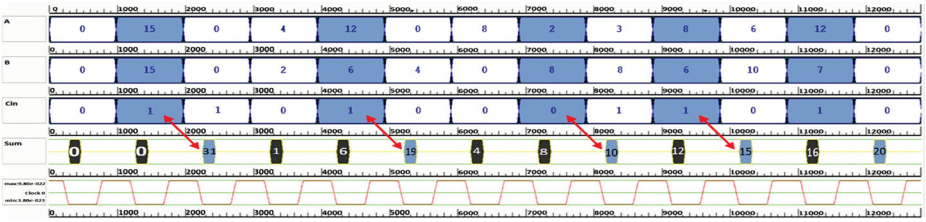

Fig. 17 The simulation results of the designed multilayer 4-bit QCA RCA

Table 3 Comparison table for 4-bit QCA RCA

Ref.	Cell count	Area (μm^2)	Latency (clock phase)	Cost
[12]	308	0.29	8	2.32
[10]	165	0.20	8	1.6
[9]	237	0.24	6	1.44
[8]	269	0.37	8	2.96
This paper	125	0.17	5	0.85

The results confirm the correctness of the designed multilayer QCA FA. In addition, the latency of the designed multilayer one-bit QCA FA is 2 clock phases.

The simulation results of the developed multilayer QCA FA and the multilayer QCA FA architectures in [8–12] are summarized in Table 2.

Based on achieved results, which are illustrated in Table 2, our developed multilayer QCA FA has advantages in terms of cost, area, and cell count compared with other multilayer QCA FA architectures in [8–12]. For instant, it has 80%, 68%, 92%, and 60% improvements in terms of area, cell count, cost and latency, respectively, in comparison to [12]. It also has 50%, 50% and 13.7% improvements in terms of cost, area, and cell count, respectively, in comparison with [8].

4.3 The Designed Multilayer 4-Bit QCA RCA

Figure 17 displays the simulation results of the designed multilayer 4-bit RCA.

According to Fig. 17, C_{out} is calculated as S_4. In addition, the results confirm the correctness of the designed multilayer 4-bit QCA RCA. The latency of the designed multilayer 4-bit QCA RCA is 5 clock phases. Table 3 compares the developed multilayer 4-bit RCA with other architectures.

According to simulation results, which are summarized in Table 3, our developed architecture has improvements in terms of area, cell count, cost and latency compared to other multilayer 4-bit QCA RCA architectures in [8–10, 12]. For instant, it has 54%, 53.5%, 71.2% and 37.5% improvements in terms of area, cell count, cost and latency, respectively, in comparison to [8]. It also has 15%, 24.2%, 46.8% and 37.5% improvements in terms of cell count, area, latency and cost, respectively, in comparison with [10].

5 Conclusions

The QCA technology is a new technology for high-speed and dense architectures design. The FA is also a widely used architecture in computer arithmetic architecture design [1–6]. A new QCA XOR gate was developed in this paper. Then, an efficient one-bit QCA FA was designed based on the developed three inputs QCA XOR gate. In addition, a 4-bit RCA architecture was developed based on this new one-bit QCA FA as structural unit. The developed architectures were simulated in QCADesigner tools version 2.0.3. Based on our simulation results, the developed architecture for 4-bit multilayer QCA RCA has 125 QCA cells, 0.17 μm^2 area, and 5 clock phases. Based on our comparison results, our designed 3-input QCA XOR gate, multilayer one-bit QCA FA architecture and multilayer 4-bit QCA RCA architecture have improvements in terms of area, cost, and cell count compared to other architectures. Therefore, the designed multilayer 4-bit QCA architecture has a huge potential to become an efficient architecture for implementing QCA RCA architectures.

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