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A Novel Adder Circuit Design in Quantum-Dot Cellular Automata Technology

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Abstract
Quantum-dot Cell Automata (QCA) technology is a promising alternative technology for CMOS technology. In this technology, the ultra-dense and low-latency digital circuits are designed. One of the important digital circuits is Full Adder (FA). In this paper, a new and efficient multilayer QCA full adder circuit is designed and evaluated. In the designed full adder circuit, sum and carry output are designed in separated layers. Then, a novel and efficient 4-bit Ripple Carry Adder (RCA) circuit is designed based on this new FA circuit. The proposed QCA circuits are simulated using QCADesigner tool version 2.0.3. The simulation results show that the proposed 4-bit QCA RCA requires 135 QCA cells, 0.06 μm^2 area and 5 clock phases. The comparison shows that the proposed QCA circuits have advantages compared to other QCA circuits in terms of area, latency, and cost.

Keywords Quantum-dot cell automata · Efficient full adder · Ripple carry adder · QCADesigner, 3-input XOR gate · Multilayer

1 Introduction

The CMOS technology as the dominant technology for VLSI has faced with limitations at nano-scale such as short channel effects [1]. So, alternative technologies such as Silicon On Insulator (SOI) [2–8], Carbon NanoTube Field Effect Transistors (CNTFETs) [9–13], molecular devices [14], single electron transistors [15], Spintronics [16] and Quantum-dot Cellular Automata (QCA) [17–19] are proposed for circuits design at nano-scale.

The QCA technology could be one of the alternatives for the CMOS technology [20]. Recently, the QCA arithmetic and logical circuits design are in the focal point of the researcher

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interests. Many logical gates and circuits such as Full Adder (FA) circuits [21, 22], multiplier circuits [23, 24], shift register circuits [25, 26], comparator circuits [27, 28] and multiplexer circuits [29, 30] have been designed in the QCA technology. Full adder circuit is one of the important elements in digital circuits. It plays a vital role in computing and arithmetic circuits such as ALUs and microprocessors [23].

Many of QCA full adders have designed using three 3-input majority gates and two inverter gates in one layer [31–38]. Some of these designs have been implemented without the use of wire crossing [39]. A few numbers of designs have used one lesser inverter gate for implementing QCA FAs in single layer [40] and multilayer [41, 42] wire-crossing layouts. The 5-input majority gate (MG5) has also been utilized for designing QCA FAs [22, 31, 43–55]: coplanar [43–50] and multilayer [22, 31, 51–55] QCA FAs. Some designers have realized QCA FAs using 3-input XOR gate. They have implemented their circuits in QCA coplanar [17, 56–58] and QCA multilayer [59, 60].

In this paper, we propose a novel and efficient QCA full adder circuit in multilayer. The sum output is designed by using one efficient QCA XOR gate. The carry output is also designed by using one efficient 3-input majority gate. Then, we propose an efficient 4-bit Ripple Carry Adder (RCA) circuit using the proposed full adder circuit. The proposed circuits are simulated using QCADesigner tool version 2.0.3 [61]. The simulation results demonstrate that the proposed circuits work correctly. The comparison shows that the proposed QCA circuits have advantages compared to other QCA circuits in term of area, latency, and cost.

The rest of this paper is organized as follows. In Section 2, an overview of the QCA technology is presented. In Section 3, previously reported designs are presented. In Section 4, the proposed new efficient 1-bit full adder and 4-bit QCA RCA are presented. Section 5 shows simulation results and compares proposed circuits to other QCA circuits. Finally, Section 6 concludes the paper.

2 Background

2.1 Quantum Cells

The normal QCA cell is usually constructed in a square form that has four quantum-dots in its corners. Generally, two electrons are injected in each cell, which are placed diagonally because

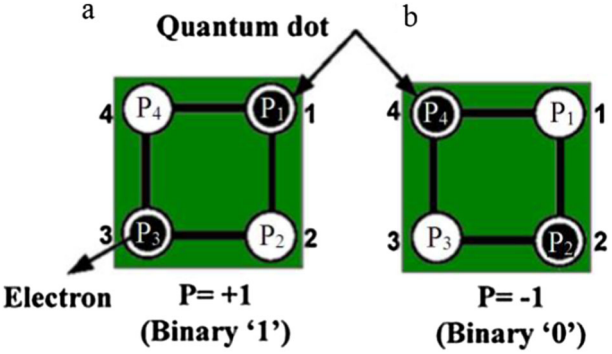

Fig. 1 Normal QCA cell [63]

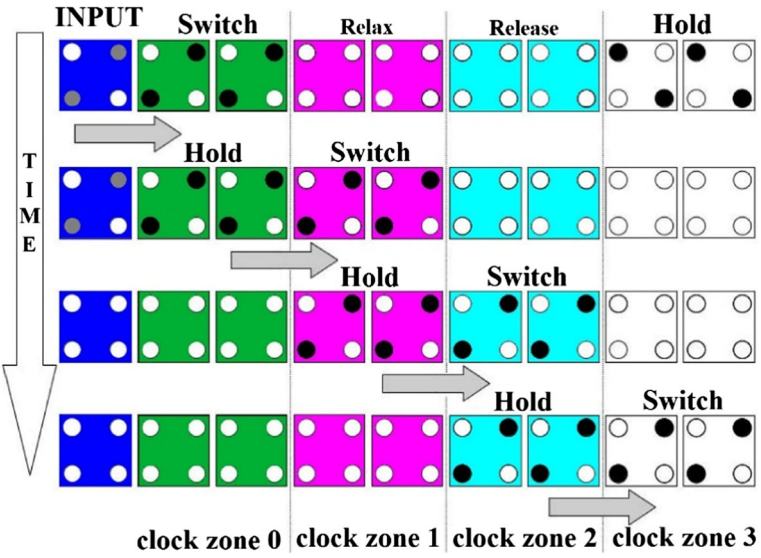

Fig. 2 Clock phases of cells and signal propagation in a wire [65]

of columbic repulsion [62, 63]. So, there are two stable states for replacing the electrons in dots that result in equalization to a binary system that are shown in Fig. 1 [63].

Unlike traditional structures, the position of electrons in the dots is based of binary logic instead of the voltage level in the QCA cells. It should be noted that two diagonal stable states of electrons in the QCA cell give two polarization states $P = -1$ and $P = +1$ which are equivalent to logic "0" and "1", respectively [64]. The polarization P is computed from Eq. (1).

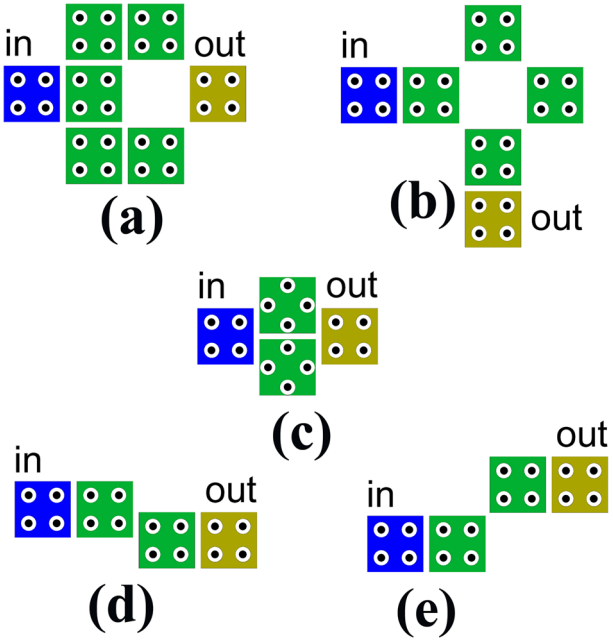

Fig. 3 Various types of IG gates [66]

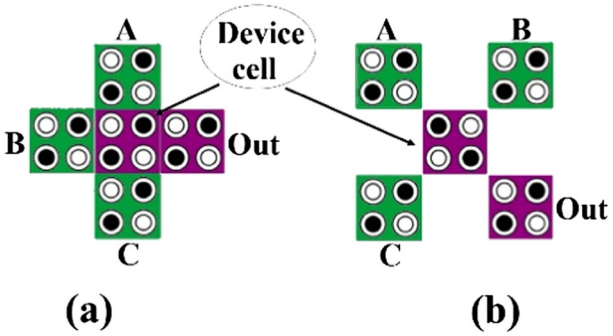

Fig. 4 Two types of 3-input majority gates; (**a**) original, (**b**) rotated [67]

$$P = \frac{(p_1 + p_3) - (p_2 + p_4)}{p_1 + p_2 + p_3 + p_4} \tag{1}$$

Where p_i denotes the polarization of i^{th} dot. At the time of applying clock signal, electrons can move between dots by tunneling because of lowering level of potential barriers. The cells are constructed in such a way that they are isolated from each other and tunneling between dots of adjacent cells cannot be happened [20].

2.2 QCA Clocking

QCA clocking is different to CMOS clocking. The QCA clock is utilized to control and synchronize signals. Furthermore, there aren't power lines in the QCA technology. The QCA cells set to four clock phases named switch, hold, release, and relax phases. Actually, clock signals change potential barrier of tunneling between dots and control electron mobility in the tunnel. Therefore, the cell polarizations will be controllable. As a result, the cell gets four states: polarization, fixed polarization, depolarization and keep depolarized in mentioned clock phases, respectively. Clock phases and signal propagation direction are illustrated in Fig. 2.

2.3 QCA Gates

Three primitive and important gates in the QCA technology are Inverter Gate (IG), Majority Vote Gate (MVG or MG) and XOR gate. In Fig. 3, the layouts of some IGs are illustrated [66].

The MG is an important gate to digital circuits design in the QCA technology. The MG works according to the superposition of inputs. In Fig. 4, two common layouts of 3-input MGs are depicted [67].

The logical function of 3-input majority gate is defined by Eq. (2).

$$MG3(A, B, C) = AB + BC + CA \tag{2}$$

The 2-input AND (AND2) and OR (OR2) gates are obtained by fixing polarization of one input of MG3 to −1 and + 1, respectively [67].

Another important QCA gate is 3-input XOR gate (XOR3). Figure 5 shows the layout of the QCA 3-input XOR gate [56].

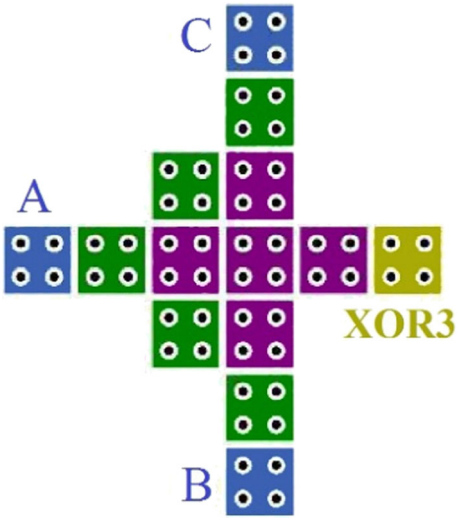

Fig. 5 The utilized 3-input XOR gate in [56]

3 QCA Full Adder

3.1 Circuit Theory

The outputs of the QCA full adder can be computed as follows [31–39]:

$$Sum = A \oplus B \oplus C_{in} = MG\left(C_{in}, \overline{C_{out}}, MG\left(A, B, \overline{C_{in}}\right)\right); \tag{3}$$

$$C_{out} = AB + AC_{in} + BC_{in} \tag{4}$$

Figure 6 shows the QCA block diagram for the implementation of this full adder circuit.

In addition, the output of the full adder can be computed as follows [40–42]:

$$\begin{aligned} Sum &= MG\left(\overline{MG(A, B, C_{in})}, MG\left(\overline{MG(A, B, C_{in})}, B, C_{in}\right), A\right) \\ &= MG\left(\overline{C_{out}}, MG\left(\overline{C_{out}}, B, C_{in}\right), A\right) \end{aligned} \tag{5}$$

Figure 7 shows the QCA block diagram for the implementation of this full adder circuit.

Moreover, the sum output can be computed as follows [22, 43–50, 52–55]:

$$Sum = MG5\left(\overline{C_{out}}, \overline{C_{out}}, A, B, C_{in}\right) \tag{6}$$

Figure 8 shows the QCA block diagram for the implementation of this full adder circuit [22, 43–55].

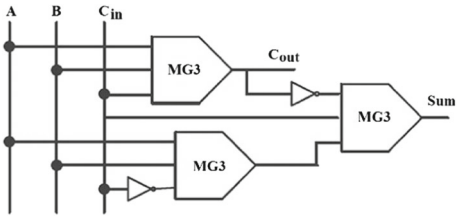

Fig. 6 Logical diagram of QCA FA in [31–39]

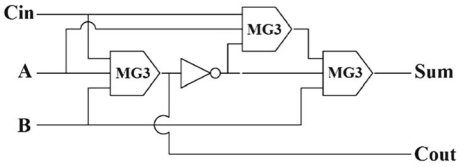

Fig. 7 Logical diagram of QCA FA used in [40–42]

Recently, by using the advantage of 3-input QCA XOR gate, designing of QCA FAs has become more optimum and has facilitated by using only two gates (i.e. XOR3 and MG3) [21, 56–60, 68]. In this method, despite using a minimum number of gates, the main issue is how to interconnect inputs of two gates to each other in coplanar approach. It is because accessing to inputs become more restricted for using the FA in the larger QCA circuits.

3.2 Previous QCA Full Adder Layouts Design

In this section, the previous multilayer QCA full adders are reviewed.

Figure 9 shows the utilized FA in [51] that is based on block diagram that is shown in Fig. 8. It constructed of 51 cells in 0.03 μm^2 effective area on three layers. It has 3 clock phases delay.

Figure 10 shows the layout of the designed full adder in [53]. This design uses 52 QCA cells, 3 clock phases and 0.04 μm^2 area in three layers.

Figure 11 illustrates the layout of the QCA FA design in [54]. The cell count, area and delay of this design are 31 cells, 0.01 μm^2, and 2 clock phases, respectively.

Figure 12 shows two layouts of the designed full adders by Navi et al. in [22, 52]. The first layout that is illustrated in Fig. 12a has 73 cells, 0.04 μm^2 area, and 3 clock phases delay. The second layout that is illustrated in Fig. 12b has 61 QCA cells, 3 clock phases, and 0.03 μm^2 area.

Another design has realized in [55] that is shown in Fig. 13. This designed FA has 22 QCA cells, 3 clock phases, and 0.01 μm^2 area. In this layout, accessing to output cells is impossible unless using extra layers.

It is noticeable that the reviewed designs in Figs. 10, 11, 12 and 13 are designed according to block diagram that is shown in Fig. 8.

Figure 14 shows the three-dimensional view of the utilized QCA FA circuit in [67]. This design consists of 23 cells, 3 clock phases, and 0.01 μm^2 area in three layers.

In addition, it is feasible to place XOR3 and MG3 gates on two separated layers using the multilayer approach. In these designed circuits, accessing to the inputs and outputs for using the FA in larger circuits become more facilitated.

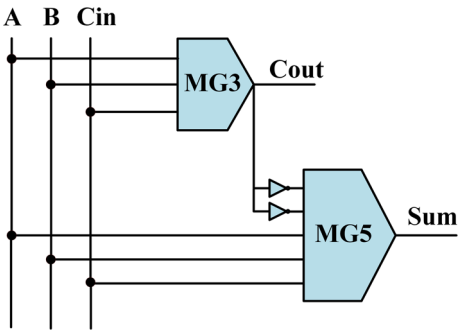

Fig. 8 Logical diagram of QCA FA in [22, 43–50, 52–55]

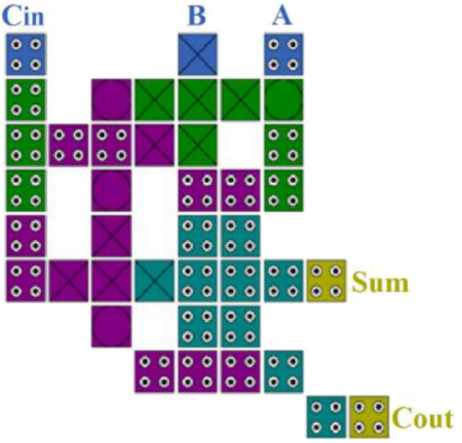

Fig. 9 The layout of the QCA FA in [51]

In this way, Safoev et al. [59, 60] has proposed efficient FA in three layers that uses only 31 cells as shown in Fig. 15. The latency of this design is 2 clock phases, and the required area is $0.02\mu m^2$.

4 The Proposed Circuits

4.1 The Proposed QCA Full Adder

As described in [18], where two beside input signals of MG3 (i.e. B and Cin inputs) in Fig. 15 with same polarization reach sooner than another input signal (i.e. A input), the B (or Cin) value temporarily dominates to A input value. Accordingly, MG3 acts like an inverter gate in this case. Thus, lengthening output paths can lead to noise amplification due to synergic effect. It can be tested that lengthening input paths in [59] can lead to wrong response where B = Cin.

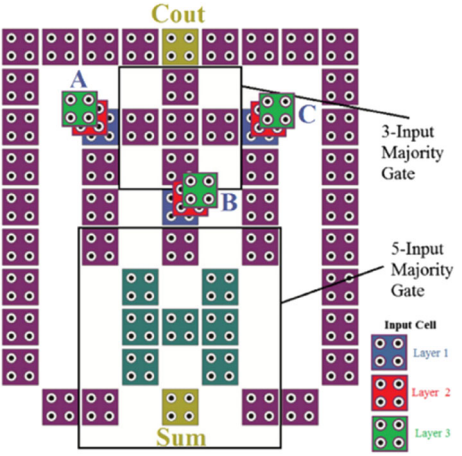

Fig. 10 The layout of the FA in [53]

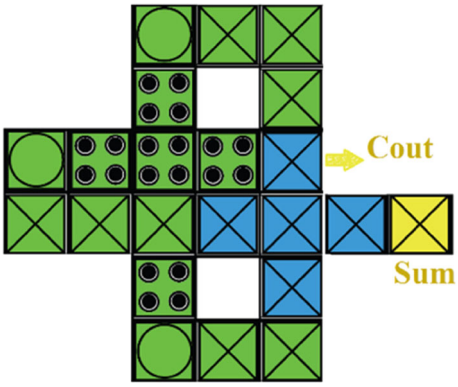

Fig. 11 The layout of the FA in [54]

Hence, drawing the mid-input (i.e. A input) closer to device cell of two gates (i.e. XOR3 and MG3) gives more reliable output response. In this paper, we use this property to design an efficient QCA full adder circuit.

The logical block diagram of the proposed FA circuit is presented in Fig. 16. In addition, Fig. 17 shows the three layers of the proposed efficient FA.

Figure 18 shows three layers of the proposed FA separately. As illustrated in Fig. 18, the XOR3 gate is placed on the main layer (i.e. layer 0) and MG3 gate is placed in layer 2. Layer 1 consists of 3 cells for interconnecting two layers.

The presented work consists of 28 QCA cells. It has 2 clock phases delay. The occupation area of the proposed full adder is $0.01\mu m^2$.

4.2 The Proposed 4-Bit RCA

The accessibility to the inputs and outputs of the proposed FA is feasible and it is simple for using the proposed FA in larger designs. Therefore, we use the proposed FA for designing an efficient 4-bit ripple carry adder. Figures 19 and 20 show the logical diagram and the layout of the proposed 4-bit QCA RCA, respectively.

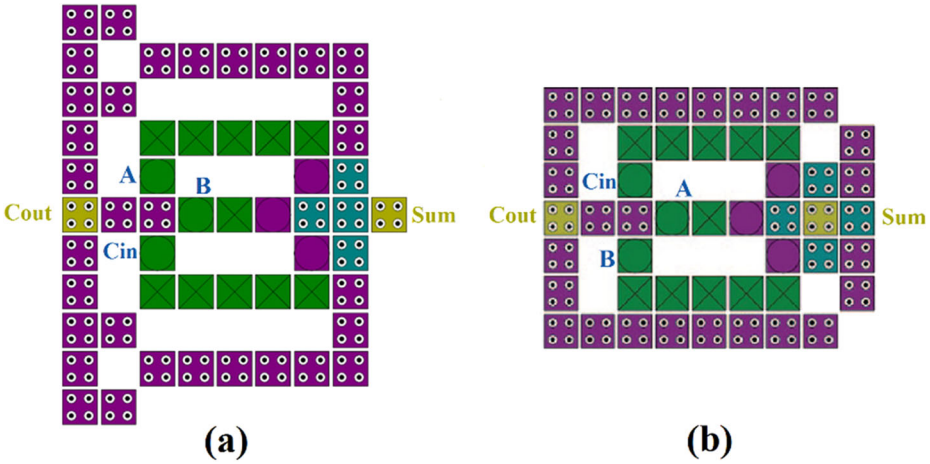

Fig. 12 The layouts of the designed FA **a** in [22] **b** in [52]

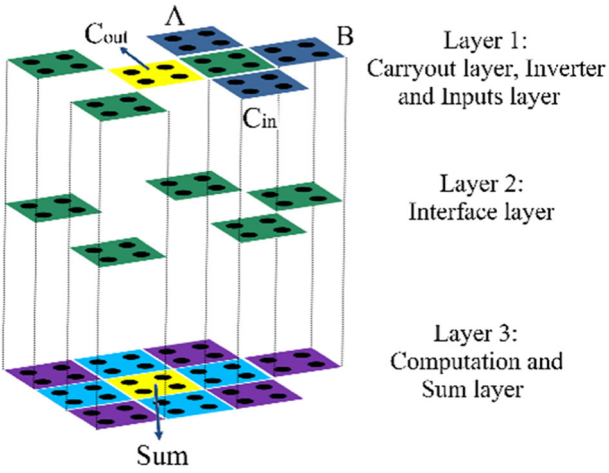

Fig. 13 Three layers of the designed FA in [55]

The layout of the proposed RCA contains only 135 cells, and 0.06μm^2 area. This design could be easily extended to n-bit RCA circuit.

5 Simulation Results and Comparison

The proposed 1-bit QCA full adder and 4-bit QCA RCA are simulated by using QCADesigner tool version 2.0.3. In this section, for determining the cost parameter value, the following equation is used:

$$\text{Cost} = \text{Area}\left(\mu\text{m}^2\right) \times \text{Latency (clock cycle)} \tag{7}$$

5.1 The Proposed QCA Full Adder

Figure 21 shows simulation results using the bistable approximation engine by default settings. The simulation results illustrate that the designed FA performs correctly. The latency is 0.5 clock cycles.

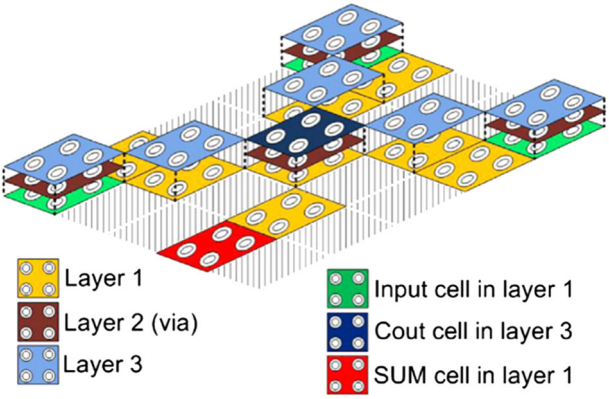

Fig. 14 The layout of the designed FA in [67]

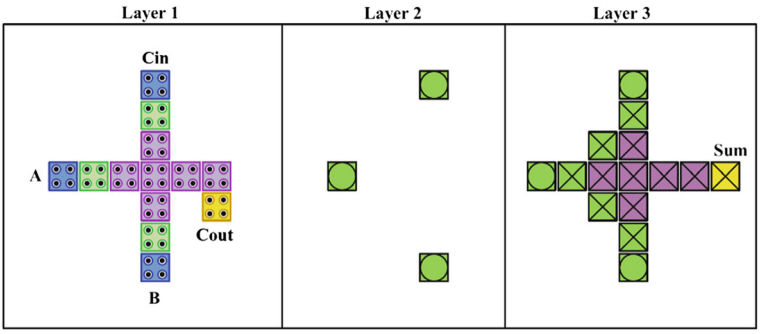

Fig. 15 Three layers of FA proposed in [59, 60]

Table 1 compares our proposed 1-bit QCA FA with other existing designs. This comparison shows that our proposed QCA FA is most cost and delay efficient compared to other QCA FA circuits in [21, 22, 31–59, 67, 68].

Based on our simulation results that are shown in Table 1, our proposed QCA FA circuit has a minimum number of cell count, area, delay and cost in comparisons with previous designs in [21, 31–51, 53, 54, 56–59]. For example, the proposed QCA FA circuit provides an improvement by about 26, 50, 33 and 66% in terms of cell count, area, latency, and cost, respectively compared to [42].

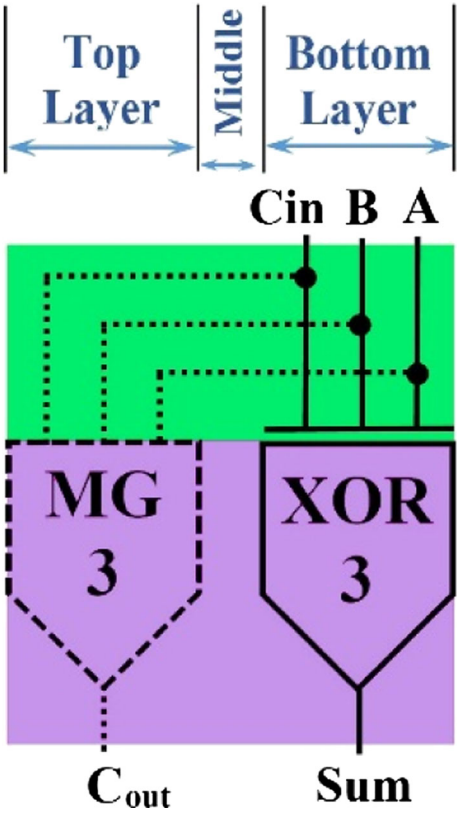

Fig. 16 Logical diagram of the proposed FA

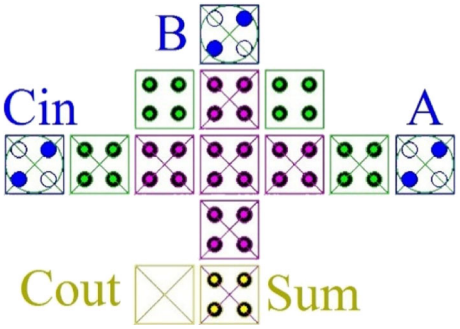

Fig. 17 QCA layout of the proposed 3-layer QCA FA

Despite less cell count in [55, 67], the designed FA circuit in this paper has a better delay and cost term features and has improved by about 33% in these two terms. Moreover, despite the presented FA circuit in [55], our design has accessibility to output cells.

Although the designed FA circuits in [21, 36, 44, 54, 56, 58, 59, 68] have the same delay time with our proposed QCA FA circuit, our proposed FA circuit has supremacy in cell count, area and cost parameters. In comparison with the designed FA in [21], our design has one cell lesser and improvement by about 50% in area and cost. In addition, our design has improvements in cell count, area and cost parameters by about 31, 75 and 75% in comparison with [56], 9, 50 and 50% in comparison with [54, 59], 15, 50 and 50% in comparison with [36], 37, 74 and 74% in comparison with [44], 31, 75 and 75% in comparison with [58], and 9, 66 and 66% in comparison with [68], respectively.

Practically, it could be tested that lengthening the input and output lines of the proposed FA circuit leads to more reliable output response and the proposed FA circuit is more relaxed about changing the input and outputs lines than previous design in [59].

The results show that we propose an efficient QCA full adder in terms of cell count, area, delay, and cost. Moreover, compatibility with other designs, accessibility to the inputs and outputs and flexibility for changing the length of the input and output lines are other advantages of the proposed FA circuit. Hence, the proposed QCA FA is applicable to use in designing larger QCA circuits such as RCA circuits.

5.2 The Proposed 4-Bit RCA

Figure 22 illustrates simulation results of the proposed 4-bit RCA that is simulated by bistable approximation engine using 220,000 samples. Other setting remained by default. The proposed RCA has 5 clock phases or 1.25 clock cycles latency.

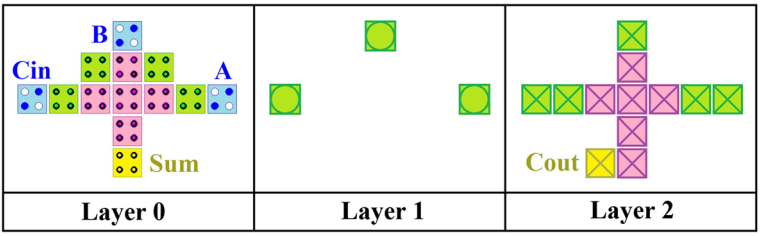

Fig. 18 Three layers of the proposed FA

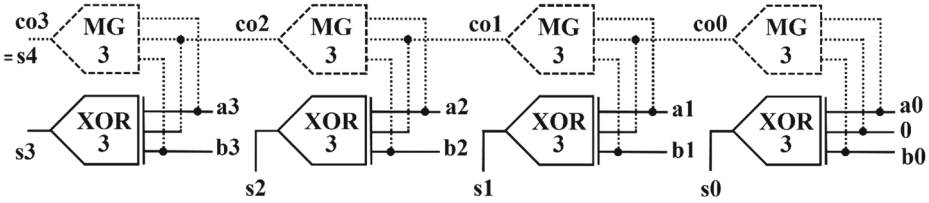

Fig. 19 The logical diagram of the proposed 4-bit QCA RCA

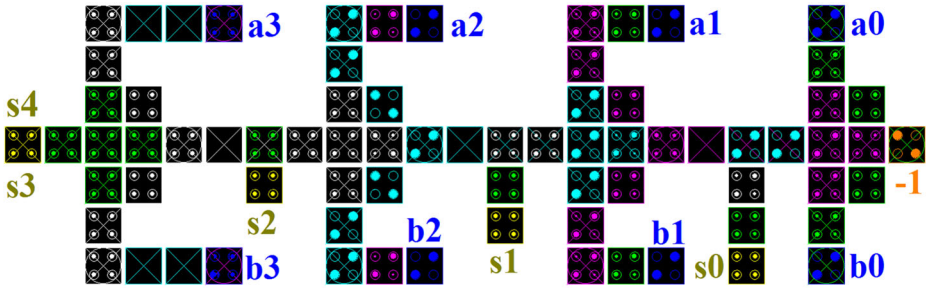

Fig. 20 The layout of the proposed 4-bit QCA RCA

The comparison between the proposed 4-bit ripple carry adder circuit and previous circuits are demonstrated in Table 2.

According to results in Table 2, the proposed 4-bit QCA RCA circuit has best results in terms of cell count, area and cost in comparison to all mentioned designs in Table 2. So, our

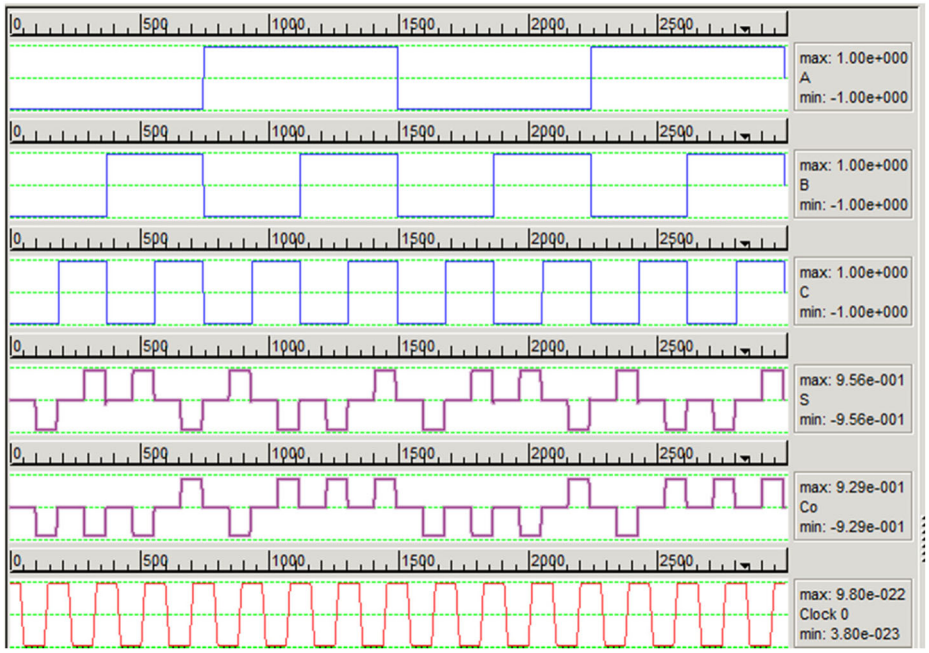

Fig. 21 The simulation results of the proposed FA

Table 1 Comparison of the QCA Full Adders

Reference	cell count	Ratio	Area (μm^2)	Ratio	Delay (clock Phase)	Ratio	Application	Cost (Area * Latency)	Ratio
[56]	41	1.5	0.04	4	2	1	coplanar	0.0200	4
[31]	108	3.9	0.08	8	4	2	coplanar	0.0800	16
[39]	45	1.6	0.03	3	3	1.5	coplanar	0.0225	4.5
[32]	47	1.7	0.04	4	4	2	coplanar	0.0400	8
[33]	59	2.1	0.043	4.3	4	2	coplanar	0.0430	8.6
[34]	52	1.9	0.039	3.9	4	2	coplanar	0.0390	7.8
[35]	46	1.6	0.04	4	4	2	coplanar	0.0400	8
[41]	86	3.1	0.06	6	4	2	multilayer	0.0600	12
[40]	95	3.4	0.12	12	4	2	coplanar	0.1200	24
[57]	60	2.1	0.06	6	4	2	coplanar	0.0600	12
[21]	29	1.0	0.02	2	2	1	coplanar	0.0100	2
[22]	73	2.6	0.04	4	3	1.5	multilayer	0.0300	6
[49]	49	1.8	0.04	4	4	2	coplanar	0.0400	8
[50]	46	1.6	0.035	3.5	4	2	coplanar	0.0350	7
[46]	53	1.9	0.047	4.7	3	1.5	coplanar	0.0353	7.05
[48]	63	2.3	0.05	5	3	1.5	coplanar	0.0375	7.5
[52]	61	2.2	0.03	3	3	1.5	multilayer	0.0225	4.5
[59]	31	1.1	0.02	2	2	1	multilayer	0.0100	2
[36]	33	1.2	0.02	2	2	1	coplanar	0.0100	2
[55]	22	0.8	0.01	1	3	1.5	multilayer	0.0075	1.5
[67]	23	0.8	0.01	1	3	1.5	multilayer	0.0075	1.5
[47]	48	1.7	0.05	5	3	1.5	coplanar	0.0375	7.5
[42]	38	1.4	0.02	2	3	1.5	multilayer	0.0150	3
[37]	86	3.1	0.08	8	4	2	coplanar	0.0800	16
[45]	71	2.5	0.06	6	3	1.5	coplanar	0.0450	9
[53]	58	2.1	0.04	4	3	1.5	multilayer	0.0300	6
[38]	69	2.5	0.07	7	4	2	coplanar	0.0700	14
[54]	31	1.1	0.02	2	2	1	multilayer	0.0100	2
[51]	51	1.8	0.03	3	3	1.5	multilayer	0.0225	4.5
[43]	95	3.4	0.087	8.7	8	4	coplanar	0.1740	34.8
[44]	45	1.6	0.0396	3.96	2	1	coplanar	0.0198	3.96
[58]	41	1.5	0.04	4	2	1	coplanar	0.0200	4
[68]	31	1.1	0.03	3	2	1	coplanar	0.015	3
This paper	28	1	0.01	1	2	1	multilayer	0.0050	1

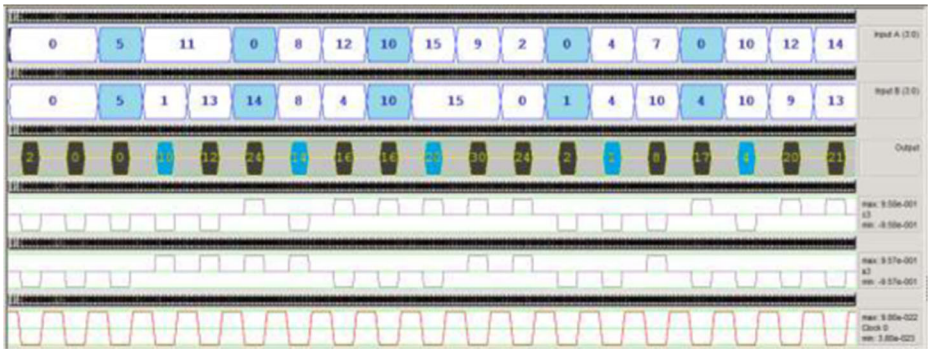

Fig. 22 The simulation results of the proposed 4-bit QCA RCA

Table 2 Comparison of the 4-bit RCA circuits

Reference	cell count	Ratio	Area (μm^2)	Ratio	Delay (clock Phase)	Ratio	Application	Cost (A*L)	Ratio
[51]	308	2.3	0.29	4.83	8	1.6	multilayer	0.58	7.73
[45]	442	3.3	1	16.67	8	1.6	coplanar	2	26.67
[42]	237	1.8	0.24	4	6	1.2	multilayer	0.36	4.80
[44]	314	2.3	0.32	5.33	6	1.2	multilayer	0.48	6.40
[36]	175	1.3	0.14	2.33	4	0.8	coplanar	0.14	1.87
[48]	295	2.2	0.3	5	6	1.2	coplanar	0.45	6
[21]	269	2.0	0.37	6.17	14	2.8	coplanar	1.295	17.27
[40]	366	2.7	0.51	8.50	10	2	coplanar	1.275	17
[35]	187	1.4	0.2	3.33	16	3.2	coplanar	0.8	10.67
[33]	262	1.9	0.2	3.33	7	1.4	coplanar	0.35	4.67
[58]	209	1.5	0.3	5	5	1	coplanar	0.375	5
[60]	184	1.4	0.1	1.67	5	1	multilayer	0.125	1.67
This paper	135	1	0.06	1	5	1	multilayer	0.075	1

design provides improvement at least by about 22, 40 and 40% in terms of cell count, occupation area and cost, respectively in comparison to other QCA RCA circuits in this table. For example, despite the more delay of one clock phase in comparison to [36], the provided improvement in terms of cell count, area and cost are 22, 57, and 46%, respectively.

Despite similar delay time to those of the designs proposed in [58, 60], our proposed design provides considerable improvement from the point of view of cell count, occupation area, and final cost. So, the cell count, area, and cost terms have been reduced by about 26, 39, and 40%, respectively compared to [60].

6 Conclusion

The QCA technology as a promising and developing alternative technology for CMOS technology is in the focal point of the researcher interests for designing the ultra-dense and ultra-speed digital circuits. In this paper, we designed a new and efficient QCA full adder circuit by designing an efficient circuit for sum and carry output in separated layers. Then, we designed a novel and efficient 4-bit QCA RCA using 135 QCA cells in 0.06 μm^2 with 5 clock phases delay. The proposed designs are simulated using QCADesigner tool version 2.0.3 that demonstrated correctness work of the proposed designs. Besides, the comparisons showed that the proposed QCA circuits have advantages compared to other QCA circuits in term of area, latency and cost.

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