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Towards Multilayer QCA SISO Shift Register Based on Efficient D-FF Circuits

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Abstract
Quantum-dot Cellular Automata (QCA) is a new technology for replacing CMOS technology at nano-scale dimansion. Shift registers have commonly used circuit in the digital circuits design. In this paper, a new 3-bit Serial Input-Serial Output (SISO) QCA shift register is presented. The proposed circuit uses 3 novel D-Flip-Flops (D-FFs) that are developed in this paper. The proposed circuits are implemented by using QCADesigner tool version 2.0.3. The developed QCA SISO shift register has 120 cells and 0.03 μm^2 area. The results show that the developed circuits have advantages compared to other QCA circuits in terms of area.

Keywords Shift register · Serial-Input-Serial-Output (SISO) · Quantum-dot Cellular Automata (QCA) · D-Flip-Flop (D-FF) · Multilayer design

1 Introduction

Quantum-dot Cellular Automata (QCA) is an emerging technology at nano-scale that can be a promising alternative for CMOS technology [1–3]. In this technology, information is transferred by reconfiguration of the charges instead of current [4, 5]. The developed circuits in this technology require low-area. They also provide high-speed switching [2, 6, 7]. Therefore, the circuits implementation such as multiplexer circuits [1, 5, 8–11], shift register circuits [2, 11–21], and full adder circuits [6, 22, 23] in this technology have received great attentions by researchers.

On the other hand, shift register circuits have important role in digital circuits. So, the performance of many digital circuits is determined by the performance of the shift register

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circuits [2, 11–21]. Recently, several attempts have been done to improve the performance of the shift register implementation in the QCA technology [12, 15, 21]. Das and De [12] have proposed a 3-bit QCA Serial Input-Serial Output (SISO) shift register, which consists of 100 cells, and 0.065 μm^2 area. Authors of [15] have presented QCA SISO shift register, which consists of 150 cells, and 0.125 μm^2 area. Mustafa and Beigh [21] have presented a 3-bit QCA shift register, which consists of 142 cells, and 0.122 μm^2 area.

This paper presents and evaluates a novel shift register circuit in the QCA technology, which has following distinctive characteristics:

a) It is based on three new D-Flip-Flop (D-FF) circuits.
b) It is implemented in 5 layers.
c) It is SISO shift register circuit.
d) It is implemented using QCADesigner tool version 2.0.3.

Our implementation results indicate that the performance of the proposed QCA SISO shift register circuit is improved compared to other QCA shift register circuits in terms of area.

The reminder of this paper is organized as follows: Section 2 provides a background to QCA technology and proposed circuits. Section 3 presents a literature review of the shift register circuits. The proposed circuits are presented in Section 4. In Section 5, the implementation results of the proposed circuits and comparison with other circuits are presented. Finally, this paper is concluded in Section 6.

2 Background

2.1 QCA Cells

The most important components in the QCA technology are cells. Each cell in this technology consists of four dots that are located in four corners of the square. Each cell has two electrons that can move freely between the dots. In stable conditions, the electrons are arranged in diagonals and create two poles of +1 (logic1) and −1 (logic 0). Figure 1 shows the logical states in the QCA cell [4, 7, 8, 17, 22, 24].

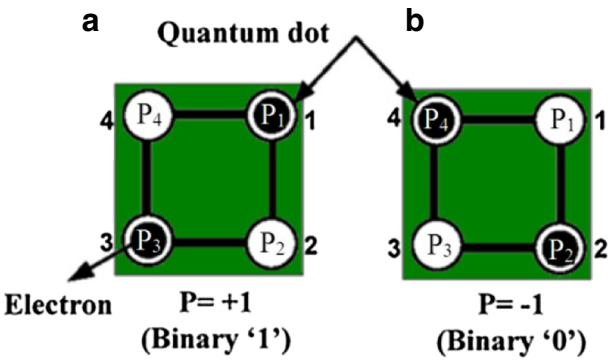

Fig. 1 QCA cellular states **a** P = +1, **b** P = −1 [4, 7, 8, 17, 22, 24]

The polarization of the cells is calculated from (1) [4, 8, 17, 22, 24].

$$P = \frac{(P1 + P3) - (P2 + P4)}{(P1 + P2 + P3 + P4)} \tag{1}$$

In this equation, Pi represents the charge at ith point.

2.2 QCA Gates

The main gates in the QCA technology are Majority (M) gate and inverter gate that are shown in Fig. 2 [4, 6, 8, 12, 22, 24, 25].

The output of the 3-input QCA majority gate can be calculated as follows:

$$M\ (A, B, C) = AB + BC + CA \tag{2}$$

It should be noted that the QCA AND gate and QCA OR gate can be achieved by applying the logic "0" and "1", respectively to one input of the QCA majority gate. The QCA majority gates in Fig. 2b, are implemented in one layer, but they can be implemented in multilayer. Figure 3 shows how the QCA majority gates can be implemented in multilayers and the effect of the layers on the output [1].

Figure 3 shows the majority gate outputs in 1-layer, 2-layer and 3-layer, where A, B, and C are inputs and M is output. As it is shown in Fig. 3a, the output of the coplanar implementation of majority gate is as follows: $M = AB + BC + CA$. However, if the majority gate is implemented in 2-layer, the output is shown as $M = AB + BC' + C'A$ and $M = (AB + BC + CA)'$ as it is shown in Fig. 3b. In addition, the output of the majority gate is $M = AB' + B'C' + C'A$ and $M = (AB' + B'C + CA)'$ as it is shown in Fig. 3c, where

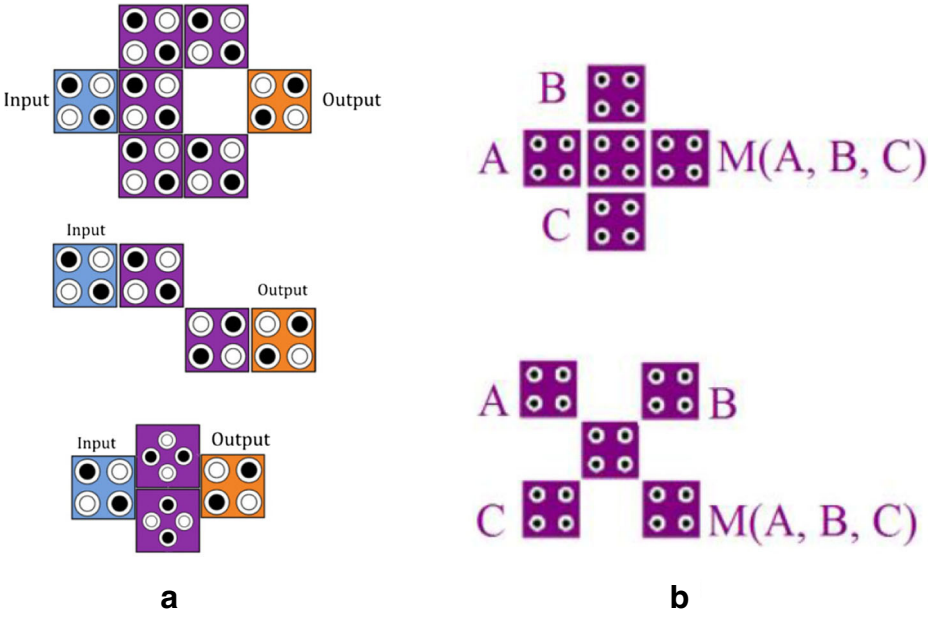

Fig. 2 The basic QCA logic gates **a** three invertors [4, 6–8, 12, 22, 24, 25] and **b** two 3-input majority gate [6, 7, 12, 22, 24]

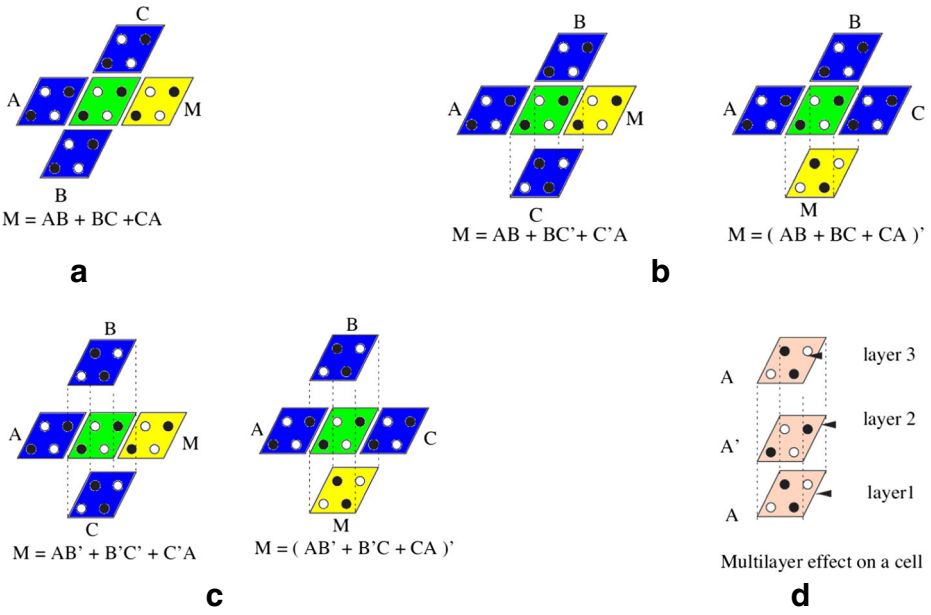

Fig. 3 Multilayer layout and its result [1]

using 3 layers for implementation. Figure 3d shows the result of layers on transforming input on the output [1].

2.3 QCA D-FF

The flip-flop circuit has an input that is shown by D. The D-FF plays an important role in digital circuits such as shift registers and memories [2, 11–21, 25–29]. So, many researchers have attempts to complete the performance of D-FF circuits, especially in the QCA technology [2, 11–21, 25, 26, 28, 29]. Table 1 shows truth table for the D-FF. where CLK, D and Q denote clock, input and output, respectively.

2.4 QCA Shift Register

Shift register is a register that can shift its content to the left or right. The shift register is combined of D-FF to save the data. An n–bit shift register combined of n D-FF and it can save n bits of data. Shift registers can be categorized into four groups: (1) Serial-Input-Serial-Output (SISO) registers. (2) Serial-Input-Parallel-Output (SIPO) registers. (3)

Table 1 D-FF truth table

CLK	D	Q
0	X	NC
1	0	0
1	1	1

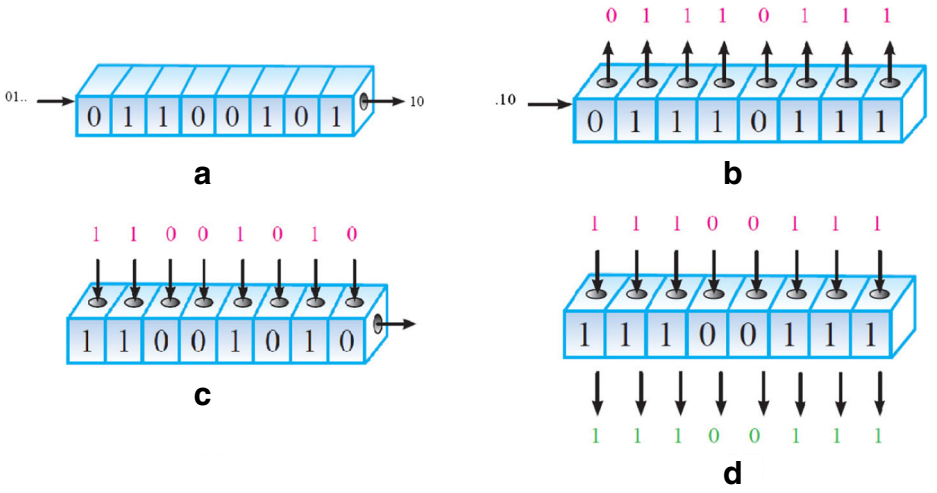

Fig. 4 Four shifts register groups, **a** SISO register, **b** SIPO register, **c** PISO register, **d** PIPO register [30]

Parallel-Input-Serial-Output (PISO) registers and (4) Parallel-Input-Parallel-Output (PIPO) registers [30]. Figure 4 shows these four groups of shift register circuits.

SISO shift register circuit is a main type of shift register circuits [12, 15, 17, 20, 21]. In the SISO shift register circuit, the inputs and outputs are received in serial. Figure 5 shows the block diagram and QCA circuit of the 3-bit SISO shift register circuit [12, 15].

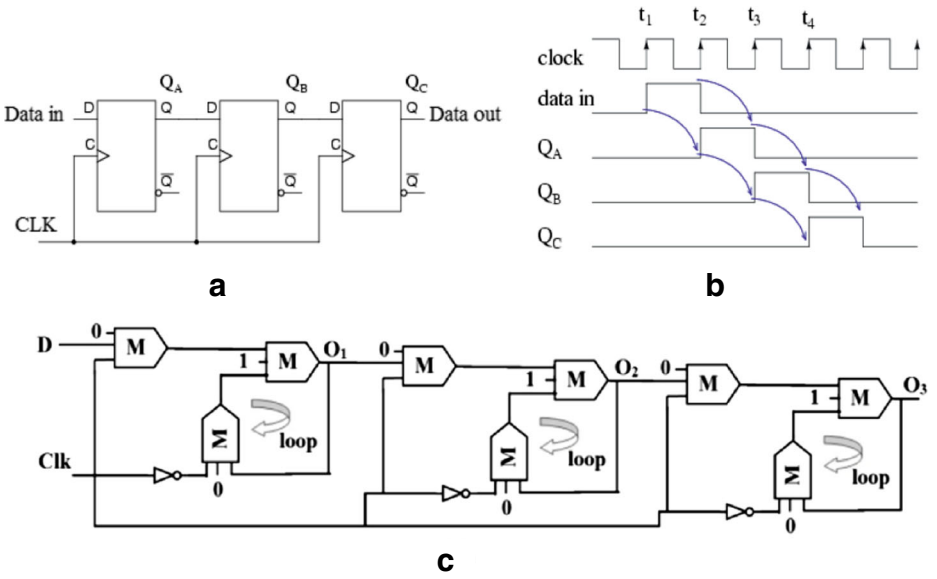

Fig. 5 3-bit SISO shift register. **a** block diagram [12, 15], **b** Timing diagram [15] and **c** QCA schematic [12]

3 Related Works

3.1 QCA D-FF

Figure 6 shows several designs that improve the QCA D-FF circuit in terms of the number of cell, area, and cock cycles [11, 12, 14, 15, 18–21, 25, 29].

Das and De [12] have proposed a QCA D-FF, which is shown in Fig. 6a. This design consists of 23 cells, 0.016 μm^2 area and 1 clock cycle. Lim et al. [14] have designed QCA D-FF, which is shown in Fig. 6b. This design consists of 104 cells, 0.20 μm^2 area and 1.25 clock cycles. Ahmad et al. [15] have presented QCA D-FF using Linear Feedback Shift Registers (LFSR), which is shown in Fig. 6c. This design consists of 33 cells, 0.03 μm^2 area and 1.75 clock cycles. In reference [18], a new QCA multilayer D-FF is presented, which is shown in Fig. 6d. This design consists of 45 cells, 0.04 μm^2 area and 1 clock cycle. Authors of [19] have proposed a D-FF, which is shown in Fig. 6e. This design consists of 46 cells, 0.50 μm^2 area and 1.75 clock cycles. Reshi et al. [20] have designed a QCA D-FF, which is shown in Fig. 6f. This design consists of 33 cells, 0.0210 μm^2 area and 1 clock cycles. Kianpour and Sabbaghi-Nadooshan [25] have presented QCA D-FF with clock control using Configurable Logic Block (CLB), which is shown in Fig. 6g. This design consists of 91 cells, 0.1 μm^2 area and 2.5 clock cycles. Shamsabadi et al. [29] have designed a master-slave QCA D-FF, which is shown in Fig. 6h. This design consists of 133 cells, 0.14 μm^2 area and 2.75 clock cycles. Goswami et al. [11] have designed a D-FF, which is shown in Fig. 6i. This design consists of 30 cells,0.03 μm^2 area and 0.75 clock cycles. Mustafa and Beigh [21] have presented QCA D-FF with clock control, which is shown in Fig. 6j. This design consists of 35 cells, 0.027 μm^2 area and 1.25 clock cycles.

3.2 QCA SISO Shift Register

Figure 7 shows several designs that improve the QCA SISO shift register circuit in terms of the number of cells, area, and cock cycles [12, 15, 21].

Das and De [12] have proposed a 3-bit QCA SISO shift register, which is shown in Fig. 7a. This design consists of 100 cells, 0.065 μm^2 area and 3 clock cycles. Authors of [15] have presented QCA SISO shift register, which is shown in Fig. 7b. This design consists of 150 cells, 0.125 μm^2 area and 7.5 clock cycles. Mustafa and Beigh [21] have presented a 3-bit QCA shift register, which is shown in Fig. 7c. This design consists of 142 cells, 0.122 μm^2 area and 3.75 clock cycles.

4 The Proposed Circuits

This section presents three new QCA D-FF circuits and then new and efficient circuit is presented for SISO shift register based on these QCA D-FF circuits.

4.1 The Proposed QCA D-FF Circuits

Figure 8 shows first proposed circuit for the QCA D-FF.

The proposed circuit for the QCA D-FF has one data input, one clock input and one output. The inputs are labeled as D for data input and clk for clock input. The output is shown by Q1.This circuit consists of 25 cells. It requires 0.02 μm^2 area and 1 clock cycle.

Figure 9 shows second proposed circuit for the QCA D-FF.

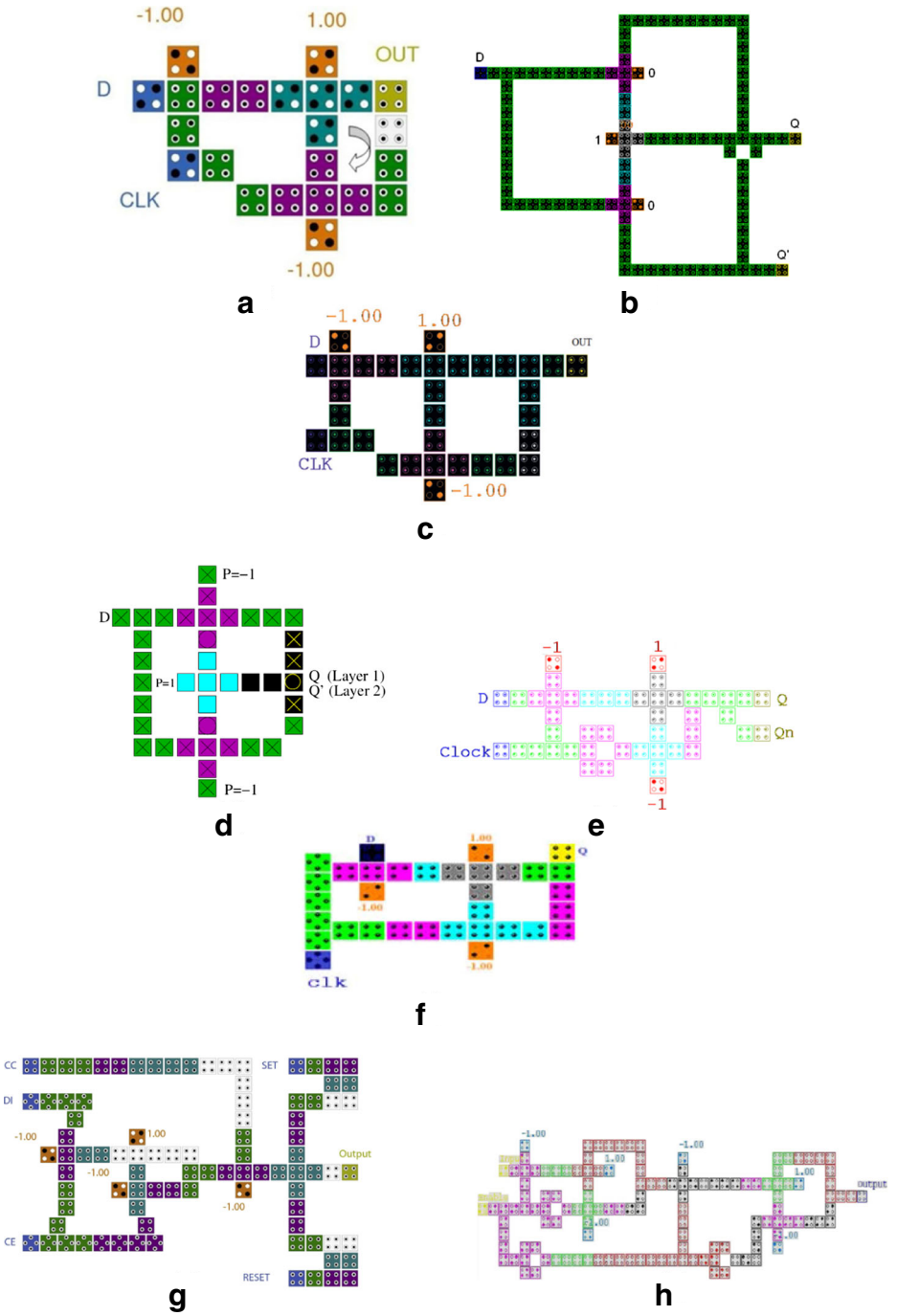

Fig. 6 The employ QCA D-FF circuits, **a** in [12], **b** in [14], **c** in [15], **d** in [18], **e** in [19], **f** in [20], **g** in [25], **h** in [29], **i** in [11], **j** in [21]

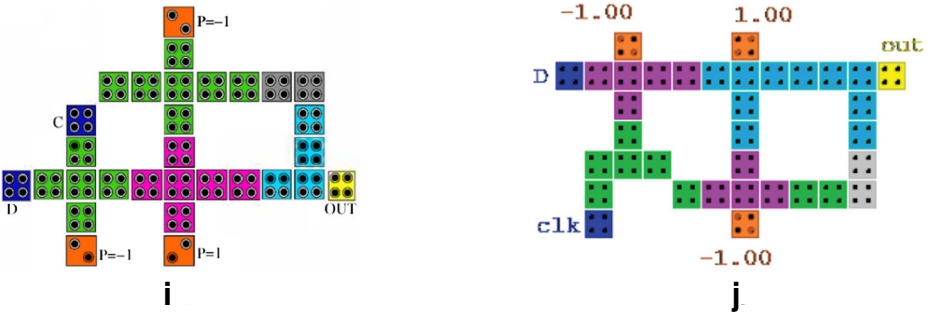

Fig. 6 (continued)

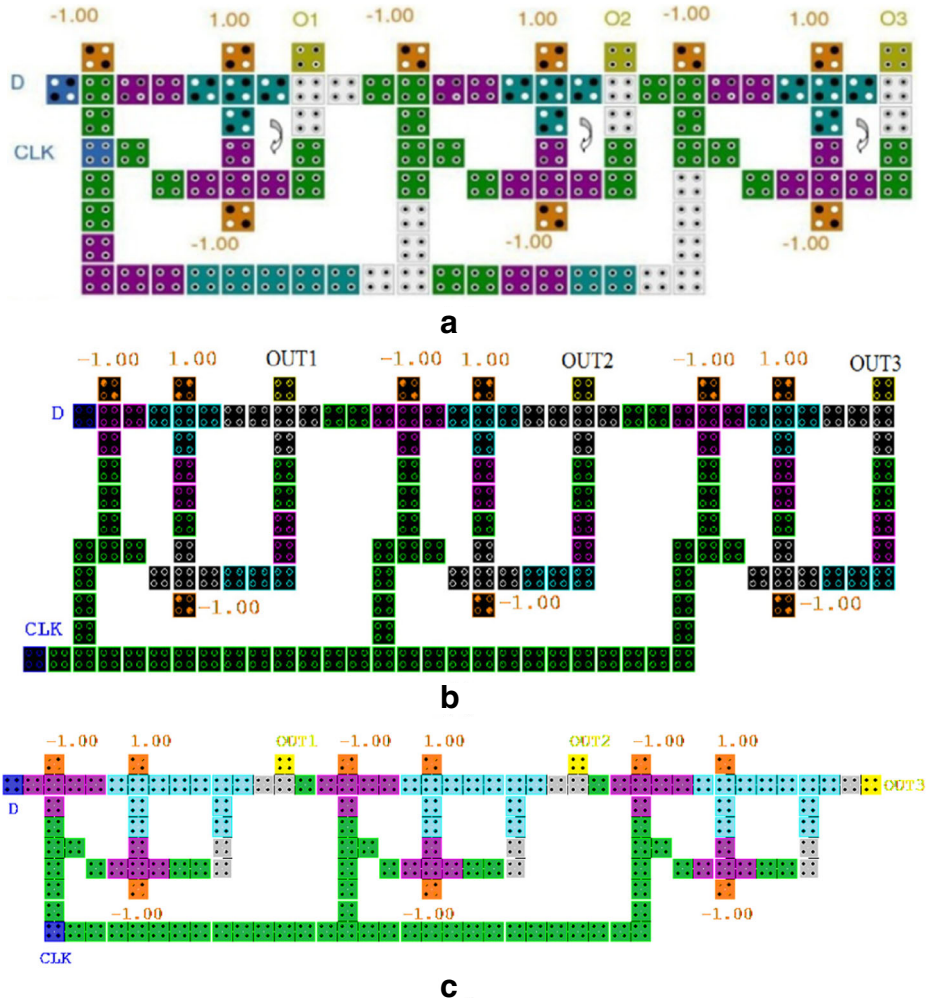

Fig. 7 The 3-bit Shift Register circuit **a** in [12], **b** in [15], **c** in [21]

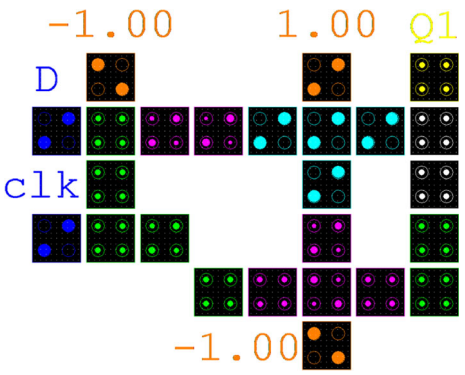

Fig. 8 The first proposed circuit for the QCA D-FF

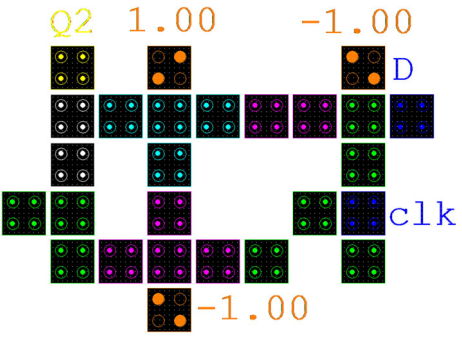

Fig. 9 The second proposed circuit for the QCA D-FF

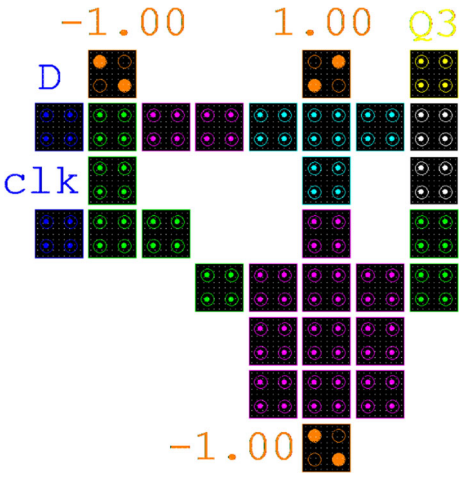

Fig. 10 The third proposed circuit for the QCA D-FF

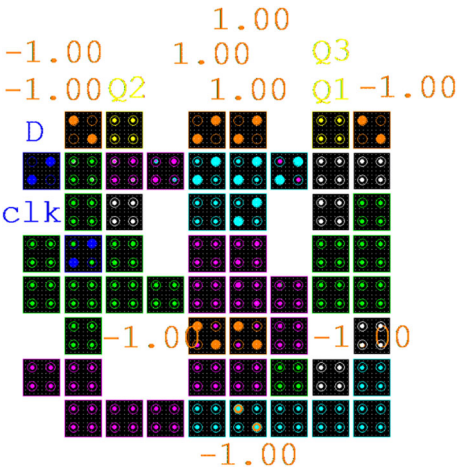

Fig. 11 The proposed 5-layer 3-bit SISO shift registers in the QCA technology

The proposed circuit for the QCA D-FF has one data input, one clock input and one output. The inputs are labeled as D for data input and clk for clock input. The output is shown by Q2. This circuit consists of 27 cells. It requires 0.02 μm^2 area and 1 clock cycle.

Figure 10 shows third proposed circuit for the QCA D-FF.

The proposed circuit for the QCA D-FF has one data input, one clock input and one output. The inputs are labeled as D for data input and clk for clock input. The output is shown by Q3. This circuit consists of 31 cells. It requires 0.03 μm^2 area and 1 clock cycle.

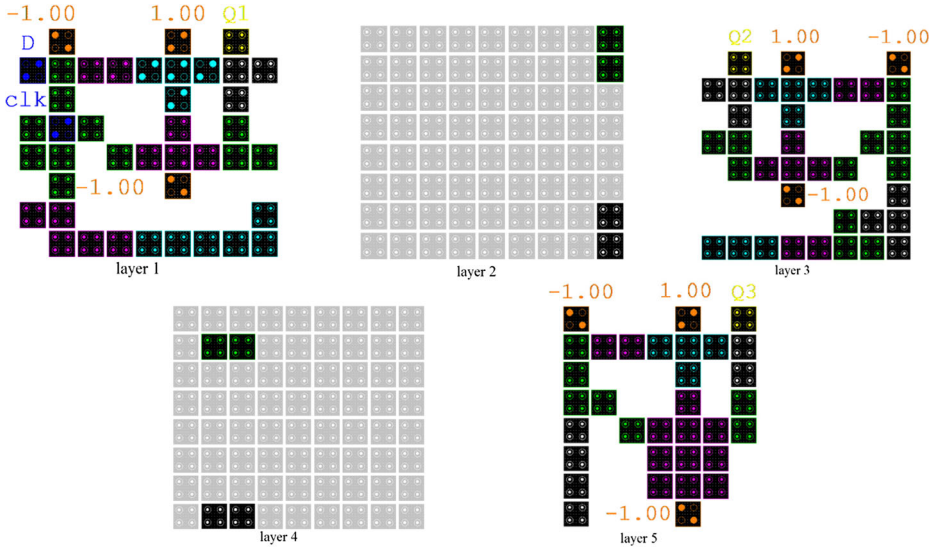

Fig. 12 Layers of the proposed 3-bit SISO shift register in the QCA technology

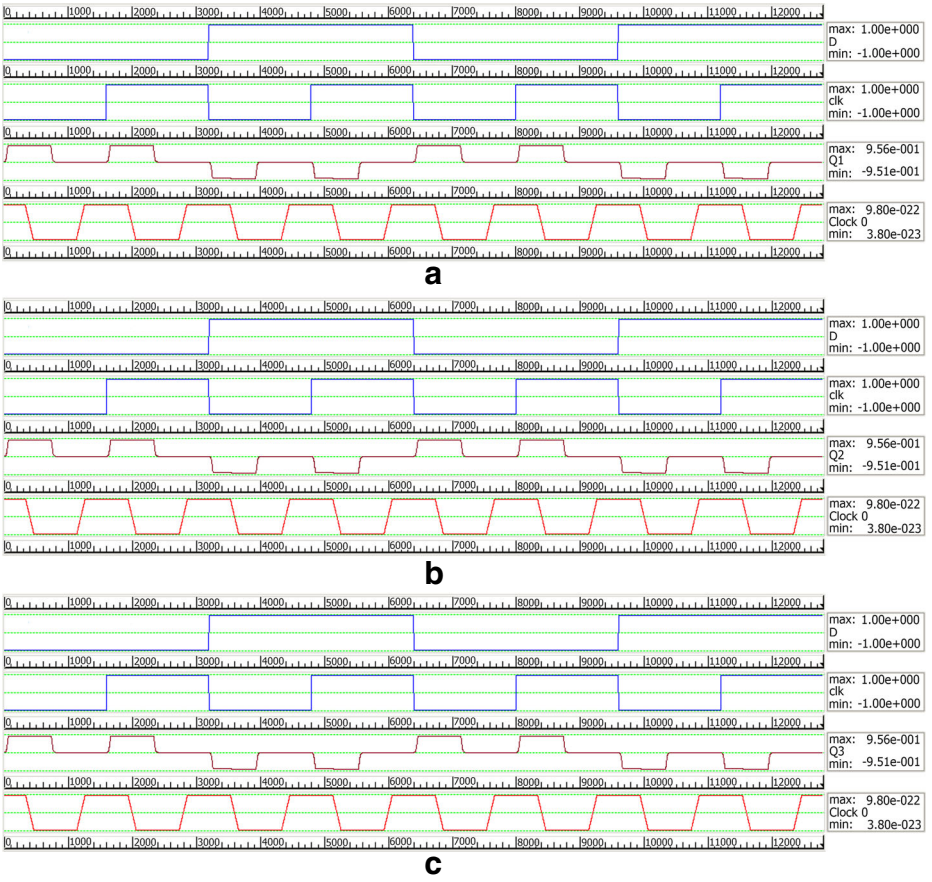

Fig. 13 Implementation results of the proposed QCA D-FF circuits **a** first proposed QCA D-FF circuit, **b** second proposed QCA D-FF circuit, **c** third proposed QCA D-FF circuit

4.2 The Proposed 3-Bit SISO Shift Registers Circuit

Figure 11 shows the proposed 3-bit SISO shift register circuit. The inputs of the proposed circuit for the 3-bit QCA SISO shift register are labeled as D for data input and clk for clock input. The outputs are shown by Q1, Q2 and Q3. The output Q3 is the ultimate SISO shift register output. This circuit is implemented in 5 layers and composed of three proposed QCA D-FF circuits that are shown in Figs. 8–10.

Figure 12 shows the utilized 5 layers in the proposed SISO QCA shift register circuit.

Based on the results, which are show in Fig. 12, the proposed QCA D-FF circuits are utilized in layers 1, 3 and 5. Layers 2 and 4 are utilized for transferring data between the D-FFs. The proposed 3-bit QCA SISO shift register consists of 120 cells. It requires 0.03 μm^2 area and 4 clock cycles.

Table 2 The comparative table for the D-FF circuits

Ref	Area (μm^2)	Cell count
[11]	0.03	30
[12]	0.016	23
[14]	0.20	104
[15]	0.027	33
[18]	0.04	45
[19]	0.05	46
[20]	0.021	33
[21]	0.027	35
[25]	0.1	91
[29]	0.14	133
This paper (first design)	0.02	25
This paper (second design)	0.02	27
This paper (third design)	0.03	31

5 The Implementation Results and Comparison

The QCADesigner tool version 2.0.3 is utilized to acquire the implemented results. The following parameters are used to implement the proposed circuits: number of samples: 12800, radius of effect(nm): 65.00, relative permittivity: 12.9000, clock high: 9.800e-022, clock low: 3.800e-23, clock shift: 0.00e-000, clock amplitude factor: 2.000, layer separation: 11.5000, maximum iteration per sample: 100, temperature: 1–15° K, relaxation time: 1.000e-015, time step: 1.000e-016,total simulation time: 7.000e-011 [3, 10, 12, 28].

5.1 The Proposed QCA D-FF Circuits

Figure 13 shows the implementation results for the proposed QCA D-FF circuits.

The implementation results confirm that the outputs of the proposed QCA D-FF circuits are correctly obtained. Table 2 summarizes the implementation results for the proposed QCA D-FF circuits compared to other D-FF circuits.

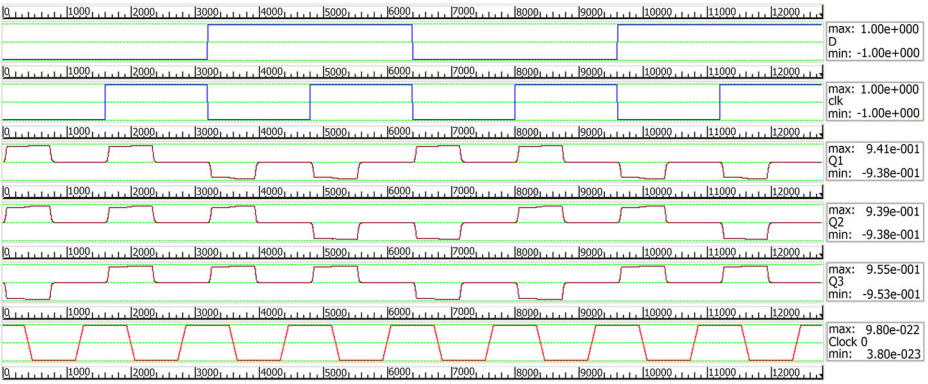

Fig. 14 Implementation result for the proposed 5-layer, 3-bit SISO QCA shift register

Table 3 The comparative table for 5-layer 3-bit SISO QCA shift registers

Reference	Cell count	Area (μm^2)
[12]	100	0.065
[15]	150	0.125
[21]	142	0.122
This paper	120	0.03

Based on our implementation results that are shown in Table 2, and Figs. 8, 9 and 10, the proposed QCA D-FF circuits have better performance in comparison with other QCA D-FF circuits. However, the designed D-FF circuit in [12] provides better performance in terms of area and cell count compared to our proposed QCA D-FFs, but our developed circuit for QCA SISO shift register using the proposed QCA D-FF circuits provides better performance in terms of area compared to [12].

5.2 The Proposed 3-Bit QCA SISO Shift Register Circuit

Figure 14 shows the implementation results for the proposed 3-bit QCA SISO shift register circuit.

The implementation results confirm that the output of the proposed 3-bit QCA SISO shift register circuit is correctly obtained. Table 3 summarizes the implementation results for the proposed 3-bit QCA SISO shift register circuit in comparison with other 3-bit QCA SISO shift register circuits.

Based on our implementation results that are shown in Table 3, Figs. 11 and 12, the proposed 5-layer 3-bit QCA SISO shift register circuit has advantage in terms of area compared to other QCA shift register circuits in [12, 15, 21].

6 Conclusion

One of the most important QCA circuit in the digital circuits design is the SISO shift register. So, this paper presented and evaluated novel and efficient circuit for the 3-bit QCA SISO shift register. The proposed circuit for the 3-bit QCA SISO shift register was implemented in 5 layers based on three new QCA D-FF circuits. The proposed 3-bit QCA SISO shift register consists of 120 cells and 0.03 μm^2 area. We utilized QCADesigner tool Version 2.0.3 to implement the proposed circuits. The results showed that the proposed circuits provide improvements in comparison with other circuits in terms of area.

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