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Fault-Tolerant Design of a Shift Register at the Nanoscale Based on Quantum-dot Cellular Automata

Sonia Afrooz[1] **· Nima Jafari Navimipour**[1]

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Abstract Quantum-dot Cellular Automata (QCA) as a novel technology in the nanometer scale has been considered as one of the substitutes to CMOS technology. The QCA helps to create faster computers with lower power consumption. On the other hand, a shift register as one of the most important logical circuit in the digital systems consists of a line of latches. Also, the QCA-based designs have more advantages compared to the conventional CMOS designs. However, some deposition defects are possible to occur in the QCA-based designs, which have necessitated the fault-tolerant structures. Therefore, this paper aims to design an optimized 2-bit universal shift register based on QCA technology through the optimized multiplexer and D flip-flop. This paper studies the functionality and the fault tolerance of the proposed universal shift register in the presence of the QCA deposition faults. The structure of the 2-bit universal register is extendable to 4-bit, 8-bit and higher. The proposed design has better performance regarding fault tolerant, complexity and area consumption compared to the current designs based on the achieved results via QCADesigner.

Keywords Universal shift register · Quantum-dot cellular automata (QCA) · Fault-tolerant · Multiplexer

1 Introduction

Quantum-dot Cellular Automata (QCA) is an innovative technology that promotes potential improvements over performance obtained through conventional Complementary Metal–Oxide Semiconductor (CMOS) operation [1–4]. It is considered as a developing technology to meet energy efficient strategy of logic circuits [5–7]. A four-dot squared cell is the basic element of the QCA that contains two free, equal charges [8–10]. These electrons involve

✉ Nima Jafari Navimipour
jafari@iaut.ac.ir

[1] Department of Computer Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran

the dots diagonally because of the Coulombic interaction [2, 11, 12]. The QCA encodes binary data by the charges instead of current. Fast operation, low energy consumption, and small dimensions are considered as the advantages of the QCA circuits [13, 14].

On the other hand, a shift register is a form of the memory in which, cells are connected in a line. Each cell stores one bit of information and its contents are shifted to the next cell during each clock cycle [15]. Registers are an essential component in any digital devices to store digital information. Though there are numerous advantages provided by QCA, there are some challenges identified. Fabrication defects in the QCA technology cause to create defective cells in the substrate [16]. It is necessary to identify the types of errors to assess and improve the robustness of the QCA-based circuits, especially shift registers. Therefore, searching the source of errors in the QCA-based shift register operation and their relative probabilities of occurrence are very challenging. Despite the importance of the shift register in QCA-based designs, fault tolerance ability in the molecular shift register is not addressed properly in the literature.

Therefore, an efficient and reliable 2-bit Universal Shift Register (USR) based on the QCA technology is proposed in this paper. A Rotated Majority Gate (RMG) is used as the main factor in the proposed design because of its correct functionality in the face of misalignment and displacement faults [17]. The functionality of the RMG is based on the Coulombic interaction among four neighboring QCA cells, which depends on the accuracy and geometry of its implementation [18]. Also, the functionality of the RMG is evaluated under different deposition to investigate the correctness of the proposed circuit. Defect tolerance is attained by using this gate at a logic gate level, which is necessary for achieving an acceptable manufacturing yield [19].

The rest of this paper is organized as follows: some of the previous design approaches about shift register based on the QCA are surveyed in Section 2. The proposed method and its layers based on QCA are explained in Section 3. The simulation results using QCADesigner simulator are discussed in Section 4. Finally, conclusions are provided in Section 5.

2 Related Work

The previous works presented several QCA-based shift register designs. An architecture of shift-register based on QCA has been presented in [20] where it maintains data in a stable conformation. The memory architecture is based on a current dual-phase synchronized and line-based one-bit memory cell block. It provides size, density and latency developments over some one-bit memory cells through its efficient clocking scheme. Also, it maintains data indefinitely by applying opposite values to the two inputs. A row enable signal is defined for each row to permit the read/write operations. An XNOR gate is used to apply opposite values to control inputs of the dual-phase and line-based memory cell for read/write operation. However, shift-register memory architecture needs extra circuitry to reserve the stored value after a read operation. Furthermore, the fault-tolerance features of the proposed method are not discussed.

Moreover, a new architecture for asynchronous registers in Null Convention Logic (NCL)**,** as a solution to the “layout = timing” problem in the QCA circuits has been proposed in [21]. The TH_{22} and TH_{12} gates are considered as the main elements of the NCL register. The TH_{22} gate can be implemented with a majority gate and the feedback to one of its inputs. The TH_{12} gate is the same as OR gate and can be implemented employing a majority gate with one of its inputs fixed at ‘1’. The NCL register leads to having a great reduction in the number of QCA cells required to implement an asynchronous NCL register. New

NCL register used to design a serial adder to prove the working of the proposed register in a sequential circuit. So, the proposed design is an efficient way to ease the "layout = timing" problem in QCA circuits. Even though sequential circuit designed with the new NCL needs a careful layout design to obtain correct timing, it can be interfaced with other circuitry without worrying about the layout affecting timing. Therefore, the "layout = timing" problem is not solved locally. Also, the fault-tolerance features are not considered in this design.

A new design of QCA-based 8-bit USR using 4 × 1 multiplexer and D-FF implementation has been proposed in [16]. The proposed 8-bit USR consists of eight 4 × 1 multiplexers and eight D-FFs. If the outputs of the shift register are available, then the serial input data may be outputted in parallel from the flip-flop. Also, the multiplexers and D-FF in [16] have the low complexity, area and delay compared to some previous designs. They may be utilized in processors designing for speed enhancement or digital communication. However, cell missing and possible defects occurrence in the proposed 8-bit USR are not considered.

Furthermore, Purkayastha, De [22] have proposed a modified design of 4-bit and 8-bit USR. At first, QCA layouts of D flip-flop with clear input and 4 to 1 multiplexer are used to design 4-bit and 8-bit USR. The proposed QCA-based USR takes serial data as inputs and performs both left and right shift operation upon them. This is decided by the 4 to 1 multiplexer circuits. There is a 4 to 1 multiplexer and a D flip-flop for each bit of the shift register. The proposed USR layout has an intense reduction of complexity, area and clock cycle delay in comparison with the previous design. The 8-bit and 4-bit USR may find its application in processors with high speed of operation, and it may be extended to design n-bit URS using QCA.

Finally, Das and De [23] have proposed an optimized design of shift register based on QCA using a new QCA layout of D flip-flop. The QCA structure of 3-bit Serial-In-Serial-Out (SISO) shift register is realized by cascading three QCA-based D flip-flops. The output of one flip-flop is also utilized as an input to next flip-flop. All the flip-flops are acted by a shared clock, and all are also set or reset simultaneously. The proposed shift register also outperforms the existing designs by reducing cell count and increasing density. The power consumption is performed by the proposed design to show the low energy consumption of the circuit. Defects may occur in three conditions in the proposed shift register, including single missing cell, single additional cell, and misalignments of the cell. They result in producing defective cells in the substrate.

Table 1 shows the summarization and comparison of the most important advantages and disadvantages of the discussed QCA-based shift registers.

3 Proposed Design

The USR as one of the most applicable and important electronic circuits is based on the QCA technology. The 4×1 multiplexer and D-FF are the essential modules in designing USR. Left and right shift are performed by the shift register, and the multiplexer is employed to select one operation at a time. Recently, great progress has been made in the molecular manufacturing of QCA in which each QCA cell is a molecule. Defects can occur in both phases of chemical synthesis and deposition phase during manufacturing. The defects occur in the deposition phase more than chemical synthesis phase, which causes to create defective cells in the substrate. In the USR, the faults can occur at two places: 2 × 1 Multiplexer and D-FF. The RMG is made by a symmetrical rotation of up to 45° of the inputs and output around the central cell, which does not affect the performance of the majority gate and is completely robust. This gives an important degree of freedom for synthesizing designs based

Table 1 Summarization of the discussed QCA-based register and their advantages and disadvantages

Paper	Main idea	Advantages	Limitation
Taskin, Chiu [20]	A QCA design of an n×m bit, serial-access, and shift-register based memory architecture	• Size improving • Latency improving • Denser implementation • Read/Write latency improving • Regularity in clock zone alignments	• Requiring the additional circuit to preserve the stored value after a read operation • Low fault tolerance
Katti and Shrestha [24]	A new architecture to implement an asynchronous NCL register alleviating the "layout = timing" problem	• Reducing the cell number • Not fault tolerance	• Locally the "layout = timing" problem is not solved
Sabbaghi-Nadooshan and Kianpour [16]	Designing and simulation of an extendable 2 × 1 multiplexer and 8-bit USR in QCA technology	• Complexity improving • Delay improving • High-speed function	• Cell missing • Occurring the faults
Purkayastha, De [22]	Designing and simulation of 4 and 8-bit USR in QCA utilizing a modified and efficient design of 4 to 1 multiplexer and D-Flip-flop	• Low cell count • Low area consumption • Low clock cycle delay	• Faults can occur • Cell missing • Power dissipation
Das and De [23]	Design and implementation of 3-bit SISO shift register in QCA using an optimized design of D flip-flop	• Low cell count • Low energy consumption • High density • Stability under thermal randomness	• Single missing cell • Single additional cell • Misalignments of cell

on QCA, as RMG can be used as the Original Majority Gate (OMG) block. Few studies are performed to investigate the properties of QCA-based fault designs, and a comprehensive comparison between the OMG and the RMG is given in [18, 25]. The comparison shows that the RMG has higher fault tolerance capability. It is based on the fact that when the rotation of all input and output cells around the center cell, electrostatic revulsion among the electrons of the cells, the inner cells influence the outcome to the durable polarization. However, the OMG is more dependent on the middle input (B) than the other inputs both regarding displacement and misalignment. But, in the RMG, this dependency can be entirely changed according to the degree of rotation. A design that makes use of the RMG instead of OMG is proposed to make a shift register more efficient with fault tolerant. The RMG and the original device have the same logic-level behavior. Two 3-input QCA majority gates, which are the OMG and the RMG, are depicted in Fig. 1a and b, respectively.

Timing in QCA is performed by clocking at four distinct and cascaded phases to synchronize the QCA cells. This strategy is used to facilitate adiabatic switching and thus a reliable circuit [26]. Not only does clocking control the information flow but also supplies the real power in QCA [27]. Each clock signal has a phase shifted by $\pi/2$. The four clock phases are a switch, hold, release and relax as shown in Fig. 2. During the switch phase, the cell polarization process starts by raising barriers and continues until the cell becomes polarized. During the hold phase, the barriers remain to their greatest extent, fix the polarization state of QCA cell and affect its neighbor. During release phase, the barriers are lowered, and reduction in the cell polarization occurs. Finally, in the relax phase, the cell barriers remain in their lowest extent, and the cell becomes unpolarized [28–30].

In the QCA memory architecture memory must be kept in motion in which the value of stored data moves through different cells. So, D-FF is used in the proposed design because of its simplicity. The basic D-FF of this architecture is shown in Fig. 3. The data bit is stored in a loop until the CLK control signal is low. When CLK increases, the input bit is stored in the loop. The right AND gate is called an enable gate and works independently from the rest of the circuit. The truth table of D-FF is shown in Table 2.

The D-FF is performed in this article using 62 cells and in an area of 0.10 μm^2. Figure 4 shows the layout of the D-FF according to its operations in Table 2. It has is 1.75 clock cycle (7 phases) delay by considering its performance.

Also, a multiplexer lets a system to choose one of the several input signals and forward it to the output. It is used as a switch because of this capability. The signal selection forwarded to the output of the multiplexer is made by the selection lines. The 4× 1 multiplexer has been

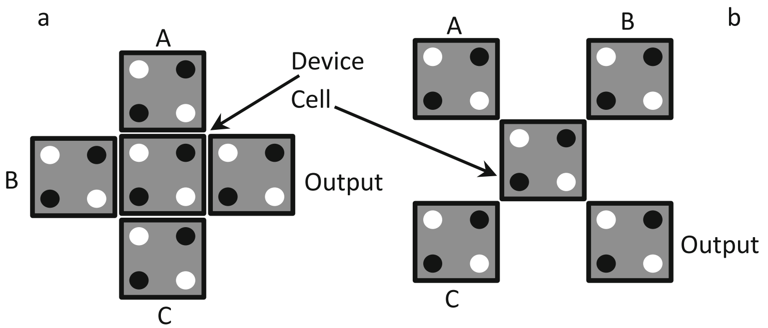

Fig. 1 Two types of 3-input majority gate, **a** OMG, **b** RMG [17]

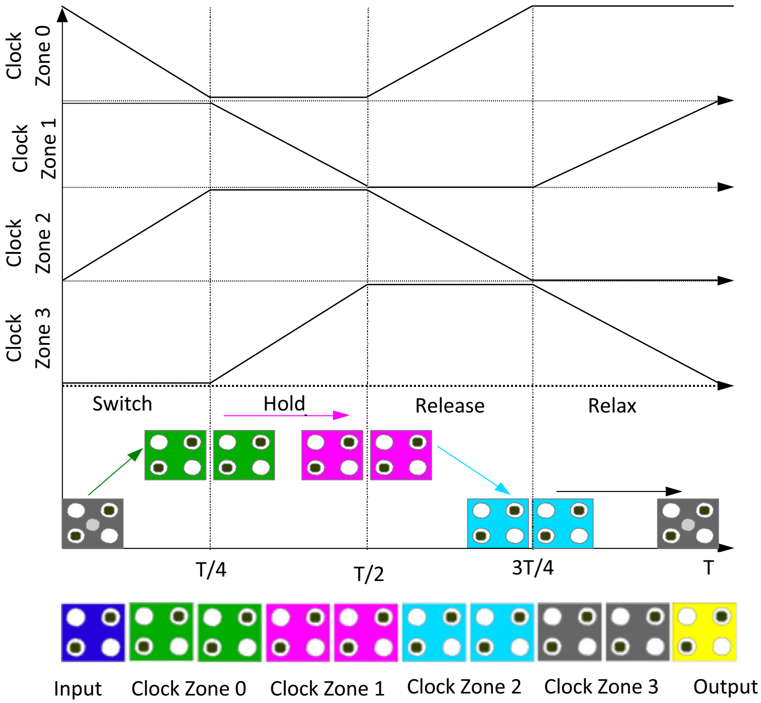

Fig. 2 Four phases of the QCA clock [31]

Fig. 3 Basic D-FF

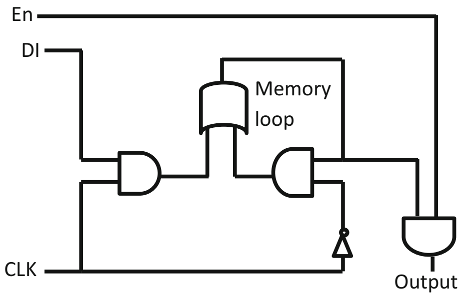

Table 2 D-FF operation

CLK	EN	DI	Memory-loop	Output
0	0	X	Unchanged	0
0	1	X	Unchanged	Stored value
1	X	0	0 (next cycle)	Don't care
1	X	1	1 (next cycle)	Don't care

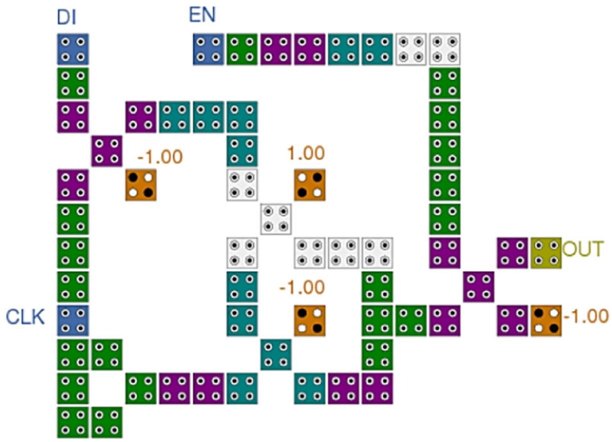

Fig. 4 Proposed D-FF implemented in QCA

implemented with three 2×1 multiplexers and used as a module. The signals from In_1 to In_4 are the four input signals and the selection lines S_0, S_1 are used to select one of the four inputs. Figure 5 represents the 4×1 multiplexer modular block implementation in the QCA that is implemented by applying modules of the 2×1 multiplexer. The logical functionality is as follows: If the S_0, S_1 rails are 00, 10, 01, 11, the outputs are set to In_1, In_2, In_3, In_4.

Figure 5 represents the implementation of the QCA-based 4×1 multiplexer in an area of 0.26 μm^2 and 161 cells. In Fig. 6, the delay of the 4×1 multiplexer is equal to 2.75 clock cycles (11 phases). As specified in the figure, In_1 to In_4 imply the multiplexer inputs and S_0 and S_1 show the selector lines of the 4×1 multiplexer. The S_0 and S_1, as one of the four inputs, are selected and transmitted to the output based on the selection lines.

A fault-tolerant USR is explained in the rest of this section using QCA technology. The S_1 and S_0 control the different operations of the registers. The list of different actions with their corresponding combinations is shown in Table 3. If the outputs of the D-FF are available, then the serial input data may be outputted in parallel from D-FF output by shifting. If the register can be shifted in two directions and loaded parallel, it is mentioned as a USR. The shifting operation is activated one at a time i.e. either right or left shift can be performed at a time. This is decided by the 4×1 multiplexer circuits. Thus, the block diagram of a 2-bit USR consisted of two 4×1 multiplexers, and two D-FF is observed in Fig. 7.

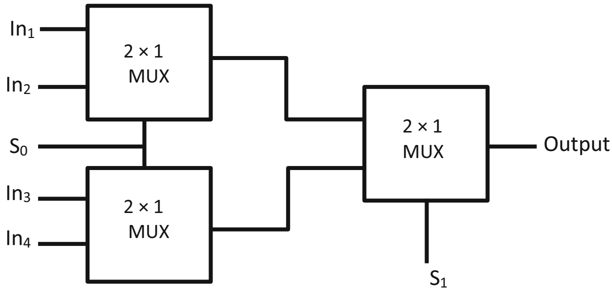

Fig. 5 4× 1 multiplexer modular block implemented in QCA

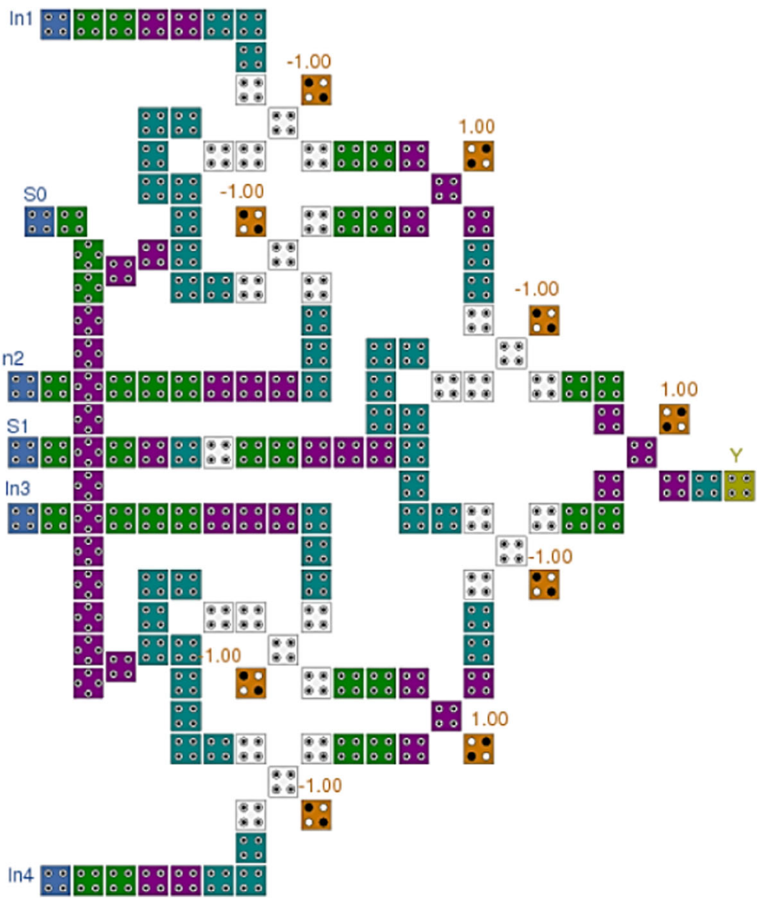

Fig. 6 Proposed 4 to 1 multiplexer implemented in QCA

Two 4×1 multiplexers have two common selectors (S_0 and S_1). When S_1S_0 = '00', the present value of the register is applied to D-FF inputs. This status creates a path from each D-FF output to its input. Therefore, the previously stored value of D-FF is increased by transmitting a signal. When S_1S_0 ='01', the input In_2 of multiplexers has a path to D-FF inputs. This causes right shift operations with the serial input transferred into In_2. When S_1S_0 ='10', a left shift operation occurs and the other serial input is transmitted to In_1. Ultimately, when S_1S_0 ='11', the binary data on the parallel input lines is transferred into the register simultaneously. Figure 8 shows the performance of the presented QCA-based

Table 3 Different mode of operations of 2-bit USR

S_1	S_0	Register operation
0	0	Unchanged
0	1	Shift right
1	0	Shift left
1	1	Parallel load

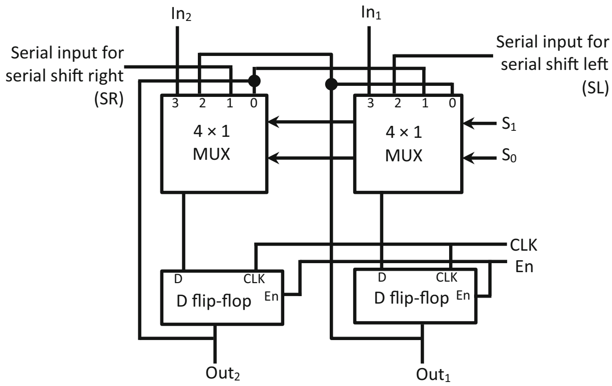

Fig. 7 Block diagram of 2-bit USR

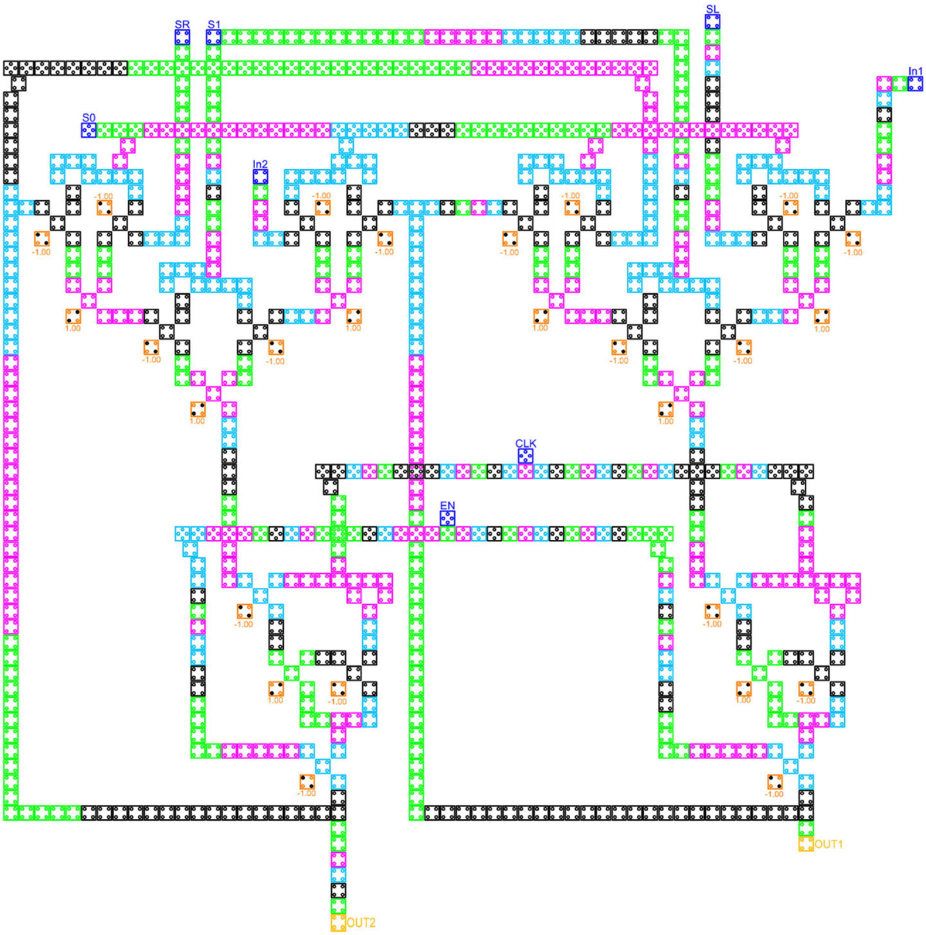

Fig. 8 Proposed 2-bit USR implemented in QCA

2-bit USR in an area of 1.45 μm^2 and 769 cells. Maximum 6.25 clock cycles (25 phases) is needed to get the first output irrespective of the S_1S_0 combination. Coplanar crossover is used for the crossing of wire in the 2-bit USR. The coplanar design uses both regular and rotated types of cells. If they are aligned properly, then these two kinds of cells do not affect each other's signals. So, it is possible to create a large and simple layout in a single layer.

4 Simulation Results and Discussion

This section presents the simulation results of the proposed USR circuit. The simulation tools, simulation parameters, accuracy analysis and comparisons with existing layouts are discussed in this section.

4.1 Simulation Tool

QCADesigner is used to create an accurate simulation and layout tool for QCA. It can simulate complex QCA circuits on most standard platforms [32]. Now, QCADesigner has three distinct simulation engines available. Each of the three engines has a diverse and important set of advantages and disadvantages. The first is a digital logic simulator in which cells are considered to be either null, logical one, or logical zero. A nonlinear approximation engine as a second engine uses the nonlinear cell-to-cell response function to define the stable state of the cells within a design. The third uses a two-state Hamiltonian to realize the full quantum mechanical model. Therefore, it is used to simulate the proposed design.

4.2 Simulation Parameters

The designs of the proposed layout in the previous section have been performed on QCADesigner Ver. 2.0.3 and are simulated using the bistable approximation simulation engine with default parameters. A short explanation of each parameter used for a simulation engine is presented in Table 4.

Table 4 Parameters model in the QCADesigner simulator

Parameter	Value
Cell Width	18 nm
Cell height	18 nm
Dot diameter	5 nm
Number of samples	50000–1000000
Convergence tolerance	0.001000
Radius of effect	65.000000 nm
Relative permittivity	12.900000
Clock high	9.800000e–22 J
Clock low	3.800000e–23 J
Clock shift	0.000000e+000
Clock amplitude factor	2.000000
Layer Separation	11.500000 nm
Maximum iteration per sample	100

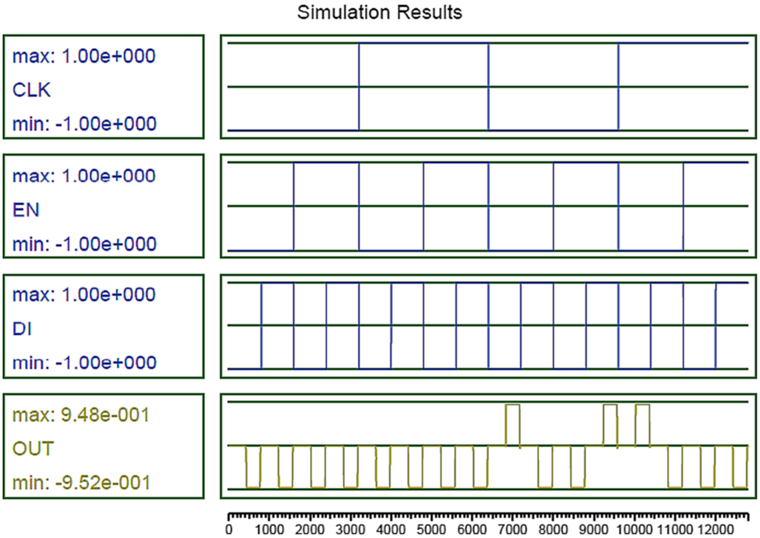

Fig. 9 Simulation results of D-FF

4.3 Accuracy Analysis

Figure 9 depicts the simulation of D-FF in QCADesigner. It takes 1.5 clock cycles that results get output correctly. When EN is “1”, the output is enabled and when EN is “0”, the

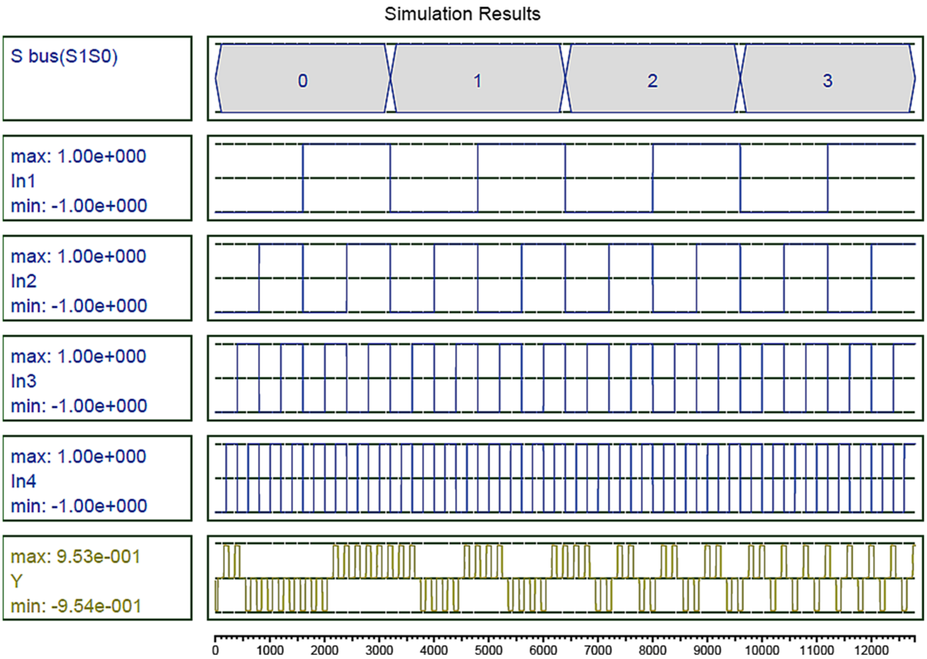

Fig. 10 Simulation results of the 4 to 1 multiplexer

output is “0”. When CLK is “1”, write state is enabled and data value save in memory loop and when CLK is “0”, read state is enabled and saved a bit is placed on output. The result is confirmed via the truth table as shown in Table 2. This confirmation shows the accuracy of the circuit.

Figure 10 shows the simulation of the 4×1 multiplexer. The delay is 2.75 clock cycles according to the simulation results. Four waveforms with different frequencies are applied to inputs In_1, In_2, In_3 and In_4 and the multiplexer outputs the signal at In1 when select bus S_1S is at 00 and outputs the signal at In_2 when S_1S is at 01. The multiplexer outputs the signal at In_3 when S_1S is at 10 and outputs the signal at In_4 when S_1S is at 11.

To confirm the operation of the 2-bit USR, the bit string is implemented and simulated for all combinations of the EN and CLK inputs of the D-FFs and selected bus (S_0S_1) of 4 to 1 multiplexers. The simulation result of the 2-bit USR is shown in Fig. 11. It can be seen from the simulation result that when S_1S_0 =11, the 2-bit USR performs parallel load

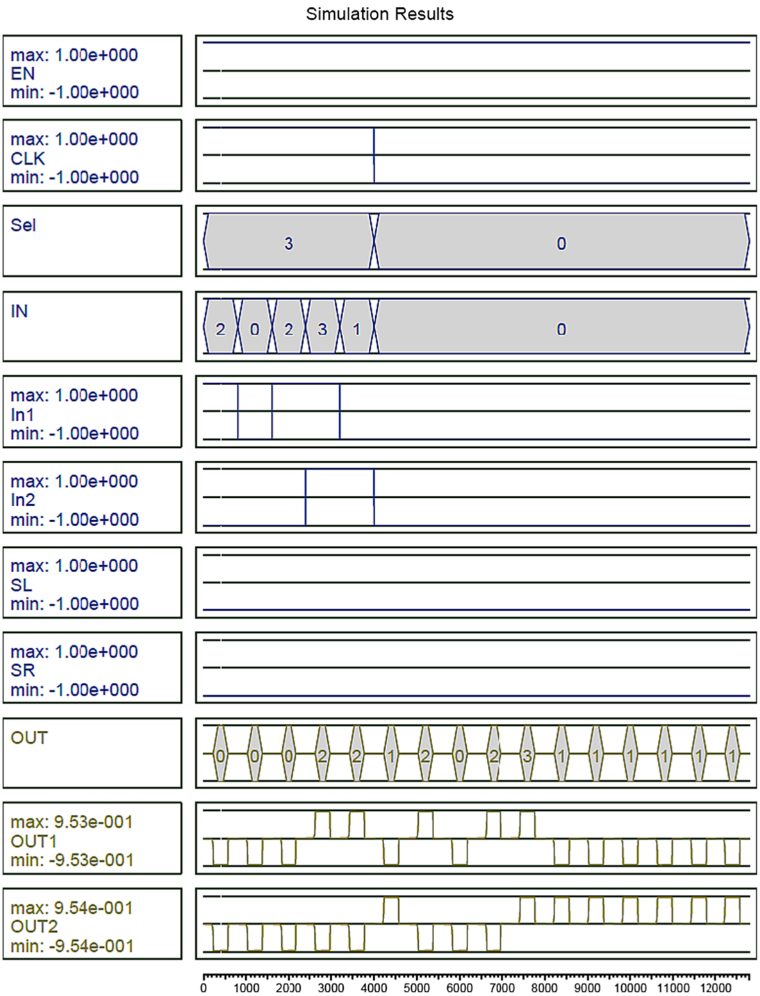

Fig. 11 The simulation of the 2-bit USR, when S1S0=“11 & 00”

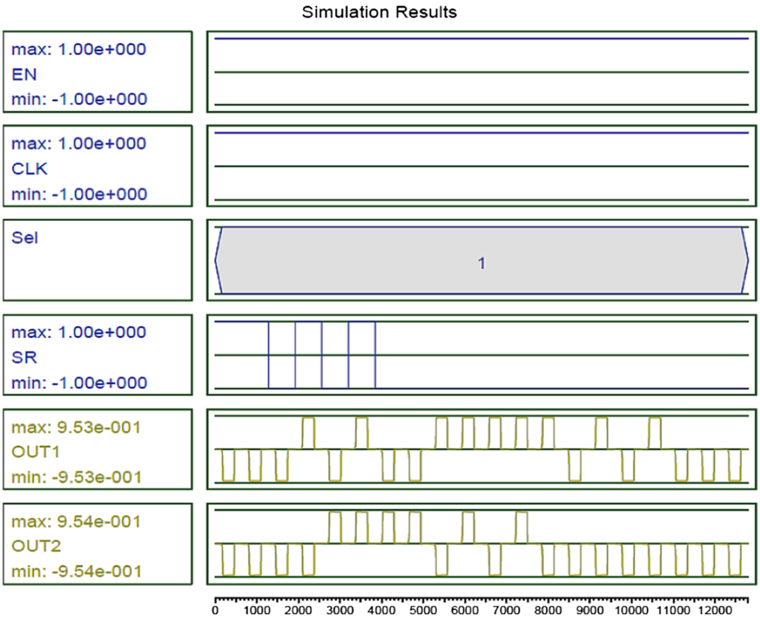

Fig. 12 The simulation of the 2-bit USR, when S_1S_0 =“01”

operation with a delay of 6.25 clock cycles and when S_1S_0 =00, the previously stored data are fed to the D-FF through the feedback path. The parallel load input is 2, 0, 2, 3, and 1. The simulation output shows that the output is the same as the input when S_1S_0 = ‘11’. When S_1S_0 = ‘00’, the previously stored data of register are latched to D-FF inputs with the control line combination. The maximum delay is 6.25 clock cycle.

Figure 12 shows the simulation result of right shift operation when S_1S_0 = ‘01’. The serial input ‘110101’ is applied to the input line 1 (SR) of the leftmost multiplexer, and then the simulated output is observed from Out_2 and Out_1, respectively. Out_2 has 6.25 clock cycles delay and Out_1 has 11.25 clock cycles delay. Also, the left shift operation occurs with the serial input string ‘110101’ and with the select line combination S_1S_0 = ‘10’. The input is applied to the serial input line 1 (SL) of the right multiplexer. The first simulated output is collected from Out_1 with 6.25 clock cycles delay and then from Out_2 with 12.25 clock cycles delay. Figure 13 shows the left shift operation of 4-bit USR.

4.4 Comparisons

The RMG accurate functionality is in the face of cell misalignment and cell displacement faults. In kind of cell misalignment, the defective cell is not properly aligned with its neighboring cells. In other words, the defective cell gets nearer to one or some cells and away from the others. When a cell is not placed in its original direction, cell displacement fault occurs. A program which imposes some cell displacement defects in the QCA circuit randomly has been generated to evaluate the proposed design. The program receives the layout file of QCA circuit generated by QCADesigner and some of the defects as inputs. Then, it displaces some cells randomly. The output file is the desired number of cell displacement defects. For each number of defects, the program has been performed 50 times, and the fault tolerance is estimated. The amount of cell displacement is assumed as 7 nm. Only the

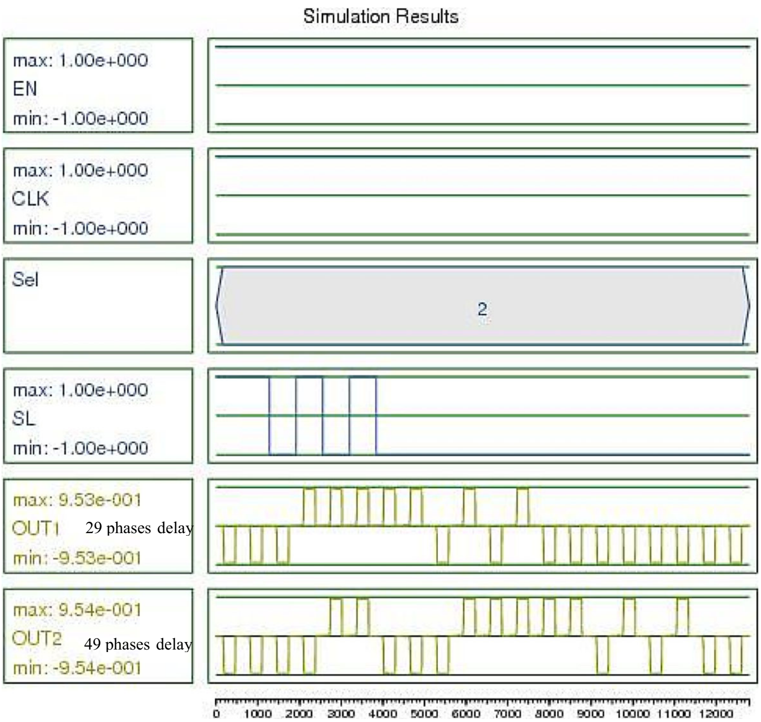

Fig. 13 The simulation of the 2-bit USR, when S_1S_0 =“10”

output, which functions true and reaches the required maximum signal level is considered as true output. In the following, some cell misalignment defects are imposed in the QCA circuit randomly to assess

circuit in the face of cell misalignment defect. Table 5 presents a comparative study of USR proposed in this paper with that proposed in [16, 22] regarding fault tolerance properties.

The proposed design based on RMG has fault tolerant attribute regarding misalignment and displacement faults compared to the previously proposed designs as shown in Table 5. Missing cell defect is likely to occur at proposed shift register because it is designed in a single layer and is not applied for cell redundancy. A comparative analysis of the proposed design is performed considering the previously proposed designs. The comparison of USR presented in this paper with other papers presented in [16, 22] is shown in Table 6 regarding area, complexity, and delay.

In the compared structures the multilayer design is used in [22], and the signal distribution network (SDN) method is used in [16] for wiring. There exist tree techniques for wiring 90 to 90 in the proposed structure: multilayer crossover, Signal Distribution Network (SDN) and wire-crossing using the difference of clock phase. The multilayer crossover technique uses a crossover bridge method. This technique is constructed by adding more layers, and the QCA signal passes through the upper layer. Using the multilayer crossover the number of cells increases in crossover area but delay remains unchanged. SDN block can accept an arbitrary number of inputs and yield an equally arbitrary number of distributed signals. So using the SDN method the implementation of proposed design divided into two parts: signal distribution network and combinational logic gates. This method requires a diversity

Table 5 A comparative study of the USRs in terms of fault tolerance properties

USR	1 cells defect		5 cells defect		10 cells defect		25 cells defect	
Defect	Displacement	Misalignment	Displacement	Misalignment	Displacement	Misalignment	Displacement	Misalignment
Proposed design in this paper	82%	70%	70%	62%	54%	48%	20%	12%
Proposed design by [16]	44%	34%	22%	20%	10%	10%	0%	0%
Proposed design by [22]	40%	28%	20%	16%	10%	6%	0%	0%

Table 6 Comparison between 2-bit USR presented in this paper with previous designs

2-bit USR	Proposed in this paper	Design proposed by [16]	Design proposed by [22]
Area (μm^2)	1.45 μm^2	1.76 μm^2	0.88 μm^2
Complexity (#cell)	769	933	550
Maximum delay (clock cycle)	6.25	8.75	4

of clocking regions that range in size from a single cell up to dozens of cells. Hence, it increases the number of cells and delay. Another type of coplanar wire crossing that uses 90° cells is based on the difference of 180 degrees between two non-adjacent clock regions. Moreover, the additional tasks which are the rotation, translation of QCA cells, and the consideration of the number of sub-layers are not necessary. Using this method the number of cells remains unchanged, but the delay is increased. The reason for increasing the number of the clock in the proposed structure is because clocking has to be controlled using this method.

5 Conclusion and Future Work

Fault-tolerant design of QCA logic circuits is necessary to replace CMOS technology. This paper presents, a new extendable and efficient design of 2-bit USR with fault tolerance attribute in QCA technology using an efficient 4×1 multiplexer and D-FF implementation to perform four actions: Remaining in an unchanged state, shift to the right, shift to left and parallel load. The 4 ×1 multiplexer and D-FF have been used as the basic modules to design USR. This study explores a fault tolerance method in designing USR by replacing RMG instead of OMG. Hence, a robust configuration is provided for cells due to its tolerance to misalignment and displacement defects. This new structure is an optimal design compared to previous works. A significant improvement has been achieved according to the comparisons and evaluations regarding the numbers of defects imposed by the circuit. But, the proposed design cannot tolerate the performed missing cell defect. Finally, the comparison of area, complexity, and delay with other structures for 2-bit USR based on QCA is done in this paper.

The high robustness of this USR can be used to assign the most commonly utilized fault-tolerant arithmetic circuits in the future. These circuits are the building block of nano processors in which the nanodevices are provided for the future. Moreover, it may be extended to the n-bit USR.

References

1. Barughi, Y.Z., Heikalabad, S.R.: A three-layer full adder/subtractor structure in quantum-dot cellular automata. Int. J. Theor. Phys. **56**(9), 2848–2858 (2017)
2. Gadim, M.R., Navimipour, J.N.: Quantum-dot Cellular Automata in Designing the Arithmetic and Logic Unit Systematic Literature Review Classiffication and Current Trends. J. Circ. Syst. Comput. **27**(10), 1830005 (2018)
3. Sherizadeh, R., Navimipour, N.J.: Designing a 2-to-4 decoder on Nano-scale based on quantum-dot cellular automata for energy dissipation improving. Optik - International Journal for Light and Electron Optics (2018)

4. Moharrami, E., Navimipour, N.J.: Designing nanoscale counter using reversible gate based on quantum-dot cellular automata. Int. J. Theor. Phys. **57**(4), 1060–1081 (2018)
5. Gupta, N., Choudhary, K., Katiyal, S.: Two bit arithmetic logic unit (ALU) in QCA. Int. J. Recent Trends Eng. Technol. **8**(2), 35 (2013)
6. Mohammadi, Z., Mohammadi, M.: Implementing a one-bit reversible full adder using quantum-dot cellular automata. Quantum Inf. Process **13**(9), 2127–2147 (2014)
7. Seyedi, S., Navimipour, N.J.: An optimized design of full adder based on nanoscale quantum-dot cellular automata. Optik - Int. J. Light Electron Opt. **158**, 243–256 (2018)
8. Gadim, M.R., Navimipour, N.J.: A new three-level fault tolerance arithmetic and logic unit based on quantum dot cellular automata. Microsyst. Technol. **24**, 1–11 (2018)
9. Karkaj, E.T., Heikalabad, S.R.: Binary to gray and gray to binary converter in quantum-dot cellular automata. Optik - Int. J. Light Electron Opt. **130**, 981–989 (2017)
10. Tougaw, D., Szaday, J., Will, J.D.: A signal distribution grid for quantum-dot cellular automata. J. Comput. Electron. **15**(2), 446–454 (2016)
11. Khan, A., Chakrabarty, R., De, D.: Static hazard elimination for a logical circuit using quantum dot cellular automata. Microsyst. Technol. **23**(9), 4169–4177 (2017)
12. Afrooz, S., Navimipour, N.J.: Memory Designing Using Quantum-Dot Cellular Automata: Systematic Literature Review, Classification and Current Trends. J. Circ. Syst. Comput. **26**, 1730004 (2017)
13. Naji Asfestani, M., Rasouli Heikalabad, S.: A unique structure for the multiplexer in quantum-dot cellular automata to create a revolution in design of nanostructures. Physica B **512**, 91–99 (2017)
14. Zhang, Y. et al.: Modular design of QCA carry flow adders and multiplier with reduced wire crossing and number of logic gates. Int. J. Circ. Theory Appl. **44**(7), 1351–1366 (2016)
15. Hopfield, J., Onuchic, J.N., Beratan, D.N.: A molecular shift register based on electron transfer. Science **241**(4867), 817–820 (1988)
16. Sabbaghi-Nadooshan, R., Kianpour, M.: A novel QCA implementation of MUX-based universal shift register. J. Comput. Electron. **13**(1), 198–210 (2014)
17. Roohi, A., DeMara, R.F., Khoshavi, N.: Design and evaluation of an ultra-area-efficient fault-tolerant QCA full adder. Microelectron. J. **46**(6), 531–542 (2015)
18. Momenzadeh, M., et al.: Quantum cellular automata: New defects and faults for new devices. In: Proceedings of 18th International on Parallel and Distributed Processing Symposium, IEEE (2004)
19. Vankamamidi, V., Lombardi, F.: Design of defect tolerant tile-based QCA circuits. In: Proceedings of the 18th ACM Great Lakes symposium on VLSI, ACM (2008)
20. Taskin, B. et al.: A shift-register-based QCA memory architecture. ACM J. Emerg. Technol. Comput. Syst. (JETC) **5**(1), 4 (2009)
21. Katti, R., Shrestha, S.: Novel Asynchronous Registers for Sequential Circuits with Quantum-Dot Cellular Automata. In: 2012 IEEE International Symposium on Circuits and Systems (ISCAS), IEEE (2012)
22. Purkayastha, T., De, D., Chattopadhyay, T.: Universal shift register implementation using quantum dot cellular automata. Ain Shams Engineering Journal (2016)
23. Das, J.C., De, D.: Operational efficiency of novel SISO shift register under thermal randomness in quantum-dot cellular automata design. Microsyst. Technol. **23**(9), 4155–4168 (2017)
24. Katti, R., Shrestha, S.: Novel Asynchronous Registers for Sequential Circuits with Quantum-Dot Cellular Automata. In: 2012 IEEE International Symposium on Circuits and Systems, IEEE (2012)
25. Tahoori, M.B., et al.: Defects and faults in quantum cellular automata at nano scale. In: 2004 Proceedings of 22nd on VLSI Test Symposium, IEEE (2004)
26. Lent, C.S., Isaksen, B.: Clocked molecular quantum-dot cellular automata. IEEE Trans. Electron Devices **50**(9), 1890–1896 (2003)
27. Kianpour, M., Sabbaghi-Nadooshan, R.: Optimized Design of Multiplexor by Quantum-dot CellularAutomata. Int. J. Nanosci. Nanotechnol. **9**(1), 15–24 (2013)
28. Lent, C.S., Tougaw, P.D.: A device architecture for computing with quantum dots. Proc. IEEE **85**(4), 541–557 (1997)
29. Cho, H., Swartzlander, E.E. Jr.: Adder and multiplier design in quantum-dot cellular automata. IEEE Trans. Comput. **58**(6), 721–727 (2009)
30. Kianpour, M., Sabbaghi-Nadooshan, R.: A conventional design and simulation for CLB implementation of an FPGA quantum-dot cellular automata. Microprocess. Microsyst. **38**(8), 1046–1062 (2014)
31. Sen, B. et al.: Modular Design of testable reversible ALU by QCA multiplexer with increase in programmability. Microelectron. J. **45**(11), 1522–1532 (2014)
32. Walus, K. et al.: QCADEsigner: A rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans. Nanotechnol. **3**(1), 26–31 (2004)