

QCA Gray Code Converter Circuits Using LTeX Methodology

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Abstract The Quantum-dot Cellular Automata (QCA) is the prominent paradigm of nanotechnology considered to continue the computation at deep sub-micron regime. The QCA realizations of several multilevel circuit of arithmetic logic unit have been introduced in the recent years. However, as high fan-in Binary to Gray (B2G) and Gray to Binary (G2B) Converters exist in the processor based architecture, no attention has been paid towards the QCA instantiation of the Gray Code Converters which are anticipated to be used in 8-bit, 16-bit, 32-bit or even more bit addressable machines of Gray Code Addressing schemes. In this work the two-input Layered T module is presented to exploit the operation of an Exclusive-OR Gate (namely LTeX module) as an elemental block. The “defect-tolerant analysis” of the two-input LTeX module has been analyzed to establish the scalability and reproducibility of the LTeX module in the complex circuits. The novel *formulations* exploiting the operability

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of the LTeX module have been proposed to instantiate area-delay efficient B2G and G2B Converters which can be exclusively used in Gray Code Addressing schemes. Moreover this work formulates the QCA design metrics such as O-Cost, Effective area, Delay and $Cost_{\alpha}$ for the n-bit converter layouts.

Keywords Quantum-dot cellular automata · Gray code addressing · Binary to gray and gray to binary converters · Layered T gate · O-Cost · $Cost_{\alpha}$

1 Introduction

The charge flow in a circuit in terms of electronic orientation instead of traditional current flow is a good solution to avoid the approaching limits of empirical CMOS (Complementary Metal Oxide Semiconductor) technology. The Quantum-dot Cellular Automata (QCA) devise a device that makes the use of Quantum Effects and carries information through the circuit by using the electron orientations either as “+1” or “-1”. As a result, the QCA technology achieves an extreme high packing density, a high speed operation in terra hertz and low power dissipation during its operation [1–3]. Although the researchers have synthesized several techniques for efficient memory designs [4–7] in the relevant field, there exists the need for the design of the efficient converter which would be extremely helpful in successive type processor designs. Even though the Binary to Gray (B2G) and Gray to Binary (G2B) converters are available for wide range of applications [8, 9], the existing QCA B2G and G2B Converters [10–19] are not designed for the applications of the Gray Code addressing. The address increments for 8-bit, 16-bit, 32bit and 64-bit machines are not implemented in the existing converters and as consequences, the designed converter for Gray Code Addressing could not be implemented with the help of these converters. This work has made an effort in designing the efficient B2G and G2B converters that would be best suitable for design of both 8-bit and higher order-bit addressable processor based architecture.

As the main component of the B2G and G2B Converters is Exclusive OR Gate, so the contribution of this work involves the QCA implementation of two-input Exclusive OR using Layered T Gate [20], namely LTeX module. A detailed analysis has been demonstrated by applying the process of defect tolerant analysis to confirm the scalability, robustness and endurance of the proposed two-input LTeX module. Next, the n-bit B2G and G2B Converters have been instigated with the help of two-input LTeX modules. In particular, the novel formulations have been introduced to achieve innovative realization of Gray converters which would explore the new paradigm specifically in Gray Code Addressing systems. A clear picture has been shown for the first time on the effectiveness of the converters in Gray Code Addressing. The proper functionality of these converters suitable for 8-bit and more than 8-bit addressable memories have been provided, simulated in QCADesigner [21] with n, number of input bits in Binary Address/Gray Address ranging from 4 to 16 and parameterized with the Gallium Arsenide based hetero structure design. The coherence vector engine has been used to validate the functionality of the layouts in this work.

The rest of the article is arranged as follows: Section 2 constitutes the background of QCA and discussed the existing QCA implementations of B2G Converters. The detailed structure, behavioral characterization and the defect tolerant nature of the two-input LTeX module is introduced in Section 3. The Cost analysis with modified equation of $Cost_{\alpha}$ has been discussed in Section 4. The proposed two-input LTeX module is extended in the design of n-bit B2G and G2B converter circuits by enunciating the novel *formulations* and

corollaries in Section 5. In addition, a pathway to generate generic (n-bit) modules has also been addressed in the stated sections. Section 6 discusses the obtained results, analyzes the $Cost_{\alpha}$ and shows analysis of the existing and proposed converter layouts. Finally Section 7 complies with conclusive discussions. The Fig. 1 proposes the organization of the entire work.

2 Background of QCA and Relevant Case Studies

2.1 QCA

The Quantum Cell is the elementary device of QCA [2, 3]. Figure 2a shows the Quantum Cell that has four dots at the corners of a square which can accommodate two mobile electrons within it. The inter-Columbic interactions between the electrons inside the cell and the intra-Columbic interactions of electrons from the neighbor cells force the inner electrons to occupy diagonal positions producing the polarization '+1' or '-1' as shown in Fig. 2b and c respectively. The mobile electrons can tunnel through the quantum dots within a square but cannot move to the neighbor cells because of higher potential barriers between the cells. The polarizations i.e. '+1' or '-1' of quantum cell interprets the information as logic 1 or logic 0 respectively. In QCA, the positional attributes of electrons represent the information in contrast to the traditional voltage or current flow of CMOS circuits.

Coupled quantum cells help in evaluating the information, form a level of Boolean circuit and forward the same to the next level to produce the proper output. The occupancy of quantum dots in the coupled cells is controlled by a back plane voltage, known as "clock zones". There are four clock zones as clock 0, clock 1, clock 2 and clock 3. These clock signals are phase shifted by 90° to their immediate precursors. The collective quantum cells

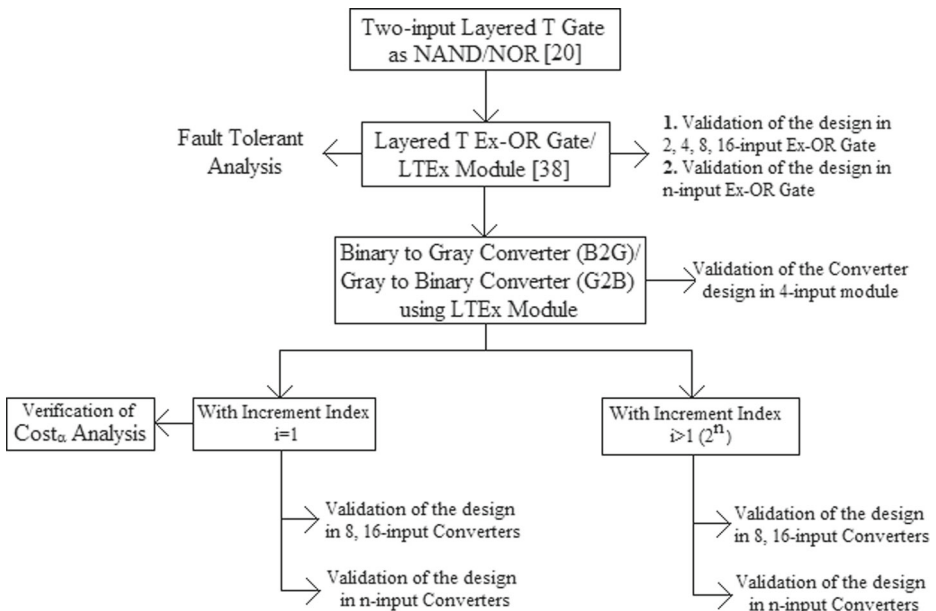
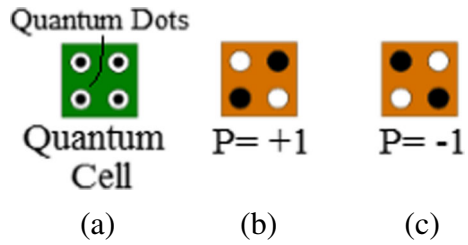


Fig. 1 The model of the proposed work

Fig. 2 a Quantum Cell, Quantum Cell with Polarization: b P= +1, c P= -1



are partitioned under the same clock zone and forward the intermediary outputs to the next level implementing the pipelined architecture [22]. The metallic-dot QCA becomes promising to operate at cryogenic temperatures [23] but the workability of molecular QCA [24], nano-magnet QCA [25] and semiconductor QCA [26] become more likely while operating at a room temperature operation [24–26]. The collective quantum cells methodize quantum Gates and interconnecting wires to design the complex multi-level Boolean circuits. From its’ invention, the QCA gets several logic gates like Majority Voter [27], conventional Inverter, Universal Logic Gate, Universal QCA Logic Gate [28], And-Or-Invert Gate (AOI Gate) [29], Coupled Majority-Minority Gate (CMVMIN Gate) [28], FNZ Gate, Khanday Gate [30], T Gate [31], but none of these implements Universal NAND/NOR function based methodologies as the Layered T Gate [20] did. The novel *formulations* described in the subsequent sections finds its better way during the implementation of the Gray Code addressing system [32, 33] based converter design process.

2.2 Literature Survey

The area-delay optimized B2G Converters play a pivotal role in the advancement of emerging nano communication circuits specifically in the field of Gray Code Addressing scheme [32, 33]. The successive Gray Codes show only one bit variation that leads to the less switching capacitance, less power dissipation in bus addressing system. As an example, the binary representations of 0 to 31 observe 31 bit changes, whereas the Gray Code representations of the same reflect 16 bit changes. There exist several architectures of QCA B2G Converters [10–19]. An n-input B2G Converter takes n-binary inputs, converts them into equivalent n-bit Gray Codes and generates the required outputs. Conversely the n-input G2B converter converts n-input Gray Code into equivalent Binary Code. The possible n-bit Binary and Gray inputs are asserted with B(n)B(n-1)... B(0) and G(n)G(n-1)... G(0) respectively. The 4-bit B2G Converter and G2B Converter, which are presented in [10], involve nine Majority Voters, three seven cell Inverter and coplanar wire crossings to complete the conversion process. Additionally, the Gray Converters presented in [11], uses nine Majority Voters, coplanar crossing and evaluates the 4-bit Gray Code output at clock 3. Another 4-bit converters with the continuous attempt to reduce O-Cost [31], effective area and Cost_α have been proposed in [12–14] exploiting the equations

$$G(3) = B(3), G(2) = B(3) \oplus B(2), G(1) = B(2) \oplus B(1), G(0) = B(1) \oplus B(0) \quad (1)$$

The Ahmed Converter [13] and Beigh Converter [14] optimize the two-input QCA Exclusive OR layouts by implementing B2G and G2B Converter circuits with the help of Majority Voters. These two Converters avoid the coplanar crossings and use two corner-cell arrangements instead of conventional seven-cell Inverter. The Waje Converter [12] instantiates CMVMIN Gate [28] which have been further extended to design the 4-bit B2G and G2B

Converters. To get the desired output $G(3)G(2)G(1)G(0)$, the Waje Converter takes binary inputs $B(0)$, $B(1)$, $B(2)$ and $B(3)$, implements the equations

$$\begin{aligned} G(3) &= B(3), \quad G(2) = \overline{MV(MV(B(3), B(2), -1), \overline{MV(B(3), B(2), 1)}, 1)}, \\ G(1) &= \overline{MV(MV(B(1), B(2), -1), \overline{MV(B(1), B(2), 1)}, 1)}, \\ G(0) &= \overline{MV(MV(B(0), B(1), -1), \overline{MV(B(0), B(1), 1)}, 1)} \end{aligned} \tag{2}$$

The QCA literature has possibly received its first contribution in designing the n-bit Gray Converter in [15]. This work exploits the (2) to design 4-bit B2G Converter design. In addition, the robustness of the Converter proposed in [15], is verified with its proper functionality in 8-bit, 16-bit, 32-bit and 64-bit B2G Converter circuits. Another 4-bit B2G Converter which uses nine Majority Voters and L-section binary wires is introduced in [16]. The B2G Converter presented in [17] starts implementing QCA designs from elementary 2-bit B2G Converter with the equations

$$G(1) = B(1), \quad G(0) = \overline{MV(MV(B(0), \overline{B(1)}, -1), \overline{MV(B(1), \overline{B(0)}, -1)}, 1)} \tag{3}$$

The proposed elementary unit has been proposed to generate 3-bit and 4-bit B2G Converter layouts. As the expression suggests, the Islam Converter needs three Majority Voters to implement 2-bit B2G Converter circuit. Hence, the Converter needs $3n$ numbers of Majority Voters to implement B2G Converter where n starts from 2. Recent trend of tiled Exclusive OR Gate structure [34] has been used by Karkaj et al. [18] where three 18-cell tiled Exclusive OR Gate generates 4-bit Gray Code $G(3)G(2)G(1)G(0)$ by using the expression (1). The non-reversible 4-bit Gray Code Converters use input and output cells abruptly within the layout which may increase the complexity in high fan-in circuits.

The proper analyses of QCA implementations of the existing converters show that the B2G and G2B Code conversions for the byte addressable processor without increments are possible. Unfortunately they are not capable to handle the 16-bit, 32-bit, 64-bit or even 2^{n-1} -bit addressable machines whereas the increment indexes are not equal to 1. Moreover, these designs do not show any pathway to implement generic (n-bit) B2G and G2B Converter designs as well.

3 LTeX Module

3.1 2-input LTeX Module

To grapple with higher order addressable processor architecture, the introduction of two-input Exclusive OR Gate design by using LT Gate [20] is necessary. The use of generic Exclusive OR Gate in Gray Code addressing which avoids significant number of bit-changing in the sequential memory access operations has been acknowledged in the literature. Therefore the QCA realization of the n-input Exclusive OR Gate design, for which two-bit elemental Exclusive OR Gate is inevitable, becomes quite obvious. An Exclusive OR Gate finds its application in the design of single bit Full Adder that takes two literals as inputs, computes the additive results between input literals and generates the “Sum” and “Carry” outputs. The trailing output “Sum” needs singular Exclusive OR Gate that can be cascaded to produce high fan-in Full Adder circuits [35]. Additionally the Exclusive OR Gate is extensively employed in Pseudo Random Number Generator modules [36], error detection and error correction circuits [37]. The two-input Exclusive-OR QCA implementation scalable up to the n-input design is introduced in [38]. This design of Ex-OR Gate using

Layered T Gate reports 18.75% less cell requirement and 6.20% reduced area requirement in [38] with respect to the existing conventional design. A high-level synthesis of elemental two-input Exclusive OR module using Layered T Gate is shown in Fig. 3.

As the QCA Layout of Exclusive OR gate requires Layered T Gate, so it is named as Layered T Exclusive OR Gate, abbreviated as LTeX module. The LTeX module includes four Layered T NAND (LT NAND) gates as given in Fig. 3a. The LT NAND1 takes two inputs A1 and A0 to produce intermediary output T1. The inputs A1, A0 along with the intermediary output T1 are connected to the input ports of LT NAND2, LT NAND3 respectively to produce second level intermediary outputs T2 and T3 from the LT NAND Gates. Lastly, these intermediary outputs T2 and T3 are inputted to LT NAND4 to generate the final output Z0. The clock signals are applied to quantum cells in an order of 0, 1, 2, 3 so that the intermediary outputs get evaluated for proper Exclusive OR output generation. The detailed mathematical equations of LTeX block are given as follows:

$$\begin{aligned}
 T1 &= L_T^+(A1, A0) \\
 T2 &= L_T^+(A1, L_T^+(A1, A0)) \\
 T3 &= L_T^+(A0, L_T^+(A1, A0)) \\
 Z0 &= LTeX(A1, A0) = L_T^+(T2, T3) \\
 &= L_T^+(L_T^+(A1, L_T^+(A1, A0)), L_T^+(A0, L_T^+(A1, A0))) \tag{4}
 \end{aligned}$$

The LTeX QCA layout is designed and simulated by QCADesigner tool [21] with the 18 nm * 18 nm cell dimension, 5 nm dot diameter, and 2 nm inter-cell distance. The 7X7 grid of Fig. 3b acquires 26 cells, 29346 nm² effective area and provides output at negative edge of clock 2. The output Z of two-input LTeX module which becomes logic ‘1’ upon anti-coincidence of the inputs A1 and A0, is evident in Fig. 4. The red-colored box of output Z is start-up time.

3.2 Defect Analysis of 2-input LTeX Module

This subsection presents the investigation of the defects of the tolerant nature of two-input LTeX module. The scalability, endurance and reusability of the proposed module would be unquestionable once the defect tolerant nature of the QCA layout is identified. The defects in the present stage of the QCA manufacturing are more likely to occur at the synthesis and deposition phase of fabrication. The defects at the synthesis phases which are fatal to the

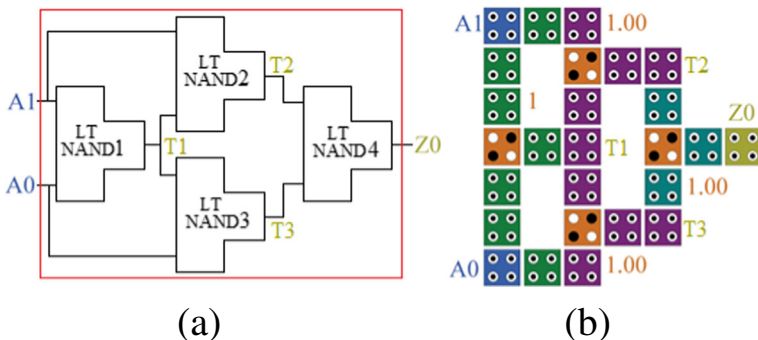


Fig. 3 a: Block diagram and b: QCA Layout of Two-input LTeX Module [38]

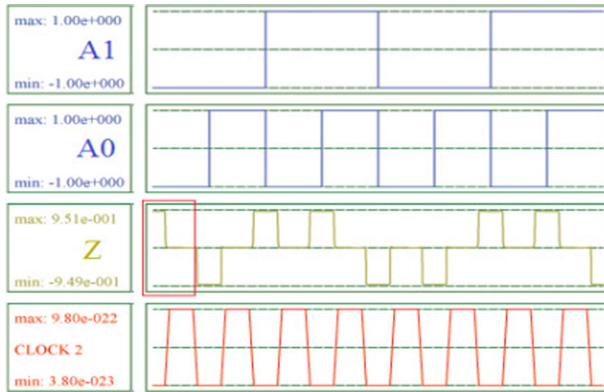


Fig. 4 Output of two-input LTeX Module

correct operation of LTeX module will cause missing, displaced, extra cell and/or electrons in the layout of Fig. 3b. There are four types of defects [39, 40] that may occur during the QCA manufacturing process as follows (a) Cell Displacement, (b) Cell Misalignment, (c) Cell Omission and (d) Cell Rotation. These defects are introduced forcefully within the layout of two-input LTeX module as mentioned in Fig. 5a and b.

(a) Cell Displacement: The shifted cells from their original positions cause Cell Displacement defects. As each of the cells of two-input LTeX module may cause the cell displacement defects, so the proposed 7X7 LTeX layout is numbered against all the cells as given in Fig. 5a and b.

Keeping the horizontal and vertical distance between the cells as d nm in mind, the effects of upward/downward and left wise/right wise cell displacements on output cell Z are summarized in Table 1. The minimal cell displacement of 0.6 nm for the cell positions {10, 22, 26, 38} towards right direction changes the output polarization instantaneously. These cells are “defect-immune” to the left displacement of more than 65 nm and vertical movements of 34.5 nm to 52 nm as reported in Table 1. The

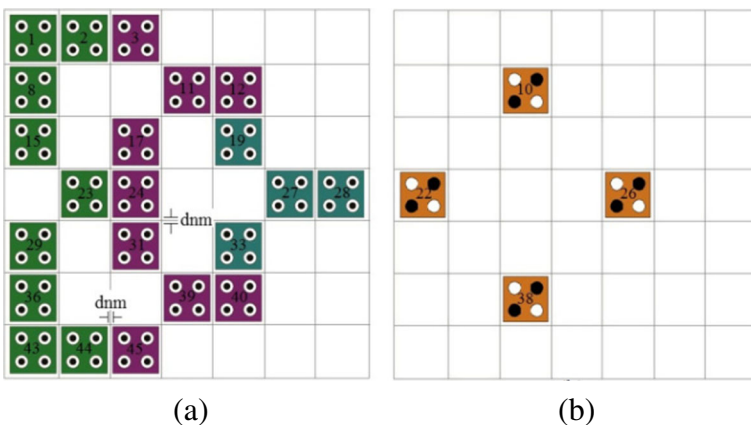


Fig. 5 Grid-View of the Proposed 2-input LTeX Module: **a** Main Cell Layer, **b** Additional Cell Layer placed 34.5 nm above the main cell layer

Table 1 Effects of cell displacement and cell rotation on the layout of Fig. 5

Cell @Position	Displacement d up to	Effect of Cell Rotation (O/P affected?)	Cell @Position	Displacement of the distance d up to	Effect of Cell Rotation (O/P affected?)	Cell @Position	Displacement d up to	Effect of Cell Rotation (O/P affected?)
1(input A)	Left: 5.7nm Upward:3.5nm	Y*	10	Right: 0.6nm Left: > 65nm Vertical:34.5 nm to 52nm	N	17	Up: 9.5nm Right:5.6nm Left:1.3nm Right:6.6nm	Y
2	Up:3.6nm Down:2.8nm	Y	11	Up: 4.5nm Down: 4.4nm	Y	19	Left: 2.9nm Right: 0.6nm	N
3	Up: 0.8nm Right: =4.8nm	N	12	Right:5nm Up: 3.8nm	N	22	Right: >65nm Vertical:34.5 nm to 52nm	N
8	Right: 4.2nm Left : 6.1nm	N	15	Right:8nm Left:5.3nm	N	23	Up:2.7nm Down:2.7nm Left:0.3nm Up:3.8nm	Y
24	Right: 0.3nm	N	26	Right: 0.6nm Left: > 65nm Vertical:34.5 nm to 52nm	N	27	Down:3.8nm Left:2.2nm	N
28 (Output)	Right:2.2nm Up:4.1nm Down:4.1nm	Y*	33	Up:9.9nm Left:2.6nm Right: 6nm	N	39	Up:4.9nm Down:5.1nm Left:8nm Right:5nm	Y
29	Up:3.8nm Left:5.1nm Right:8nm	N	36	Right: 4.2nm Left:6nm	N	40	Down:3.8nm	N
31	Left:0.7nm Right:5.4nm Down:8.3nm	N	38	Right: 0.6nm Left: > 65nm Vertical:34.5 nm to 52nm	N	43 (input B)	Left:5.7nm Down:3.5nm	Y*
44	Up:3.6nm Down:2.8nm	Y	45	Right:0.8nm Down:4.8nm	N	-	-	-

* As the Cell Rotation errors at input and output cells are quite obvious, so defect performance exclude Cell {1, 28, 43}

manufacturer should pay the highest attention during the synthesis phase of the cell positions {23, 24, 27, 28, 44, 45} because any displacements of less than 5 nm in either directions at these positions will lead the output Z to cause severe deviation from its originality. The displacement defects at the cell positions {1-3, 8, 11-12, 17, 19, 29, 31, 33 and 43} report that they are highly noise prone in any one of the four directions. As the multidirectional defects of the singular and multiple cell positions are complex in nature, this work considers only horizontal, vertical displacements between the layers as well.

- (b) **Cell Rotation:** When a cell within the layout is rotated by an angle θ , this type of error occurs. The Table 1 summarizes the effects of cell rotations on the output polarizations. It can be noted that the rotational effects at the positions {10, 22, 26, 38} (i.e. cells on the upper layer) does not affect the operation of LTeX module and hence the output polarizations are free from deviations. The cell-rotation defects on the main layer cells affect the output and as a consequence invalid waveform or sometimes clipped waveform at the output may obtain.
- (c) **Cell Omission/Missing:** When a specific cell(s) remains un-deposited, missing cell defect occurs. Table 2 shows the missing cell deposition defect in two-input LTeX module. It is seen that the cell numbered {12, 19, 24, 27, 28, 33, 43} produce undesired output under single cell omission whereas the cell missing at the positions {10, 22, 26, 38} will cause no effect on output. The double cell missing and triple cell missing defects are frequently observed in tiled structure in QCA [41]. As a result such type of errors is not subjected to happen in two-input LTeX module.
- (d) **Additional Cell Deposition:** When the extra cell(s) are mistakenly deposited on the layout of LTeX module, additional cell deposition error would occur. Some of the configurations with additional cell deposition defects which the proposed LTeX module can tolerate are reported in Fig. 6a–c. The additional cells at the cell positions {9, 16}, {30, 37} and {18, 25, 32} of the Fig. 5 change the functionality of the two-input LTeX module and results the wrong output.

The worthwhile point during the QCA implementation of multilevel digital circuits is the effects of Radius of Effect (RoE) and layer separation on the output polarization. The variations of RoE (from 20 nm to 100 nm) and of the layer separations (from 12 nm to 30 nm)

Table 2 Effect of missing cell on the layout of Fig. 5

Cell Missing @position	Output Effected (Y/N)	Cell Missing @position	Output Effected (Y/N)	Cell Missing @position	Output Effected (Y/N)	Cell Missing @position	Output Effected (Y/N)
1	Y*	15	N	27	N	39	Y
2	N	17	Y	28	X*	40	N
3	N	19	N	29	Y	43	X*
8	N	22	Y	31	N	44	Y
10	N	23	Y	33	N	45	N
11	Y	24	X	36	N	–	–
12	X	26	Y	38	N	–	–

* As the Cell Rotation errors at input and output cells are quite obvious, so defect performance exclude Cell {1, 28, 43}, X= No output

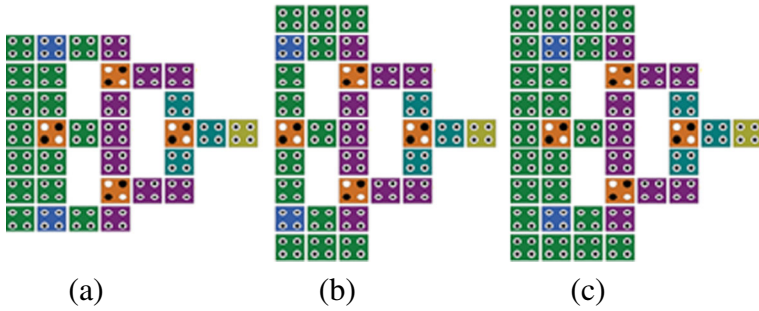


Fig. 6 Different Configurations of defect-free 2-input LTeX Module

with the maximum and minimum polarization are demonstrated in Fig. 7a–b respectively. Moreover the variations of output polarizations with some significant dimensions of the cell size of LTeX module at a specific RoE of 65 nm and 80 nm are summarized in Table 3. The table also shows the statistics of nanometer level variations of the layer separation with the output polarizations of the LTeX module.

4 Novel Formulations for QCA Implementations of n-bit Binary to Gray (B2G) and Gray to Binary (G2B) Converters

The two-input LTeX module is further extended in the design of n-input (generic) B2G and G2B Converter designs. These are extensively used in the Gray Code Addressing [32, 33, 42]. The QCA-based technical literature reveals the binary encoded memory designs several times [4–7]. Still the QCA implementation of Gray Code addressing remains unexplored. This work introduces the novel formulations and also implements the QCA design methodologies in the Gray Code addressing. In a uniprocessor based memory architecture design, the memory address of the next instruction is stored in the Program Counter. Each time after the execution of the present memory address, the program counter is increased by one unit to point out correctly the next instruction in the queue. The fetching of branch instruction

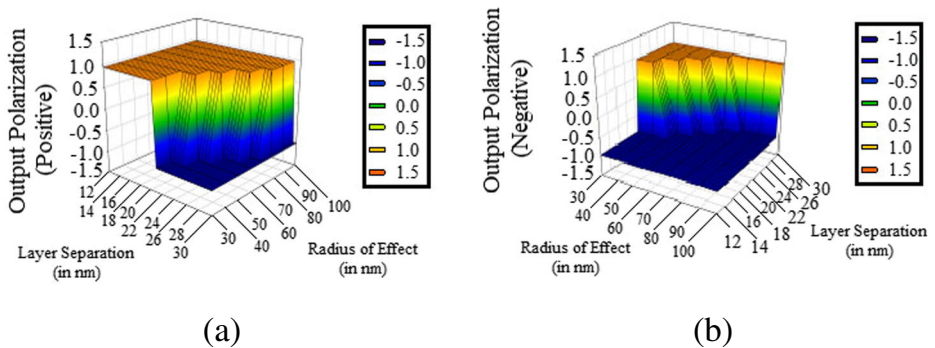


Fig. 7 a: Variations of Output Polarization (positive) in terms of Layer Separation (12 nm to 34.5 nm) and Radius of Effect (30nm to 100nm), b: Variations of Output Polarizations (negative) in terms of Layer Separation (12 nm to 34.5 nm) and Radius of Effect (30 nm to 100 nm)

Table 3 Polarizations of two-input LTeX Module

Design	Cell Size in nm X nm	RoE (nm) Separation In nm	Layer	Polarization
LTeX Block	18X18	80	12	0.954/-0.948
	22X22	80	14	0.954/-0.949
	26X26	80	16	0.953/-0.949
	30X30	80	18	0.953/-0.95
	34X34	80	20	0.953/-0.95
	38X38	80	22	0.952/-0.95
	42X42	80	34.5	0.952/-0.951
LTeX Block	18X18	65	12	0.954/-0.948
	22X22	65	14	0.954/-0.949
	26X26	65	16	0.953/-0.949
	30X30	65	18	0.953/-0.950
	34X34	65	20	0.953/-0.950
	38X38	65	22	0.952/-0.950
	42X42	65	34.5	0.952/-0.951

pushes the content of the program counter to the stack pointer and the program counter gets updated about the branch address [43, 44]. In the Gray Code Addressing system, a “Gray Code incrementer” is required to change the index of program counter to manage the offset address as shown in Fig. 8 below.

The 8-bit binary address is firstly converted to 16 bit Gray Code equivalent by the B2G Converter. The content of the binary encoded Program Counter is converted by another B2G Converter; the output from the later one is then fed to the Gray Incrementer block. The Gray Incrementer increments the 16 bit Gray Address using an index *i* that includes word-size of the processor. For example, the 8-bit addressable machine requires Gray Address index as 1, the 16-bit addressable machine needs the index *i* with increment of 2, the 32-bit addressable machine needs the index with the increment of 3 and so on. For an *n*-bit addressable machine, the incremental index *i* becomes 2^{n-1} . The subsequent subsections implements B2G and G2B Converters with and without increments by using the LTeX module.

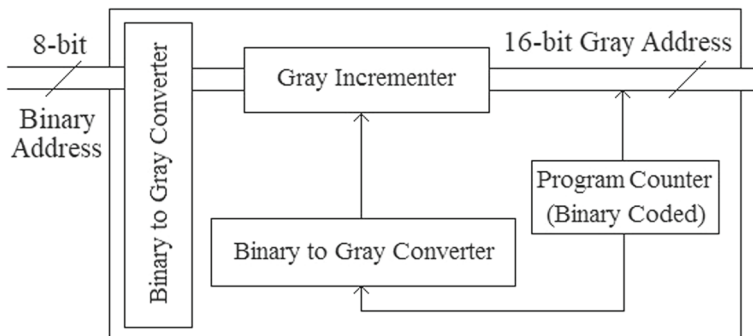


Fig. 8 Significance of B2G and G2B Converters in Processor based designs

The *formulations 1, 2* and subsequent *corollaries* are enunciated that significantly improves the QCA based designs of B2G and G2B Converters. These can improve the QCA implementations of the converter layouts in terms of O-Cost, Effective area in nm², Delay and Cost_α [38]. The appendixes at the end retrospect the definitions of these parameters and present the proof of the formulations and corollaries.

The Formulation 1 and 2 can be exploited by considering the Binary and Gray operands, B[n-1:0] and G[n-1:0] respectively. Here n is the number of bits in Binary and Gray codes. Here the Binary and Gray operands are implicitly indicated as the addresses involved in Gray Code Addressing scheme.

Formulation 1 *The n-bit Binary Code/Address is divided into left and right parts specified as B[n-1:k] and B[k-1:0] respectively. The expressions of the B2G Converter using two-input LTeX module for different increments i (= 2ⁿ⁻¹) and k (= n - 1) can be formulated as the (5):*

(a) $G1[n-1:k]=B2G1[B(n-1:k)]:G[n-1]=B[n-1],G[n-2]=LTeX[B[n-1],B[n-2]]...up$ to $G[k]=LTeX[B[1],B[k]]$ for increment $i=1, k=0,$	to
(b) $G2[n-1:k]=B2G1[B[n-1:k]]:G[n-1]=B[n-1],G[n-2]=LTeX[B[n-1],B[n-2]]...up$ to $G[k]=LTeX[B[2],B[k]]$ and $G2[k-1:0]=B2Gr[B[k-1:0]]:G[k-1]=B[k-1]$ for increment $i=2, k=1,$	to
(c) $G4[n-1:k]=B2G1[B[n-1:k]]:G[n-1]=B[n-1],G[n-2]=LTeX[B[n-1],B[n-2]]...up$ to $G[2]=LTeX[B[3],B[2]]$ and $G4[1:0]=B2Gr[B[1:0]]: G[1]=B[1], G[0]=LTeX[B[1],B[0]]$ for increment $i=4, k=2,$	to
...	
(d) $G2^{n-1}[n-1:n-1]=B2G1[B[n-1:n-1]]: G[n-1]=B[n-1]$ and $G2^{n-1}[n-2:0]=B2Gr[B[n-2:0]]:G[n-2]=B[n-2],$ $G[n-3]=LTeX[B[n-2], B[n-3]]...up$ to $G[0]=LTeX[B[1],B[0]]$ for increment $i = 2^{n-1}$ and $k = n-1$... (5)

Corollary 1 *The number of two-input LTeX modules required for the QCA implementations of n-bit Binary to Gray Converter with increment i=1, k=0 is (n-1) and with increment i>1, k≠0 is (n-2).*

Formulation 2 *The n-bit Gray Code/Address is divided into left and right parts specified as G[n-1:k] and G[k-1:0] respectively. The expressions of the Gray to Binary Converter using two input LTeX module for different increments i (=2ⁿ⁻¹) and k (=n-1) can be formulated as the (6):*

(a) $B1[n-1:0]=G2B1[G[n-1:0]]:B[n-1]=G[n-1],B[n-2]=LTeX[B[n-1],G[n-2]],B[n-3]$ $=LTeX[B[2],G[1]]...up$ to $B(0)=LTeX(B(1),G(0))$ for increment $i=1, k=0,$	
(b) $B2[n-1:1]=G2B1[G2[n-1:1]]:B[n-1]=G[n-1],B[n-2]=LTeX[G[n-1],G[n-2]]...up$ to $B[1]=LTeX[B[2],G[1]]$ and $B4[0:0]=G2Br[G2[0:0]]: B[0]=G[0]$ for increment $i=2, k=1,$	to
(c) $B4[3:2]=G2B1[G4[3:2]]:B[3]=G[3],B[2]=LTeX[G[3],G[2]]$ and $B4[2:0]=G2Br[G4[1:0]]:$ $B[1]=G[1], B[0]=LTeX[B[1],G[0]]$ for increment $i=4, k=2,$	
...	
(d) $B2^{n-1}[n-1:k]=G2B1[G[n-1:k]]: B[n-1]=G[n-1]$ and $B2^{n-1}[k-1:0]=G2Br[G2B[k-1:0]]: B[n-2]=G[n-2],$ $B[n-3]=LTeX[B[n-2],G[n-3]]... up$ to $B[1]=LTeX[B[2],G[1]],B[0]=LTeX[B[1],G[0]]$ for the increment $i=2^{n-1},$ and $k=(n-1)..$... (6)

Corollary 2 *The number of two-input LTeX modules required for the QCA implementations of n-bit Gray to Binary Converter with increment i=1, k=0 is: (n-1), with increment i>1, k≠0 is(n-2).*

These *formulations* and *corollaries* constitute the LTeX methodology that helps in the converter designs described in next sections.

5 Designing Binary to Gray and Gray to Binary Converters Exploiting new Formulations

5.1 4-bit Binary to Gray Converter Design (n=4)

i=1, k=0: The 4-bit B2G Converter is exploiting the *formulation1*, are demonstrated in Fig. 9a–d. The binary address B[3]B[2]B[1]B[0] is keen to produce Gray equivalent which can be further processed for the next level of intermediary circuits of Fig. 8. According to *formulation1* and *corollary1*, the binary address B[3]B[2]B[1]B[0] is fetched by the (4-1)=3 two-input LTeX modules resulting the expressions as $G1[3:0]=B2G1[B[3:0]]$: $G[3]=B[3]$, $G[2]=LTeX[B[3],B[2]]$, $G[1]=LTeX[B[2],B[1]]$, $G[0]=LTeX[B[1],B[0]]$. The generated layout which implements the above expressions is given in Fig. 9a. The higher the cascaded QCA Gates in computational path, the higher will be the delay [38]. The layout for 4-bit converter, as in Fig. 9a, employs three LTeX modules in parallel connections instead of cascaded connections. Hence the delay for the circuit becomes 0.5.

i=2, k=1: As the incremental index *i* is not equal to 1 for higher byte addressable machines, so it is recommended to utilize the modified designs of 4-bit B2G Converters by exploiting the *formulation1* and *corollary1*. For this case, the binary address B[3]B[2]B[1]B[0] is divided into left part and right part as B[3]B[2]B[1] and B[0] respectively. The proposed *formulation1* utilizes the expressions $G1[3:0]=B2G1[B[3:0]]$: $G[3]=B[3]$, $G[2]=LTeX[B[3],B[2]]$, $G[1]=LTeX[B[2],B[1]]$ and $G1[0:0]=B2Gr[B[0:0]]$: $G[0]=B[0]$. The B2G Converter for *i*=2, *k*=1 is given in Fig. 9b.

i=4, k=2 and i=8, k=3: The 4-bit converter allows two more designs with the incremental index *i*=4 (*k*=2) and *i*=8 (*k*=3). Rendering the *formulation1*, the binary address B[3]B[2]B[1]B[0] has been divided into sets of [B[3]B[2]], [B[1]B[0]] and [B[3]], [B[2]B[1]B[0]]. For *i*=4, the Binary to Gray Converter equations become $G[3]=B[3]$,

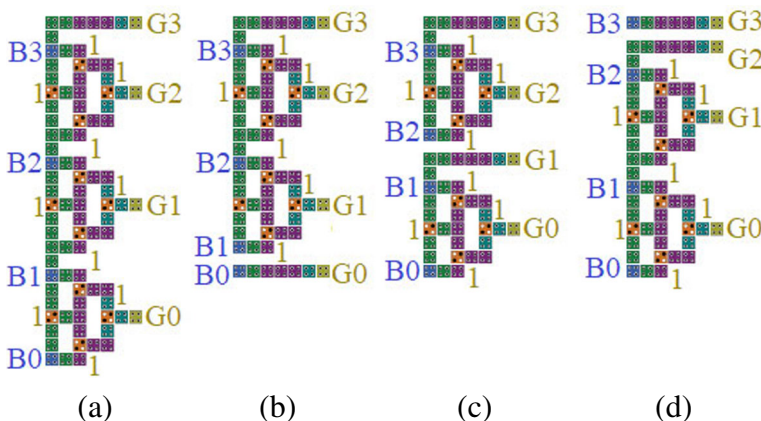
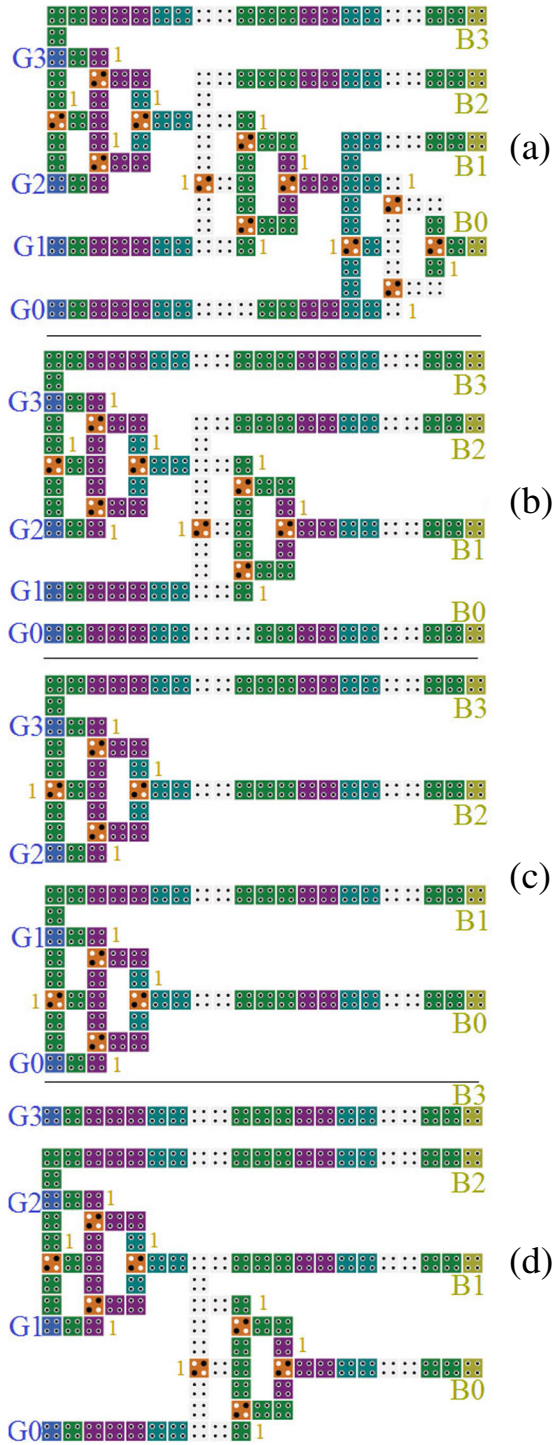


Fig. 9 The 4-bit B2G Converters for **a** *i*=1, *k*=0, **b** *i*=2, *k*=1, **c** *i*=4, *k*=2 and **d** *i*=8, *k*=3

Fig. 10 The 4-bit G2B Converters for **a** $i=1, k=0$, **b** $i=2, k=1$, **c** $i=4, k=2$ and **d** $i=8, k=3$



$G[2]=LTeX[B[3],B[2]]$ and $G[1]=B[1],G[0]=LTeX[B[1],B[0]]$. Similarly as for $i=8$, the expressions evaluate $G[3]=B[3],G[2]=LTeX[B[3],B[2]],G[1]=LTeX[B[2],B[1]]$ and $G[0]=B[0]$. As demonstrated in Fig. 9c–d, so $(4-2) = 2$ numbers of two-input LTeX modules are needed for both the cases.

The B2G layouts of Fig. 9a–d are generated with the cell size $18\text{ nm} * 18\text{ nm}$, layer separation 34.5 nm and examined with RoEs $65\text{ nm}, 80\text{ nm}$ as mentioned in Table 3, Fig. 7a–b.

5.2 4-bit Gray to Binary Converter Design (n=4)

i=1, k=0: The QCA implementations of 4-bit G2B converter for $i=1, k=0$ are discussed in this sub-section. The proposed converter of Fig. 10a with $i=1, k=0$ conforms the output of conventional 4-bit G2B Converters designs [10, 12, 14]. The Gray Address $G[3]G[2]G[1]G[0]$ is given to the converter and processed by using the expressions of $B[1[n-1:0]]=G2BI[G[n-1:0]]:B[3]=G[3],B[2]=LTeX[B[3],G[2]], B[1]=LTeX[B[2],G[1]],B[0]=LTeX[B[1],G[0]]$ and finally produces the output as shown in Fig. 10a.

i=2, k=1: The 4-bit G2B Converter is used in 16-bit word size processors, to convert Gray Address $G[3]G[2]G[1]G[0]$ to its equivalent Binary address. The Binary equivalent is evaluated by the expressions $B[2[n-1:0]]=G2BI[G[n-1:0]]:B[3]=G[3],B[2]=LTeX[B[3],G[2]],B[1]=LTeX[B[2],G[1]],B[0]=G[0]$. The QCA layout of the converters is shown in Fig. 10b.

i=4, k=2 and i=8, k=3: The 4-bit G2B Converters which have been represented in Fig. 10c and d are suitable for 32-bit, 64-bit word size respectively with the incremental indexes $i=4, 8$. The Gray Address $G[3]G[2]G[1]G[0]$ is divided into sets $[G[3]G[2]], [G[1]G[0]]$ and $[G[3]], [G[2]G[1]G[0]]$ by following the application of *formulation 2*. The QCA layout of concerned converter is shown in Fig. 11c. For $i=4$, the G2B Converter equations are $B[4[n-1:0]]=G2BI[G[n-1:k]]:B[3]=G[3], B[2]=LTeX[B[3],G[2]]$ and $B[4[k-1:0]]=G2Br[G[k-1:0]]: B[1]=G[1],B[0]=LTeX[B[1],G[0]]$.

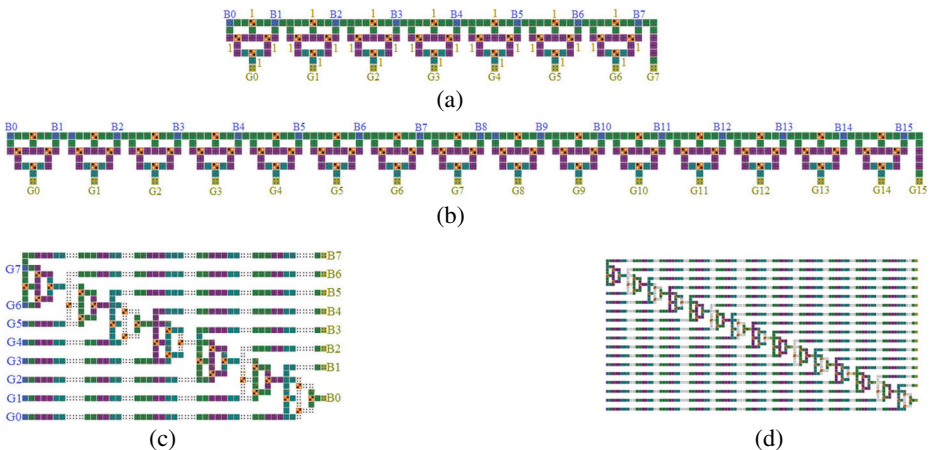


Fig. 11 QCA Layouts of **a** 8-bit, **b** 16-bit B2G Converters and **c** 8-bit, **d** 16-bit G2B Converters (with $i=1$)

Table 4 Design summary of 4-bit B2G converter with existing designs [11–18]

SI No	4-bit B2G Converter Designs Proposed	O-Cost	Effective Area in nm ²	Cost _α	Gate Count	Types of Wire Crossing
1	In [17]	131	166344	65.25	MV:9	NA
2	In [15]	109	98604	69.75	MV:10	Multilayer
3	In [14]	192	269724	273	MV:12	NA
4	In [11]	389	>126000	87	MV:9	Coplanar
5	In [18]*	92	81844	NA	NA	NA
6	In [13]	137	120684	43.5	MV:9	NA
7	In [16]	127	151844	72	MV:9	Multilayer
8	In [12]	133	161656	63.75	MV:9	Multilayer
9	This work	88	68724	32.25	LT:6	Multilayer

* The tiled structure is not considered for Cost_α analysis

Similarly the G2B Converter for i=8, k=3 which is shown in Fig. 10d uses *formulation 2* to generate $B4[n-1:k]=G2B1[G[n-1:k]]:B[3]=G[3]$ and $B4[k-1:0]=G2Br[G[k-1:0]]:B[2]=G[2], B[1]=LTeX[B[2],G[1]], B[0]=LTeX[B[1],G[0]]$. It's worth to note the pre-implementation fact of 4-bit G2B Converter that the number of LTeX modules required to implement 4-bit G2B Converter is $(4-1)=3$ for i=1, k=0 where the number becomes $(4-2)=2$ for i>1 (i.e. for i=2,4,8). Hence the *corollary2* is justified.

The post-implementations of the 4-bit Converters have been summarized in Tables 4 and 5. Various QCA design metrics like O-Cost, Effective Area in nm², Cost_α and number of Gate counts [38] have been calculated and compared with previously existing designs [11–18]. It is important to note that the Tables 4 and 5 consider the 4-bit B2G Converter and G2B Converter layouts for i=1, k=0 respectively. As the previous methodologies does not consider the Gray Code addressing purpose, so the statistical analysis should be done carefully to avoid the confusion regarding the incremental index i in converter designs.

5.2.1 Scalability of the Converter Designs in High Fan-in Designs

For increment index i=1: To check reproducibility, redesign ability and scalability of the proposed two-input LTeX module, the designs and verifications of high fan-in Gray Code Converters are highly required. Apart from 4-bit designs, the designs of 8-bit, 16-bit, 32-bit and 64-bit B2G and G2B Converters are implemented keeping the proposed *formulations* in mind. This sub-section reports the designs of 8-bit and 16-bit B2G Converters and G2B Converters in Fig. 11a–d.

Table 5 Design summary of 4-bit G2B converter with existing designs [10, 14]

SI No	4-bit G2B Converter Designs Proposed	O-Cost	Effective Area in nm ²	Cost _α	Gate Count	Types of Wire Crossing
1	In [10]	276	339096	–	MV:9	Coplanar
2	In [14]	269	690000	468	MV:12	NA
3	This work	144	144092	96.75	LT:6	Multilayer

The 8-bit and 16-bit B2G Converters receive the binary address to generate the equivalent Gray Address after the negative edge of the clock cycle 0.75. The LTeX methodology employs a novel B2G converter design paradigm that needs 0.75 clock cycles irrespective of the number of the bits present in binary address. The 8, 16-bit converters of Fig. 11a and b need $(8-1)=7$ and $(16-1)=15$ numbers of two-input LTeX modules. It is also evident from the Fig. 11c and d that 8-bit and 16-bit G2B converters require $(8-1)=7$ and $(16-1)=15$ numbers of two-input LTeX modules. The Ahmad Converter [15] has given the primary guidelines to design n-bit G2B Converter so far. The post-implementation design summary of the converters (with $n=8, 16, 32, 64$ and $i=1$) has been demonstrated in Table 6 which highlights the statistics of existing n-bit B2G converter [15] and compares it with LTeX counterparts.

The design criteria in this work for n-bit Gray Converter circuit consider proper formulation of O-Cost, Effective Area in nm^2 , Delay and $Cost_{\alpha}$. The efficient wire connections have been used with the two-input LTeX modules to confirm the optimal design of converter circuits. Table 7 formulates the Effective Area and O-Cost as $\{(n-1)*0.022080+0.0248\}$ and $(27*n-20)$ for n-bit QCA implementation of B2G Converter iff LTeX formulations are taken into considerations. For example, the 128-bit LTeX B2G Converter would require $\{(128-1)* 0.022080+0.0248\} nm^2 = 2.828 \mu m^2$ and $(27*128-20)= 3436$ QCA cells with $Cost_{\alpha} =49344.75$. Apart from the formulations of QCA design metrics, the main achievement is to generate QCA converters with delay independent of n. The delay for the B2G Converter becomes 0.75 irrespective of its size. Similarly the LTeX G2B Converters can be designed by taking the statistics of the Table 7 in to considerations. Unlike the B2G Converter design, the delay of the G2B converter design is dependent on n as $0.75*(n-1)$ as specified Table 7.

For increment index $i>1$ ($k>0$): The proposed *formulations* find its usefulness in the designs of Gray Converter designs for the value of the incremental index i more than 1. If 32-bit machine is concerned, then byte increment becomes 4. Hence incremental index i becomes 4. This work extends its methodology to implement converter design meant for machine with $i=2, 4, 8...$ up to 2^{n-1} . Figure 12a introduces the 8-bit B2G Converter design with $i=8, k=3$ as an instance.

From the *formulation1*, the equations can be inferred that $G4[7:3]=B2GI[B[7:3]]$: $G[7]=B[7], G[6]=LTeX[B[7],B[6]], G(5)=LTeX[B[6],B[5]], G[4]=LTeX[B[5],B[4]], G[3]=$

Table 6 Comparison of n-bit B2G converter [15] with n-bit LTeX B2G converter

n-bit B2G Converter Structures	n	O-Cost	Improvement	Delay	Improvement	$Cost_{\alpha}$	Improvement
In [15]	8	233	–	1.5	–	372.75	–
	16	489		3		1698.75	
	32	1001		6		7230.75	
	64	2050		12		29814.75	
This work	8	196	15.88%	0.75	50%	204.75	45.08%
	16	411	15.96%	0.75	75%	792.75	53.33%
	32	844	15.7%	0.75	87.5%	3120.75	56.84%
	64	1708	16.68%	0.75	93.75%	12384.75	58.46%

Table 7 Post implementation results of n-bit B2G and G2B converters designs

B2G Code Converter				G2B Code Converter					
Structures	Area in μm^2	O-Cost	Delay	Cost $_{\alpha}$	Structures	Area in μm^2	O-Cost	Delay	Cost $_{\alpha}$
8-Bit	0.157044	196	0.75	204.75	8-Bit	0.551450	532	5.25	1433.25
16-Bit	0.526784	411	0.75	792.75	16-Bit	2.240731	1980	11.25	11891.25
32-Bit	6.86964	844	0.75	3120.75	32-Bit	9.2285	7564	23.25	96743.25
64-Bit	13.93524	1708	0.75	12384.75	64-Bit	35.544	29484	47.25	780239.25
n-Bit (i=1,k=0)	$(n-1)*0.022080+0.0248$	27n-20	0.75	$(4n^2+2n+1)*0.75$	n-Bit (i=1,k=0)	NA **	$7n^2+13n-20$	0.75*(n-1)	$(4n^3-2n^2-n-1)*0.75$
n-Bit (i>1,k≠0)	$(n-2)*0.021804$ $+(n-1)*0.02484+0.0276*n$	27n-40	0.75	$(4n^2-6n+3)*0.75$	n-Bit (i>1,k≠0)	NA **	$7n^2+13n-46$	0.75*(n-1)	$(4n^3-10n^2-9n-3)*0.75$

**As the grid matrix for G2B Converter changes with input bit n, so this work does not include the formulation of effective area for generic G2B Converters

$LTeX[B[4],B[3]]$ and $G4[2:0]=B2Gr[B[2:0]]:G[2]=B[2],G[1]=LTeX[B[2],B[1]], G[0]=LTeX[B[1],B[0]]$ for increment $i=8, k=3$. Similar exploitation can be done for 16-bit G2B Converter design with $i=16, k=4$. The equations for the design refers the *formulation2* and as a result becomes $B16[15:4]=G2B1[G16[15:4]]:B[15]=G[15], B[14]=LTeX[B[15],G[14]],B[13]=LTeX[B[14],G[13]],B[12]=LTeX[B[13],G[12]], \dots B[4]=LTeX[B[5],G[4]]$ and $B16[3:0]=G2Br[G16[3:0]]: B[3]=G[3],B[2]=LTeX[B[3],G[2]], B[1]=LTeX[B[2],G[1]],B[0]=LTeX[B[1],G[0]]$ for increment $i=16, k=4$. The QCA Layout of the G2B converter is shown in Fig. 12b.

6 Result Analysis

Features of Layouts This work introduces the elemental two-input LTeX module which can be further extended in the designs of generic B2G Converter and G2B Converter, suitable for Gray Addressing schemes. It is worth pointing out that the layouts of Figs. 3a, 9a–d, 10a–d, 11a–d, 12a–b which are presented in this work have the following features:

- (a) The inputs and outputs are placed at the border of the circuits to avoid additional interconnecting wires during the signal flow through the different levels [45]. As no interconnecting wires are needed to connect fixed polarization cells, so the constants are placed abruptly in the QCA layouts,
- (b) To ensure the proper output, there are minimum two cells which are clocked together. Moreover, the long QCA wires are divided into different clocking zones to ensure the process of robust communications [45, 46],
- (c) The use of QCA cells with $+1/-1$ orientation makes the layouts more stable [26],
- (d) The outputs of B2G and G2B Converters have been generated at the negative edge of the same clocking zone. To avoid the “race around data” hazard in multilevel QCA layouts, it is very much essential to have all the outputs at the same clocking pulse.

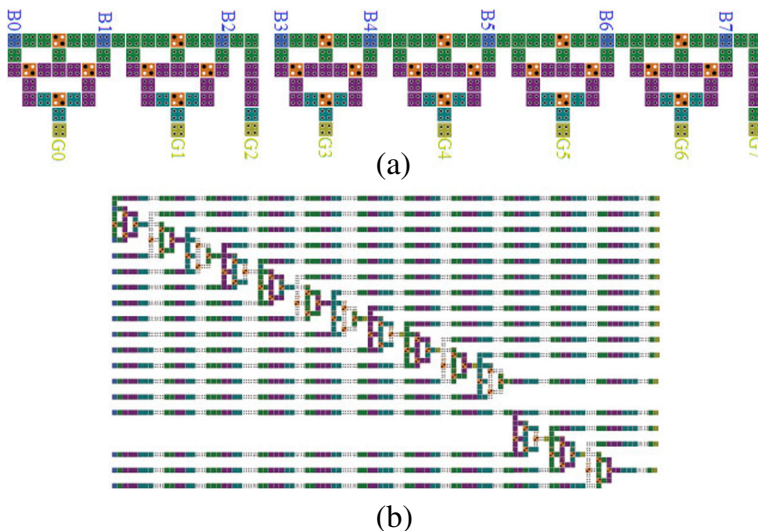


Fig. 12 QCA Layouts of **a** 8-bit B2G Converters with $i=8, k=3$, **b** 16-bit G2B Converters with $i=16, k=4$

The proposed layouts of this work only use a single layer that can be fabricated by biplanar alternative cells [47]. Although three dimensional structures becomes complex during fabrication, it is important to note that it can be done since this is not true three-dimensional structure. The rotated cell using two-dimensional electron gases can implement the upper layer cells of Fig. 3b. Moreover, in terms of QCA design metrics the biplanar approach of the proposed layouts makes the methodology effective as follows.

LTeX Module and its Defect Tolerant Analysis According to the work-flow presented in the Section 1, this work firstly discusses novel two-input LTeX module as demonstrated in Fig. 3a. Then the defect tolerant analysis of the two-input LTeX module is performed to check the endurance and the degree of vulnerability for different defects of QCA such as Cell Displacement, Cell Rotation, Cell Omission and Additional Cell Deposition. Special caution has to be taken during the optical lithographic etching and synthesis phase of all coplanar cells as mentioned in Fig. 5a. The utmost attention should be given to the cells from upper layer at the positions {10, 22, 26, 38} to prevent the right-side cell displacement error. Otherwise the upper layer cells are appeared to be higher noise immune cells as summarized in Table 1. The Cell Rotation defect of all the coplanar cells of Fig. 5a produces either erroneous output or no output whereas the rotational defect at upper layer cells has shown no effect on output as shown in Table 1. In Table 1, 17 out of 23 cells are fault tolerant it means fault tolerance of Cell Rotation up to 73.91% is achieved. The Missing Cells of the positions at {2, 3, 8, 10, 15, 19, 27, 31, 33, 36, 38, 40 and 45} from the entire layout cause no effect on the output. The fault tolerant of Missing Cell error of LTeX module becomes 56.52% as reported in Table 2. Various layouts with additional cells have been examined, out of which the layouts of Fig. 6a–c resulted unaffected output.

The variations of output polarizations in terms of RoE and layer separation yielded interesting results to show. From the Fig. 7a and b it can be shown that if the layer separation is varied from 12 nm to 34.5 nm at the higher values of RoE, both the positive and negative output polarizations remain unaffected. Similarly the lower value of layer separation has left errors at output polarizations for lower RoE values. It implies that in terms of output polarization the layer separation and RoE are inversely related to each other.

Another experimental analysis has been done in Table 3 to show the effects of change of cell size on output polarizations. It can be observed from Table 3 that the output polarizations have no effect if the cell size of LTeX module is extensively varied between (18 nm * 18 nm) to (42 nm * 42 nm) at the fixed values of RoE and layer separation. Based on the analysis and observations, the B2G and G2B Converters of this work are carried out with the parameters as mentioned in Table 8.

Code Converter Realizations The existing B2G and G2B Converters [10–19] are not intended for the Gray Code Addressing scheme. Two novel *formulations* and *corollaries* have been introduced in the Section 4 which implements n-bit B2G and G2B Converters anticipated for the 2ⁿ-bit Gray Code Addressable architectures.

As the requirement of such converters are essential for Gray Code addressing, so the binary/gray addresses are treated as literal inputs to the converters that generate gray/binary addresses. The n-bit binary/gray addresses are divided into two operands B[n]B[n-1]B[n-2]...B[k]/G[n]G[n-1]G[n-2]...G[k] and B[k-1]B[k-2]...B[0]/G[k-1]G[k-2]...G[0]. The (5) and (6) are proposed accordingly to produce gray/binary equivalents by using LTeX methodology.

The **4-bit B2G Converter** designs are shown in Fig. 9a–d. Figure 9a reports the design that takes four inputs B[3]B[2]B[1]B[0], consumes 68724 nm² effective area, O-Cost 88 and

Table 8 Design parameters

Parameters	Coherence Vector
Cell Size	18 nm * 18 nm
Layer Separation	34.5 nm
Relative Permittivity	12.9
Number of Samples	50000
Radius of Effect (RoE)	80 nm
Total Simulation Time	7e-011 Second
Clock Amplitude factor	2
Dot Diameter	5 nm
Inter Cell Distance	2 nm

produces the output $G[3]G[2]G[1]G[0]$. For an 8-bit addressable machine, the index $i=1$ and $k=0$ confirms the conventional 4-bit B2G Converter outputs. The layout of Fig. 9b has been obtained after applying the *formulation 1* to the binary address $B[3]B[2]B[1]B[0]$. As it has been meant for 16-bit addressable machine, so the value of i becomes 2 and k equals 1. The 7X19 grid layout consumes 76570 nm^2 and O-Cost of 68. The layouts of Fig. 9c and d have been designed for 32-bit, 64-bit addressable machines. Both of these layouts show 76570 nm^2 effective area and O-Cost of 68. The post-implementation result of 4-bit B2G Converter has been reported in Table 4. The converters which can process 16-bit, 32-bit, 64-bit ...up to 2^{n-1} bit addressable machines have not been reported so far, that's why this work individually compares the proposed 4-bit QCA layouts of Fig. 9a with the previous designs in terms of QCA metrics as mentioned in Table 4. This table parameterized Cost_α [38, 48] along with the other design metrics such as O-Cost [38], effective area in nm^2 and number of gate counts in the layout. It can be observed that the Cost of Crossing C becomes 1 for proposed LTeX designs because of the requirement of one layer in the layouts. The proposed 4-bit B2G Converter needs $\sim 4.35\%$ less O-Cost, 16.04% less effective area, as compared to the best reported design of Karkaj Converter [18]. The proposed converter shows 26.863% less Cost_α compared to Ahmad Converter [13] and 33.33% less number of gates as compared to Rao Converter [16].

The **4-bit G2B Converter** designs are instantiated by applying the *formulation 2* to the operand $G[3]G[2]G[1]G[0]$. The conventional 4-bit Converter (with increment index $i=1$) of Fig. 10a consumes 21X15 grid and results the effective area of 144092 nm^2 and O-Cost of 144. The test vectors $G[3]G[2]G[1]G[0]$ are settled as Gray input to the converter that produces binary equivalent $B[3]B[2]B[1]B[0]$ at the negative edge of third clock 0 resulting the delay of 2.25. As the layout of Fig. 10a is identical with the conventional designs, so the proposed LTeX converter is compared with the existing designs [10, 14] and summarized in Table 5. The Beigh Converter of [14] has been the superior design in terms of O-Cost (of 269) till date. The proposed LTeX G2B Converter of Fig. 11a needs O-Cost of 144 resulting in 46.47% less O-Cost requirement compared to the Beigh Counterpart [14]. The use of LTeX modules in the design forces the proposed Gray Converter to excel in terms of Cost_α and the effective area (in nm^2) that reports 57.5% less area compared to the counterpart of Ilanchezhian converter [10]. The gate count is also reduced for LTeX converter as compared to the previous designs as demonstrated in Table 5. Higher the number of gate count, higher will be the value of Cost_α .

Like the B2G Converters, the intended G2B Converter do not exist in the literature that can fix the converter issues in Gray Code Addressing of 8-bit, 16-bit, 32-bit...up to 2^{n-1} -bit

addressable machines. The 4-bit G2B Converters are those which can address 8-bit, 16-bit, 32-bit addressable machines and these are shown in Fig. 10b–d respectively. It can be observed from layouts that the O-Cost becomes 124 for all the 4-bit converters of Fig. 10b–d. The 16-bit addressable machine can use the converter of Fig. 10b whereas the 32-bit and 64-bit addressable machine can use the layouts of Fig. 10c and d respectively. The layouts of Fig. 10b, c and d have taken the effective area of 116204 nm², 158004 nm², and 116204 nm² respectively.

The realization of **high fan-in converters** designs start with the implementations of 8-bit, 16-bit, 32-bit and 64-bit B2G and G2B Converters. The design summary of 8-bit and 16-bit **B2G Converters** with increment index $i=1$ is demonstrated in Table 6. The 8-bit layout of Fig. 11a consumes 224581 nm² effective area with the value of O-Cost 196. The output gets its value exactly at the negative edge of clock 0. The 16-bit binary address B[15:0] is fed to the input of the layout of Fig. 11b to produce the expected gray address G[15:0]. The 16-bit B2G converter layout of Fig. 11b takes 526784 nm² effective area with O-Cost 411. The design summaries of 32-bit and 64-bit B2G Converters are summarized in Table 6.

For the instances of n -bit B2G converters, the percentage improvement can be noted in every aspect of QCA design parameters as compared to Ahmad Converter [15]. Utmost 16.68% improvement has been noted during the O-Cost comparison of 64-bit LTeX Converter. As the delay remains independent with the number of inputs for the n -bit LTeX inverter, so 93.75% improvement has been reported for 64-bit layout comparison with Ahmad Converter counterpart [15]. The Cost analysis of generic LTeX B2G Converter consumes an average of 53.42% reduced value as compared to Ahmad Converter counterpart [15].

This work formulates the QCA design parameters of B2G and G2B Converters in terms of input n for both the cases i.e. $i=k=0$ and $i>1, k\neq 0$ as summarized in Table 7. The *formulation1* is signified with the instantiation of 8-bit B2G Converter with $i=8$ as shown in Fig. 12a. The needs of $O-Cost=176$ and $Cost_{\alpha} =158.25$ verifies the formulations for B2G Converter mentioned in Table 7. The significant advancements are noted in Table 7 in terms of effective area of B2G Converter realizations as n -bit B2G Converter needs $\{(n-1)*0.022080+0.0248\}nm^2$ for $i=1, k=0$ and $\{(n-2)*0.021804+(n-1)*0.02484+0.0276*n\}nm^2$ for $i>1, k\neq 0$. Since the grid matrix for G2B Converter changes with the number of inputs, the mathematical formulation for area of G2B Converter cannot be formulized. The uniform delay of 0.75 makes the B2G Converters ultra-fast amongst

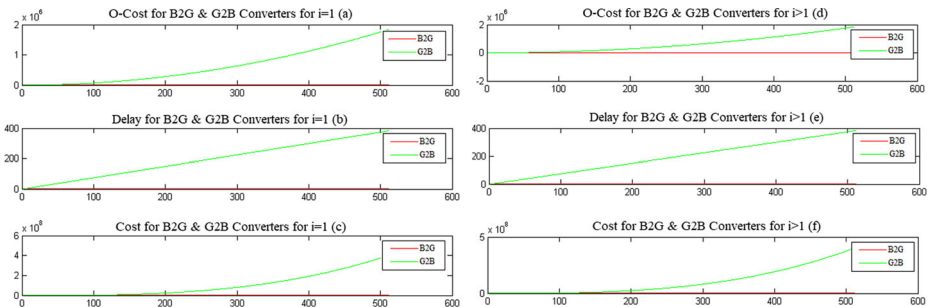


Fig. 13 Analysis of B2G and G2B QCA Circuits in terms of **a** O-Cost for B2G & G2B Converters for $i=1, k=0$, **b** Delay for B2G & G2B Converters for $i=1, k=0$, **c** $Cost_{\alpha}$ for B2G & G2B Converters for $i=1, k=0$, **d** O-Cost for B2G & G2B Converters for $i>1, k\neq 0$, **e** Delay for B2G & G2B Converters for $i>1, k\neq 0$ and **f** $Cost_{\alpha}$ for B2G & G2B Converters for $i>1, k\neq 0$

the other existing B2G Converters. Figure 11c–d are showing the 8-bit, 16-bit **G2B Converters** with index $i=1$. Additionally the G2B converter which is proposed to be used in 64-bit addressable machine is shown as an instance in Fig. 12b. Figure 13a–f analyses the post implementation QCA Design Parameters of B2G and G2B Converters such as O-Cost, Delay and $Cost_{\alpha}$ for conventional implementation schemes ($i=1, k=0$) and Gray addressing implementation schemes ($i>1, k\neq 0$).

7 Conclusion

The B2G and G2B Converters may exist in the literature but the designs, envisioned for the usage in Gray Addressing are not available. This work attempts to explore the designs to achieve the need of efficient generic B2G and G2B Converters with the help of two-input LTeX module. Several compact two-input Exclusive OR Gates are reported in the literature. But the Layered T Exclusive OR Gate is scalable to high fan in circuits and reproducible to generate n-bit Exclusive OR Gate. The defect tolerance analysis of two-input LTeX module is provided to characterize the endurance of the module. After the description of the LTeX module, the novel LTeX methodology consisting of the *formulations* and *corollaries* are proposed. The binary and gray addresses are fetched by the LTeX Converters, are processed accordingly and the required outputs are generated. Apart from the conventional converter designs, the B2G and G2B Converters projected for the use of 2^{n-1} -bit addressable machines are very much essential. Additionally the generic designs of the converters are also proposed with the proper formulations of the QCA metrics like Effective Area, O-Cost, Delay and $Cost_{\alpha}$. The proposed layouts obey the design rules of QCA and utilize minimum clock zones by making the designs ultra-fast so far. During the design of multi-level processor based designs, the usefulness of the LTeX converters are verified by their proper outputs and cost analysis. In each instance, the superior value of the $Cost_{\alpha}$ excels from the other existing designs. So the use of defect tolerant and scalable LTeX converters is highly proposed in the Gray Code based processors and memory designs. As the LTeX Code Converters utilize single layer in their QCA layouts, so the biplanar alternative QCA cells may be used to avoid the complexity during the fabrication of multi-layer QCA circuits.

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Compliance with Ethical Standards

Conflict of interests The authors declare that they have no conflict of interest.

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