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Design of Low-Complexity and High-Speed Coplanar Four-Bit Ripple Carry Adder in QCA Technology

Moslem Balali[1] · **Abdalhossein Rezai**[1]

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Abstract Quantum-dot Cellular Automata (QCA) technology is a suitable technology to replace CMOS technology due to low-power consumption, high-speed and high-density devices. Full adder has an important role in the digital circuit design. This paper presents and evaluates a novel single-layer four-bit QCA Ripple Carry Adder (RCA) circuit. The developed four-bit QCA RCA circuit is based on novel QCA full adder circuit. The developed circuits are simulated using QCADesigner tool version 2.0.3. The simulation results show that the developed circuits have advantages in comparison with existing single-layer and multilayer circuits in terms of cell count, area occupation and circuit latency.

Keywords Quantum-dot cellular automata · One-bit full adder design · Four-bit ripple carry adder · Single-layer design

1 Introduction

Quantum-dot Cellular Automata (QCA) technology, which is a candidate technology to replace CMOS technology, promises extremely dense, extra low-power and high-speed structures at Nano scale [1]. The logic state in this technology is determined based on the position of the electrons in quantum cells [1–5]. On the other hand, full adders have important roles in digital circuits. It is because other logical operations and mathematical functions can be constructed using full adder [1–4]. So, the main object in designed circuits is to reduce complexity (cell count) and occupation area and increase the operation speed.

✉ Abdalhossein Rezai
rezaie@acecr.ac.ir

Moslem Balali
moslembalali59@gmail.com

[1] ACECR Institute of Higher Education, Isfahan Branch, Isfahan 84175-443, Iran

Recently, several efforts have been done to improve the efficiency of the full adder implementation in the QCA technology [6–12]. Roohi et al. [6] have offered a QCA full adder that requires 52 cells, and 0.04 μm^2 area. Sasamal et al. [7] have offered a QCA coplanar one-bit full adder that requires 49 cells, and 0.04 μm^2 area. Navi et al. [8] have presented a QCA full adder using five-input majority gate that requires 61 cells, and 0.03 μm^2 area. The authors of [9] have developed QCA coplanar full adder using 73 cells that has 0.04 μm^2 area. Kianpour et al. [10] have presented a one-bit coplanar full adder using three three-input majority gates that requires 69 cells and 0.07 μm^2 area. Hashemi and Navi [11] have developed QCA coplanar full adder using 71 cells that has 0.06 μm^2 area. Angizi et al. [12] have presented a QCA one-bit full adder using XOR gate and majority gate that requires 95 cells and 0.09 μm^2 area. However, these full adder architectures have advantages, but the complexity and required area of the full adder architecture in the QCA technology can be reduced as described in this paper.

In this paper, we propose a new QCA four-bit Ripple Carry Adder (RCA), which is constructed based on the developed robust QCA one-bit full adder. The developed circuits are simulated using QCADesigner tool. The results demonstrate that the developed circuits have advantages compared to other QCA circuits in terms of speed, area and complexity.

The rest of this paper is organized as follows. In Section 2, an over view of the QCA and related works are presented. A novel QCA one-bit full adder cell is developed in Section 3. In addition, we construct a new four-bit QCA RCA based on this novel full adder. Section 4 compares the developed circuits to other QCA circuits. Finally, Section 5 concludes this paper.

2 Background

This section investigates the QCA cell, QCA wire, QCA gates, QCA full adder circuits and related works.

2.1 QCA Cell

A QCA cell is a square-shape structure that has four quantum dots positioned at the four corners and two electrons. These two electrons can move between the dots [5]. Due to Coulomb repulsion, the diagonally opposite corners are considered as the position of electrons in the QCA cell. The position of the electrons in the QCA cells determines the logic state as shown in Fig. 1 [1–4].

2.2 QCA Wire

QCA contact wires are formed from the same QCA cells that interact with each other to transmit information. Figure 2 shows three types of wire crossing methods in the QCA technology [7].

2.3 QCA Gates

Inverter gate and majority gate are two main gates in the QCA technology. Figure 3 shows three types of the formerly presented inverters [6].

In this figure, the input polarization is inversed when it reaches the output cell.

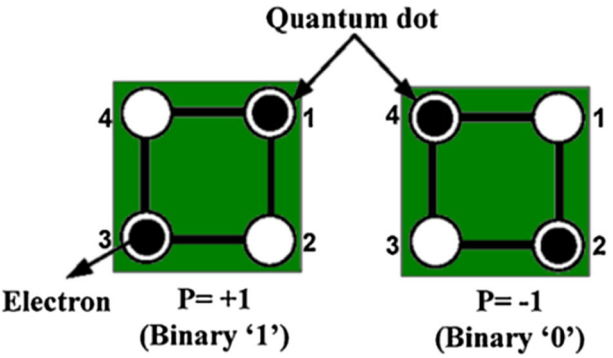

Fig. 1 The possible QCA logic state: logic '0' and logic '1' [1–4]

In the majority gate, the polarization of output cell is determined by voting on the polarization of the input cells. Figure 4 shows two types of three-input majority gate [4].

The logical function of three-input majority gate is shown by following equation [4]:

$$\text{Maj3 (A, B, C)} = AB + AC + BC \tag{1}$$

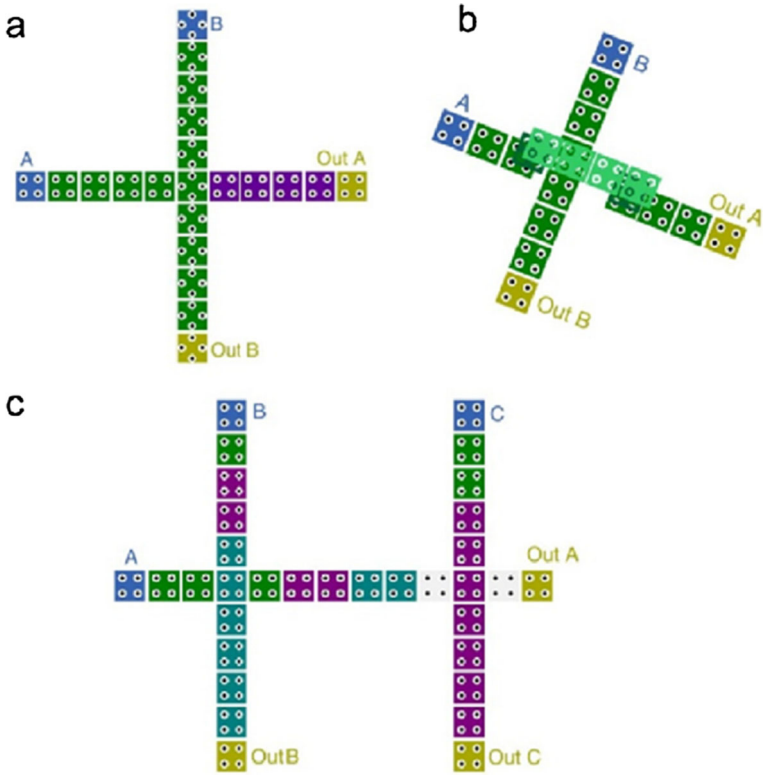

Fig. 2 Wire crossing methods: **a** single layer, **b** multi-layer, **c** logical crossing [7]

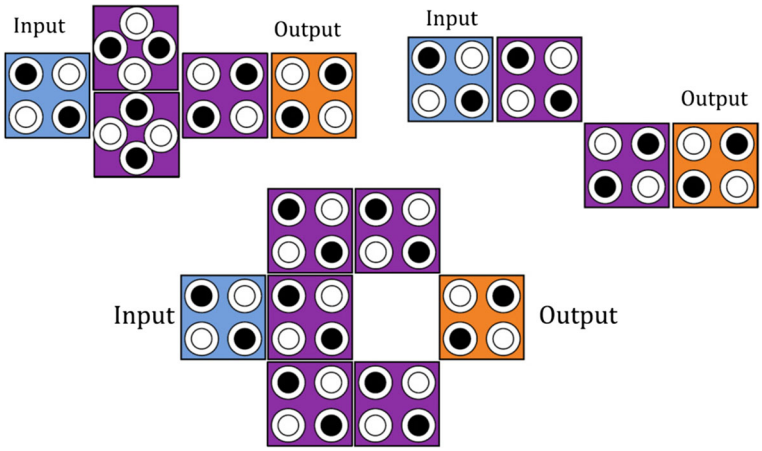

Fig. 3 Three types of inverter [6]

In addition, five-input majority gate is defined according to (2) [7].

$$\begin{aligned} \text{Maj5 (A, B, C, D, E)} = {} & \text{ABC} + \text{ABD} + \text{ABE} + \text{ACD} + \text{ACE} + \text{ADE} \\ & + \text{BCD} + \text{BCE} + \text{BDE} + \text{CDE} \end{aligned} \tag{2}$$

Figure 5 shows three types of five-input majority gate [8, 9, 13].

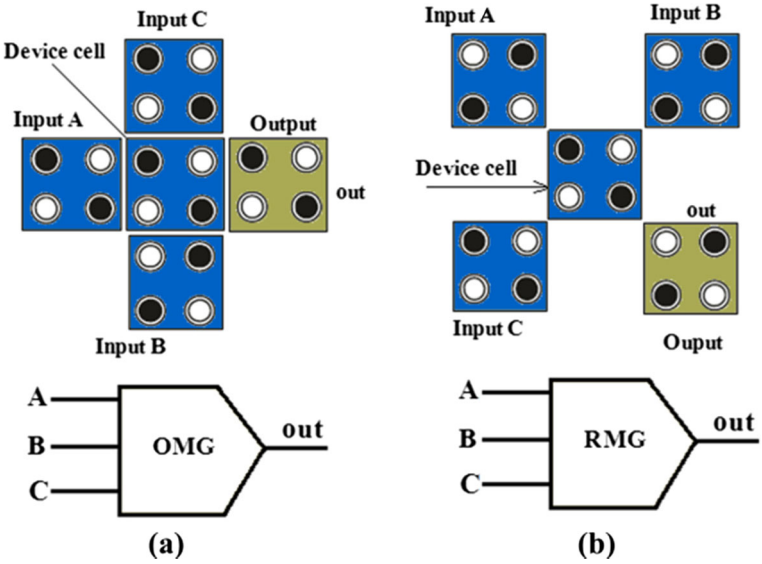

Fig. 4 Two types of three-input majority gate: **a** Original Majority Gate (OMG), **b** Rotate Majority Gate (RMG) [4]

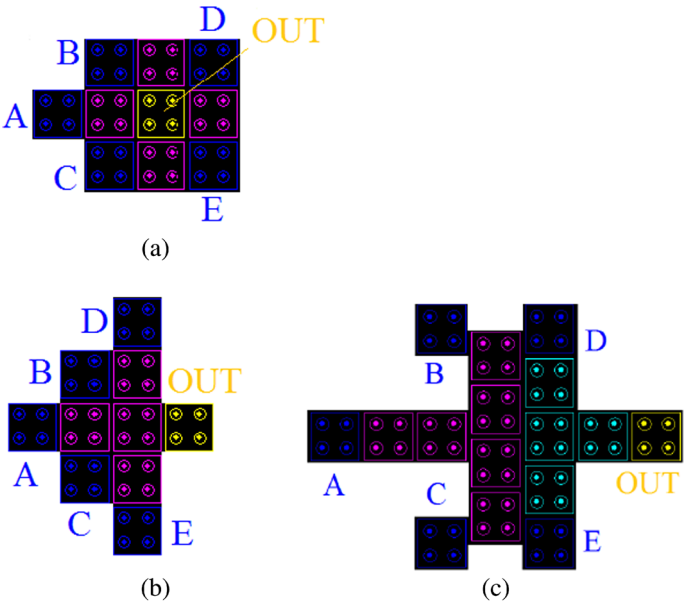

Fig. 5 Three types of five-input majority gate, **a** in [8] **b** in [9] **c** in [13]

2.4 QCA Full Adder

In the full adder with inputs A, B and Cin, the outputs of sum and $\text{Carry}_{\text{out}}$ are calculated as follows [14]:

$$\text{Carry}_{\text{out}} = \text{AB} + \text{BCin} + \text{ACin} \tag{3}$$

$$\text{Sum} = \text{ABCin} + \overline{\text{A}}\,\overline{\text{B}}\text{Cin} + \overline{\text{AB}}\,\overline{\text{C in}} + \text{A}\overline{\text{BCin}} = \text{A} \oplus \text{B} \oplus \text{Cin} \tag{4}$$

To design the full adder in the QCA technology, $\text{Carry}_{\text{out}}$ can be reformulated as follows:

$$\text{Carry}_{\text{out}} = \text{Maj3(A, B, Cin)} \tag{5}$$

In addition, sum can be reformulated as follows [15–17]:

$$\begin{aligned}
\text{Sum} &= \text{Maj3}(\text{Maj3}(\text{A, B, Cin}), \text{Maj3}(\text{A, B, Cin}), \text{Maj3}(\text{A, B, Cin})) \\
&= \text{Maj3}(\overline{\text{Carry}_{\text{out}}}, \text{Maj3}(\text{A, B}, \overline{\text{Carry}_{\text{out}}}), \text{Cin}) \\
&= \text{Maj3}(\overline{\text{Carry}_{\text{out}}}, \text{Maj3}(\text{A, B}, \overline{\text{Carry}_{\text{out}}}), \text{B}) \\
&= \text{Maj3}(\overline{\text{Carry}_{\text{out}}}, \text{Maj3}(\text{B, Cin}, \overline{\text{Carry}_{\text{out}}}), \text{A}) \\
&= \text{Maj5}(\overline{\text{Carry}_{\text{out}}}, \overline{\text{Carry}_{\text{out}}}, \text{Cin, A, B})
\end{aligned} \tag{6}$$

So, this output can be implemented using five-input majority gate.

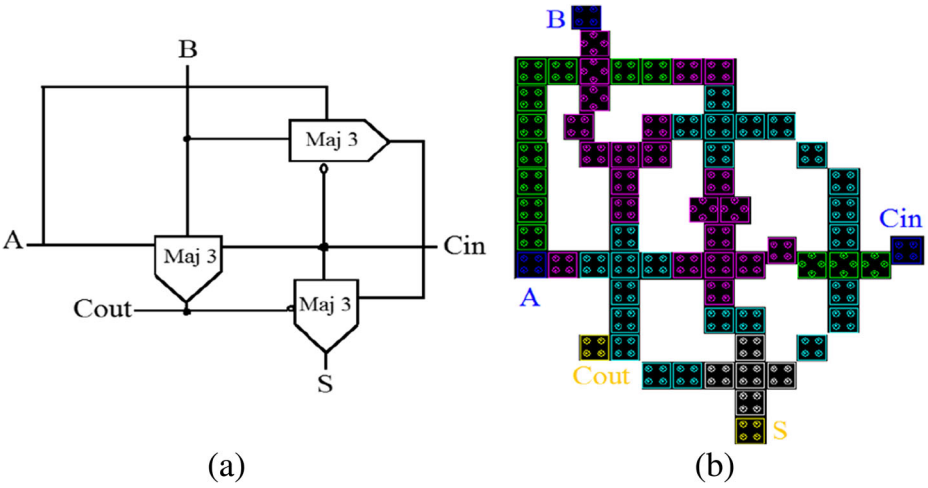

Fig. 6 The QCA full adder in [10] **a** logical diagram **b** QCA layout

2.5 Previously Reported Designs

Kianpour et al. [10] presents a one-bit coplanar full adder using only three three-input majority gates as shown in Fig. 6.

This full adder is consists of 69 cells, which has a 0.07 μm^2 area. The latency of this full adder is 1 clock cycle.

The authors of [11] have developed QCA coplanar full adder using 71 cells as shown in Fig. 7.

In this full adder, the latency is 1.25 clock cycle, and the area is 0.06 μm^2. According to Fig. 7, this full adder consists of one three-input majority gate, one five-input majority gate

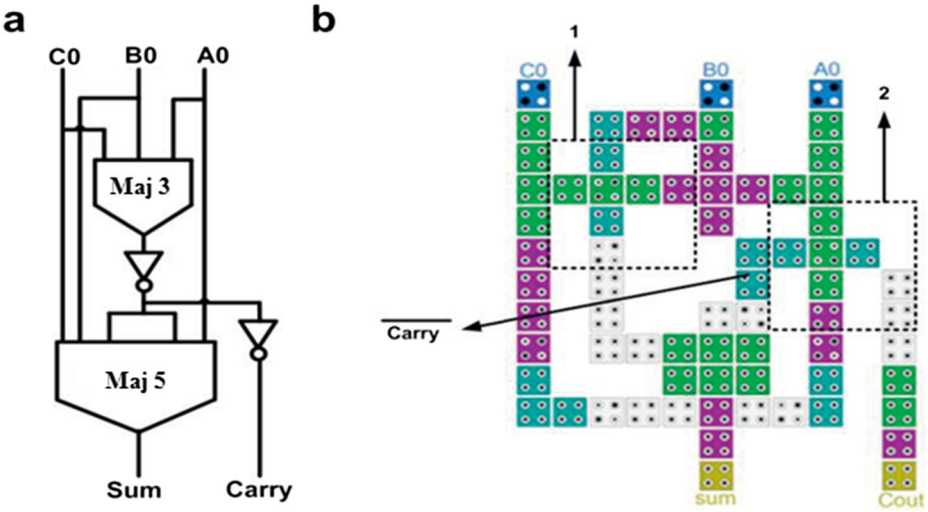

Fig. 7 The QCA full adder in [11] **a** logical diagram **b** QCA layout

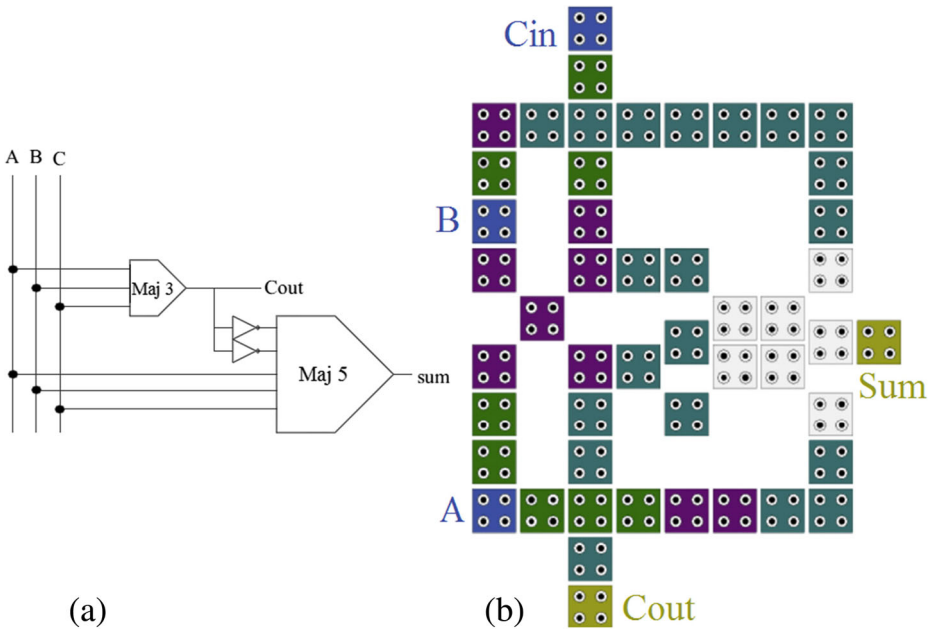

Fig. 8 The QCA full adder in [7] **a** logical diagram **b** QCA layout

and two inverter gates. Sasamal et al. [7] presents a QCA coplanar one-bit full adder, which is shown in Fig. 8.

This full adder has less complexity in comparison with two designs in [10, 11]. It is consists of 49 cells, which has a 0.04 μm^2 area, the latency is 1 clock cycle as using one three-input majority gate, one five-input majority gate and two inverter gates.

In addition, Angizi et al. [12] presents a QCA coplanar four-bit Ripple Carry Adder (RCA), using 494 cells as shown in Fig. 9. The latency of this design is 4.25 clock cycles, which has a 0.68 μm^2 area.

The authors of [14] have developed the QCA coplanar four-bit RCA using 262 cells as shown in Fig. 10. The latency of this design is 1.75 clock cycles, which has a 0.208 μm^2 area.

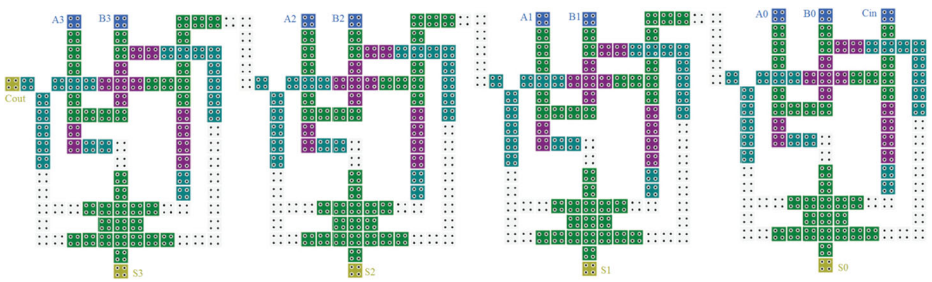

Fig. 9 The layout of four-bit QCA RCA in [12]

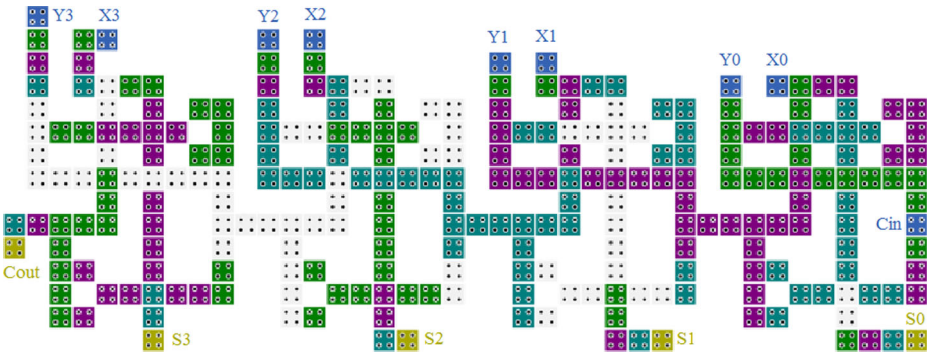

Fig. 10 The layout of four-bit QCA RCA in [14]

Mohammadi et al. [19] have developed the QCA multilayer four-bit RCA using 237 cells as shown in Fig. 11. The latency of this design is 1.5 clock cycles, which has a 0.24 μm^2 area. There are three layers of cells in this design.

3 The Developed Circuits

This section presents a novel QCA one-bit full adder. Then a novel QCA coplanar four-bit RCA circuit is presented based on this one-bit full adder.

3.1 The Developed QCA One-bit Full Adder Circuit

In this section, a robust QCA one-bit full-adder is presented. Figure 12 demonstrates the structure of the developed QCA full adder circuit.

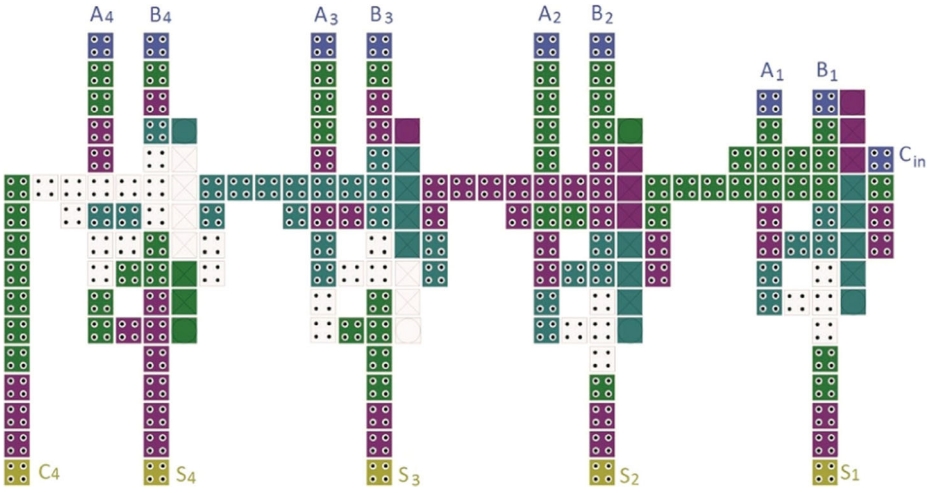

Fig. 11 The layout of four-bit QCA RCA in [19]

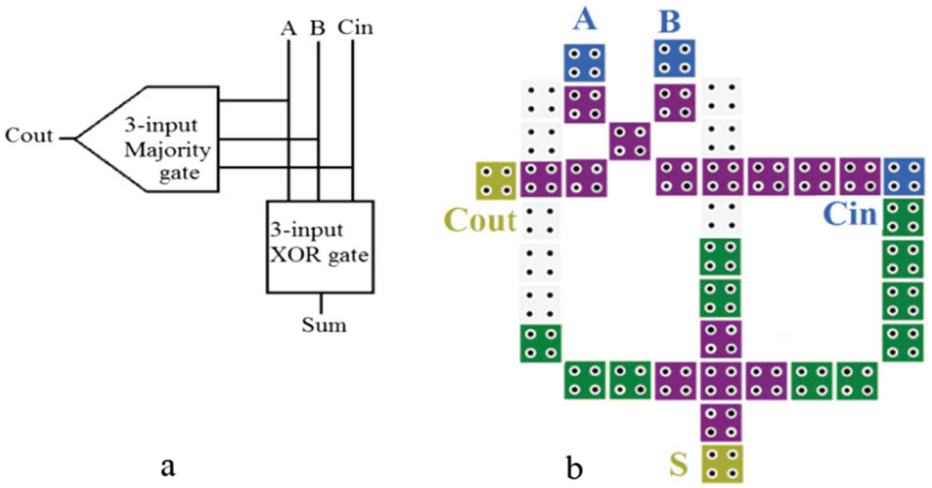

Fig. 12 The developed QCA full adder: **a** block diagram **b** layout

As it is shown in this figure, the carry is produced using the three-input majority gate and the sum is produced using a three-input QCA XOR. The arrangement of inputs and outputs of cells in this full adder is such that it can be used in both single-layer design and multilayer design.

3.2 The Developed Four-bit QCA RCA Circuit

Figure 13 shows the developed four-bit QCA RCA circuit, which is utilized the developed QCA one-bit full-adder as its structured unit.

The developed four-bit RCA is consists of 209 cells, which has a 0.3 μm^2 area. So, the cells are also located in four clock cycles and latency of circuit is 1.25 clock cycles.

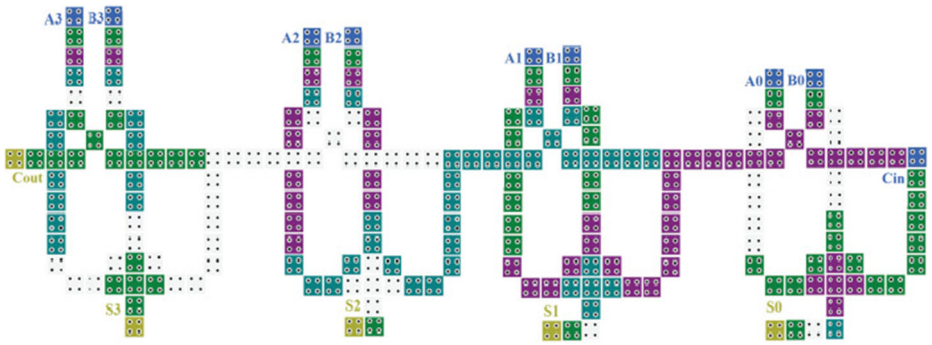

Fig. 13 The layout of the developed four-bit QCA RCA

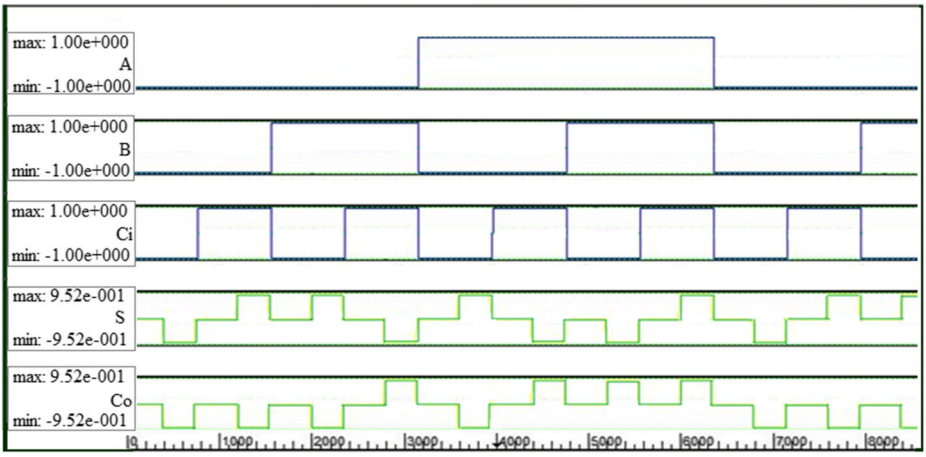

Fig. 14 The simulation results for the developed one-bit full adder

4 Simulation and Comparison Results

This section outlines the simulation results for the developed circuits and compares these results with other circuits. In this section, the cost value is computed using (7):

$$\text{Cost} = \text{Latency} \times \text{Area} \tag{7}$$

Where Latency denotes the number of required clock cycle and Area is shown in terms of μm^2.

4.1 The Developed QCA One-bit Full Adder Circuit

Figure 14 shows the simulation results for the developed QCA one-bit full adder.

As it is shown in the achieved simulation waveform in Fig. 14, the developed circuit for the QCA full adder performs correctly. Table 1 shows the extensive comparison of the developed QCA full adder with other QCA full adders in [6–12].

Table 1 Comparison table for the QCA full adders

Ref.	Number of required cells	Area (μm^2)	Latency (clock cycle)	Cross-over type	Cost
[12]	95	0.09	1.25	Coplanar	0.1125
[11]	71	0.06	1.25	Coplanar	0.075
[8]	61	0.03	0.75	Coplanar	0.0225
[9]	73	0.04	0.75	Coplanar	0.03
[10]	69	0.07	1	Coplanar	0.07
[6]	52	0.04	0.75	Multilayer	0.03
[7]	49	0.04	1	Coplanar	0.04
This paper	41	0.04	0.5	Coplanar	0.02

According to Table 1, our simulation results demonstrate that the developed QCA full adder provides an improvement in terms of area occupation, cell count, circuit latency and cost in comparison with other QCA full adder circuits in [6–12], which are implemented in single-layer. However the developed one-bit QCA full adder is also competitive with multilayer designs.

In particular, the cell count, latency and cost of the developed full adder are reduced by about 16%, 50% and 50% in comparison with QCA full adder in [7]. Despite similar area to that of the multilayer design presented in [6], our developed design surpasses it by 21%, 33%, and 33% improvements in terms of cell count, latency and cost, respectively.

4.2 The Developed High-speed Four-bit RCA

The simulation results of the developed four-bit QCA RCA are shown in Fig. 15.

According to Fig. 15, after 1.25 clock cycles delay, the sum of the inputs (A, B, C_{in}) is calculated, which is absolutely corrected. Table 2 contains a comparison between our developed four-bit QCA RCA and other four-bit QCA RCA circuits.

Based on our simulation results, which are shown in Table 2, the developed design has the lowest circuit latency and cell count compared to other QCA RCA designs in [11, 12, 14, 19–23]. In particular, the design in [14] has a lower area occupation than our developed design, but the developed design is able to counteract that by having a lower latency and cell count, as there are 20% and 28% improvements in cell count and circuit latency, respectively.

According to Table 2, our developed four-bit QCA RCA has the minimum value in terms of the circuit latency except the design in [24]. In comparison to [24], it is worth noting that application of the design in [24] is only in multilayer design and it cannot be used in single-layer. In other words, our developed design has highest-speed coplanar design in single-layer applications, so far.

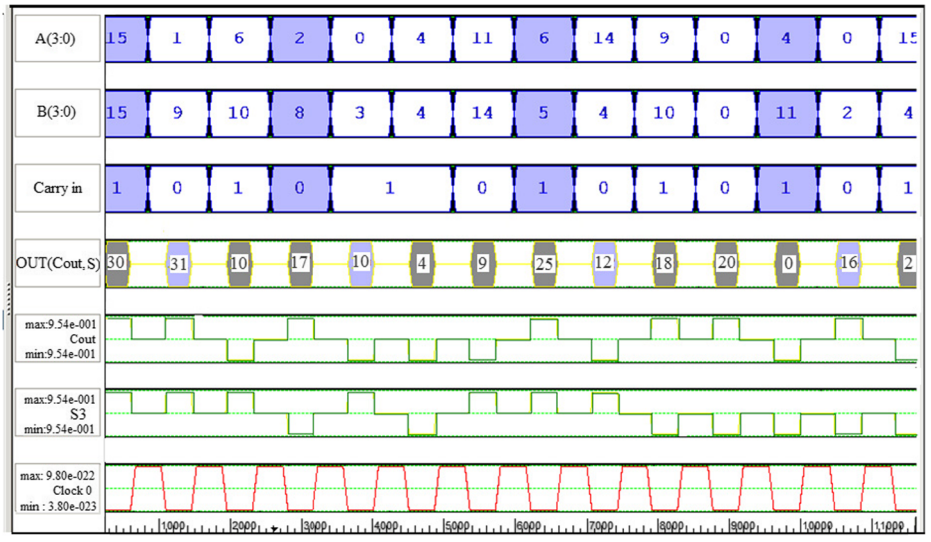

Fig. 15 The simulation results for the developed four-bit RCA

Table 2 Comparison table for the QCA four-bit RCA

Ref.	Number of required cells	Area (μm^2)	Latency (clock cycle)	Cross-over type	Application type	Cost
[20]	1246	2.5	3.25	Coplanar	Coplanar	8.125
[12]	494	0.68	4.25	Coplanar	Coplanar	2.89
[23]	269	0.37	3.5	Coplanar	Coplanar	1.295
[11]	442	1	2	Coplanar	Coplanar	2
[21]	308	0.29	2	Multilayer	Multilayer	0.58
[14]	262	0.208	1.75	Coplanar	Coplanar	0.364
[19]	237	0.24	1.5	Multilayer	Multilayer	0.36
[22]	295	0.3	1.5	Coplanar	Coplanar	0.45
[24]	175	0.14	1	Coplanar	Multilayer	0.14
This paper	209	0.3	1.25	Coplanar	Coplanar	0.375

5 Conclusion

The QCA is a suitable alternative for CMOS technology at Nano-scale level due to low-power consumption, high-speed and high-density devices. On the other hand, full adder is one of the most important circuits in logical operations and mathematical functions such as multipliers. In this paper, a novel QCA structure was developed for one-bit full adder. We also used this new one-bit full adder to design a robust, efficient and high-speed four-bit RCA in the QCA technology. Our simulation results showed that our developed designs have yielded significant improvements in term of circuit latency and speed.

According to results and tables, among the designs that are single-layer and have coplanar application, the cell count and circuit latency of the developed coplanar four-bit RCA are considerably reduced. The developed four-bit ripple carry adder in the QCA technology has high-speed and low-complexity design, so far.

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