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Modular Adder Designs Using Optimal Reversible and Fault Tolerant Gates in Field-Coupled QCA Nanocomputing

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Abstract The challenges which the CMOS technology is facing toward the end of the technology roadmap calls for an investigation of various logical and technological solutions to CMOS at the nano scale. Two such paradigms which are considered in this paper are the reversible logic and the quantum-dot cellular automata (QCA) nanotechnology. Firstly, a new 3×3 reversible and universal gate, RG-QCA, is proposed and implemented in QCA technology using conventional 3-input majority voter based logic. Further the gate is optimized by using explicit interaction of cells and this optimized gate is then used to design an optimized modular full adder in QCA. Another configuration of RG-QCA gate, CRG-QCA, is then proposed which is a 4×4 gate and includes the fault tolerant characteristics and parity preserving nature. The proposed CRG-QCA gate is then tested to design a fault tolerant full adder circuit. Extensive comparisons of gate and adder circuits are drawn with the existing literature and it is envisaged that our proposed designs perform better and are cost efficient in QCA technology.

Keywords Adder · Fault tolerant design · QCA · Clocking · Reversible gate · Universal gate · Nanotechnology · Quantum cells

1 Introduction

The boom that the electronics industry has seen in the last few decades is due to the evident success of the CMOS technology and the miniaturization that has been possible due to the scaling of the basic MOS structure. This paradigm of scaling has helped in maintaining the famous Moore's law for the industry [1] according to which the number of components on a

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single chip doubles after approximately every two years. The growth suggests an exponential nature which is hard to maintain since no exponential can continue forever [2]. The ITRS (International Technology and Roadmap for Semiconductors) has pointed out the asperities which the CMOS is facing in surviving through the nano regime and it now seems that the CMOS technology is approaching the end of the roadmap.

In the nano scale the classical laws are no longer applicable for the device and the various quantum mechanical effects start dominating the device physics [3]. Though the present generation CMOS technology is 22 nm [4] many aftereffects can and will arise due to the reduction in the feature size in future. Few such consequences are in terms of leakage currents, power dissipation, oxide thickness, crosstalk and electron-migration. All these effects and consequences call for the development of alternate paradigms for the CMOS in nano regime [5–8]. Reversible logic and QCA nanotechnology form two such promising alternatives. The following sub-sections present a brief introduction of reversible circuits and QCA technology.

1.1 Reversible Logic

According to Landauer [9], the processing of information in digital circuits leads to the generation of heat due to erasing of bits during the process. This is because of the entropy changes accompanied with the destruction of information. He suggested that for every bit of information that is erased KTln2 joules of energy is dissipated. A few decades back this quantity was negligible since the power dissipation of the circuits was high but as the industry moves toward the ultra-low power architectures this quantity is becoming a matter of concern for VLSI circuits [10]. For targeting this heat generation, reversible logic is the proposed solution. According to this logic if the erasing of the bits is avoided in digital circuits the KTln2 joules of energy loss can be avoided [11–15]. A device is said to be logically reversible if there is a one-to-one mapping between the inputs and outputs and the number of inputs and outputs are equal. Besides this logical reversibility the physical reversibility is also important. This means that the technology that can be used for the implementation of these reversible circuits should be a system which is quantum mechanically reversible. Since CMOS doesn't satisfy this, new technology alternatives are needed for the implementation of the reversible logic design. One of the technologies which stands as an alternative to the CMOS technology in nano regime and also design the reversible circuits is QCA.

1.2 QCA Nanotechnology

One of the most promising technology as seen by the researchers is the nanotechnology based Quantum Cellular Automata [16–19]. This technology incorporates a shift from the conventional transistorized designs to designing using nano structures like quantum dots or metal islands. This archetype works on the principles of quantum physics and uses the effects that were a threat to CMOS to its advantage. It was first proposed in 1993 by Craig S. Lent, P. Douglas Tougaw, Wolfgang Porod and Gary H. Bernsteain, at the University of Notre Dame. Quantum-dot Cellular Automata (QCA) is a newly developed paradigm for digital design and offers a breakthrough required for the fulfillment of certain lacking aspects of CMOS technology in the nano regime. Since the technology is new and in the premature phase a lot of scope lies ahead of researchers to take the designing using QCA to a commercial level. The basic component in the QCA circuits consists of a QCA cell as shown in Fig. 1.

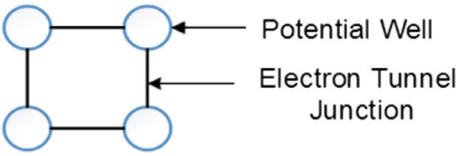

Fig. 1 Illustration of a basic QCA cell

The basic cell consists of four quantum dots or metal islands in which two electrons are allowed to localize. The dots are separated by tunnel junctions through which the electrons can move from one site to another. The basic mechanism of working of the cell is the coulombic repulsion between the cells and the quantum mechanical tunneling. Due to coulombic forces the electrons are allowed to only occupy the antipodal sites. This results in two polarization states called the binary zero and the binary one as shown in Fig. 2.

The cell to cell interactions are responsible for the transmission of information between the cells and hence no currents are involved in this technology. The polarization of one cell impacts the polarization of the other cell and so on. The basic building blocks in QCA are the binary wire, the inverter and the majority voter [34, 35]. The basic cell in QCA technology performs both transmission and processing. Various circuits in the designing require crossing of wires just like in CMOS circuits. This is implemented in QCA using QCA wire crossing. There are two types of wire crossings in QCA viz. the multilayer crossover and the coplanar crossover [20, 21].

For the proper functioning of the QCA circuits, they are provided with the clock signal which controls the information flow and also provides the true power gain in the circuits. The clock is provided in four zones with each zone consisting of four phases. The four phases are the switch, hold, release and relax. The clock signal is responsible for raising and lowering the barrier between the sites of electron localization. During the switch phase the barriers are lowered and the electrons are influenced by the neighboring cell polarizations. The switch phase is followed by the hold phase in which the cell is latched and retains its polarization state. During the release and relax phases the cell again loses its polarization and attains a null state. The clock phases need to follow each other in the above sequence for proper information flow via pipelining. The entire clocking process and its different phases are shown in Fig. 3.

The different clock zones in QCA are represented by different colors e.g. clock zone 0 is represented by green, clock zone 1 by magenta, clock zone 2 by blue and clock zone 3 by white in QCA Designer 2.0.3 simulator [22–26]. For the designing of the circuits in QCA, various parameters of designing need to be taken into consideration. These include the cell count, cell area, total area, latency and complexity of the designs.

The rest of the paper has been organized as follows. The proposed 3 × 3 reversible gate (RG-QCA) and its two implementations using majority voter approach and explicit interaction

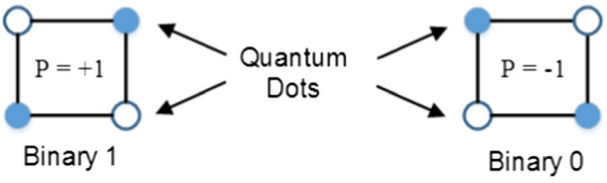

Fig. 2 QCA cell polarizations and representations of binary 1 and binary 0

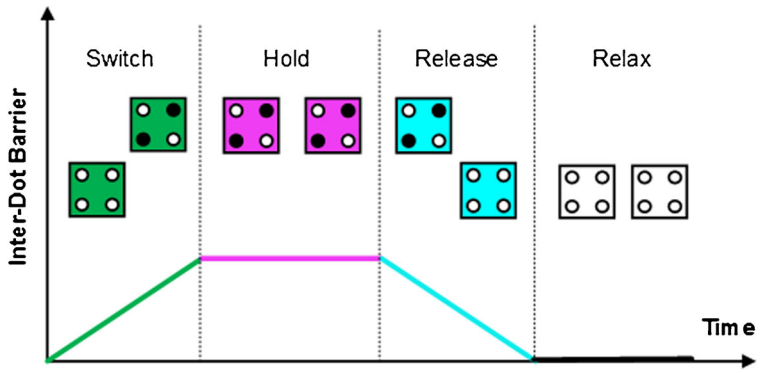

Fig. 3 Illustration of clocking and different clock phases in QCA

of cells is presented in Section 2 followed by validation of proposed reversible gate as a universal structure and its hardware complexity in Sections 3 and 4 respectively. The full adder design using proposed RG-QCA gate and its QCA implementation is presented in Section 5. The CRG-QCA gate, which is the optimized RG-QCA gate with additional fault tolerance characteristics, is presented in Section 6 followed by the design and QCA implementation of optimal fault tolerant full adder circuit. Finally, the performance comparison of proposed designs with other state-of-the-art designs from the literature is presented in Section 7 followed by the conclusion.

2 Proposed Reversible RG-QCA Gate

In this work, a new 3 × 3 reversible logic gate called the RG-QCA (Reversible Gate–Quantum-dot Cellular Automata) is proposed. The equations at the output of the reversible gate are designed in order to be most suitable for digital circuit implementation. The proposed RG-QCA gate is a 3 input and 3 output gate having its input vector (IV) and output vector (OV) as:

$$IV = (A, B, C) \tag{1}$$

$$OV = (P = A \oplus B, Q = AB + BC + AC, R = B'C + A(B \oplus C)') \tag{2}$$

The block diagram of the proposed gate is shown in Fig. 4 and the truth table verifying the gate as reversible is shown in Table 1.

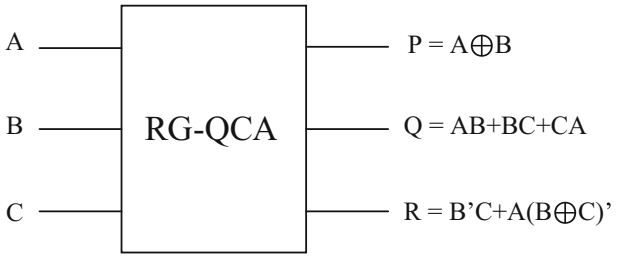

Fig. 4 Block diagram representation of proposed RG-QCA gate

Table 1 Truth table of proposed RG-QCA gate

Input encoding	Input A	B	C	Output P	Q	R	Output encoding
0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	*1*
2	0	1	0	1	0	0	*4*
3	0	1	1	1	1	0	*6*
4	1	0	0	1	0	1	*5*
5	1	0	1	1	1	1	*7*
6	1	1	0	0	1	0	2
7	1	1	1	0	1	1	3

From the above truth table the reversibility of the proposed gate can be verified. As is explicit from the table, there is a one-to-one mapping between the inputs and outputs, which means that for a particular input combination, a unique output combination is present. This reversibility is achieved by designing the equations for the gate appropriately. The encoding as seen from the truth table is different on input and output side but all the combinations are present on both sides.

2.1 RG-QCA Using Conventional Majority Gate Approach

The simplest implementation of RG-QCA gate in QCA can be achieved using the conventional majority voter approach. This design has a large cell count and hence the area and latency of the circuit are also on the higher side. The total cell count of this design is 427 cells which is quite a large number for any QCA design. The QCA implementation of RG-QCA and its simulation waveform are shown in Fig. 5.

The majority equations for the outputs of the gate can be written as in (3)–(5) and the block diagram representation of the majority equations is given in Appendix A.

$$P = M\left[M(A', B, -1), M(A, B', -1), 1\right] \tag{3}$$

$$Q = M\left[M\left[M(A, B, -1), M(B, C, -1), 1\right], M(A, C, -1), 1\right] \tag{4}$$

$$R = M\left[M(B', C, -1), \left[M\left[M(B', C, -1), M(B, C', -1), 1\right]'\right], A, -1, 1\right] \tag{5}$$

2.2 RG-QCA Using Explicit Interaction of Cells

For obtaining the most efficient design of the RG-QCA, the gate is redesigned using the best approaches available in literature. Mostly the approaches of explicit interaction of cells has been used in the new design [33]. The final optimized design obtained is highly efficient as compared to the majority logic designs. The cell count of 143 cells including one multilayer crossover has been used in the realization of the RG-QCA. The proposed RG-QCA is shown in Fig. 6.

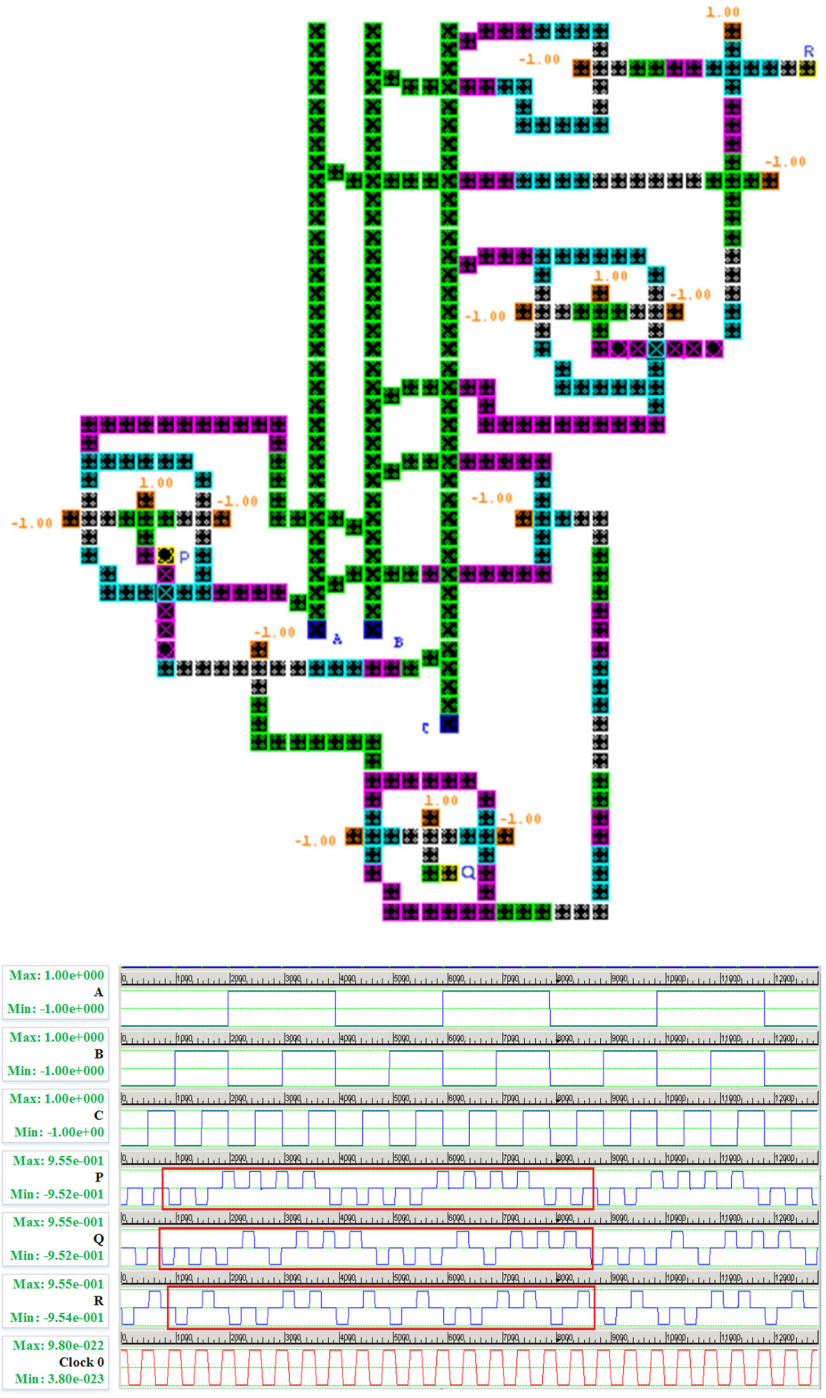

Fig. 5 QCA implementation and simulation waveforms of proposed RG-QCA gate using majority gate approach

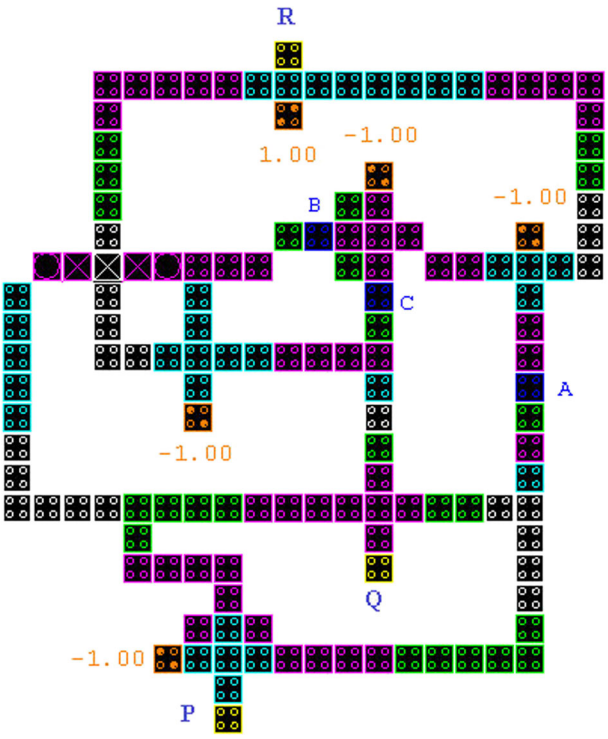

Fig. 6 QCA implementation of proposed RG-QCA gate using explicit interaction of cells

The performance parameters of the RG-QCA using the conventional majority voter approach and the explicit interaction of cells are discussed in Section 7, Table 9. The percentage improvement that is obtained using the explicit interaction of cells is also shown.

3 RG-QCA as a Universal Structure

For a gate to be efficient the functionality of the gate is the prime parameter. This refers to the maximum number of basic Boolean operations that the gate can perform. A gate is said to be universal if it can implement all the seven basic Boolean functions. The RG-QCA can act as a universal gate by manipulating the various inputs of the gate. The inputs required for each function implementation are given in Table 2.

4 Hardware Complexity of RG-QGA Gate

In the case of the reversible circuits, one important parameter to measure the complexity of the implemented hardware is defined by the number of Exclusive-OR functions and the number of AND and NOT operations that are required to realize the outputs of the gate. The logical calculation for Ex-OR operation is calculated as α, for the AND operation the logical calculation is given by β and for the NOT operation the calculation is defined by the γ.

Table 2 Implementation of various logic gates using RG-QCA gate

S.No.	Logic gate	RG-QCA function
1	NOT	RG-QCA (A,1,0)
2	AND	RG-QCA (A,B,0)
3	NAND	RG-QCA (A′,B′1)
4	OR	RG-QCA (A,B,1)
5	NOR	RG-QCA (0,B,C′)
6	Ex-OR	RG-QCA (A,B,C)
7	Ex-NOR	RG-QCA (A,B′,0)

From the equations of RG-QCA we can observe that the equations can be modified to include only these three operations without any change or threat to the reversibility of the gate. The equations for RG-QCA can thus be rewritten as,

$$P = A \oplus B \tag{6}$$

$$Q = (A \oplus B)\, C \oplus AB \tag{7}$$

$$R = B'C \oplus A\,(B \oplus C)' \tag{8}$$

From the above equations we see that there is a slight modification in the outputs Q and R, however these variations do not incorporate any changes in the truth table of the RG-QCA and thus can be used interchangeably with the previous RG-QCA output equations. Now the overall hardware complexity can be calculated by counting the number of Ex-OR, AND and NOT operations in the final equations. This results in the following equation for the hardware complexity of RG-QCA. Total Logical Calculation is given as:

$$5\alpha + 4\beta + 2\gamma \tag{9}$$

where α, β and γ are the logical calculations for Ex-OR, AND and NOT respectively.

The proposed RG-QCA gate can also be used to implement the 13 standard logic functions. Table 3 shows the gate count and reversible parameters like the garbage output and constant input for the implementation of these functions.

Table 3 Implementation of 13 standard logic functions using RG-QCA gate

S.No.	Function	No. of gates	Constant output	Garbage output
1	ABC	2	2	4
2	AB	1	1	2
3	AB+BC+AC	1	0	2
4	A	1	1	2
5	A′BC+A′B′	2	1	4
6	AB+A′B′	1	0	2
7	ABC′+A′BC+A′B′C′	5	5	10
8	A′BC+AB′C+ABC′+ABC	1	0	2
9	ABC+AB′C′	5	5	10
10	AB+B′C	3	3	6
11	AB+BC	2	2	4
12	AB+A′B′C	5	6	10
13	AB+BC+A′B′C′	5	5	10

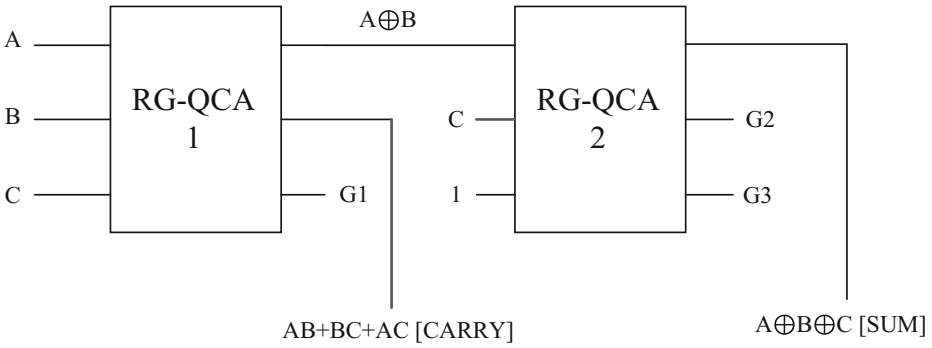

Fig. 7 Block diagram of full adder design using proposed RG-QCA gate

5 Full Adder Design Using RG-QCA

From the extensive literature survey that we have done on reversible circuits and QCA we have realized the need for optimized designs of the adder circuits in QCA nano-technology. Adders form the core component of almost all the digital circuits which include the DSP processors, filters, microprocessors etc. The overall performance of the system is highly dependent on the type, speed and performance of the adder circuits incorporated in it. So the current research also focuses on the arithmetic units (like addition) in the reversible logic [27–32].

The adder designs in existing literature majorly focus on designs using modified adder equations and not on design using gate which can have additional functionalities in other digital components and architectures. In this paper, a new architecture for the design of full adder using the proposed RG-QCA which is based on explicit interaction of cells [33] has been proposed.

The various parameters of reversible logic which include the garbage output, constant input and quantum cost along with the various parameters in QCA that are the cell count, cell area, total area, latency have been taken into consideration in the design. The design of the new full adder requires two RG-QCA gates for implementation and results in the production of three garbage outputs and needs one constant input. The block diagram representation of the adder is shown in Fig. 7 along with the truth table of the adder in Table 4 to verify the results at the output.

Table 4 Truth table of full adder using RG-QCA gate

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

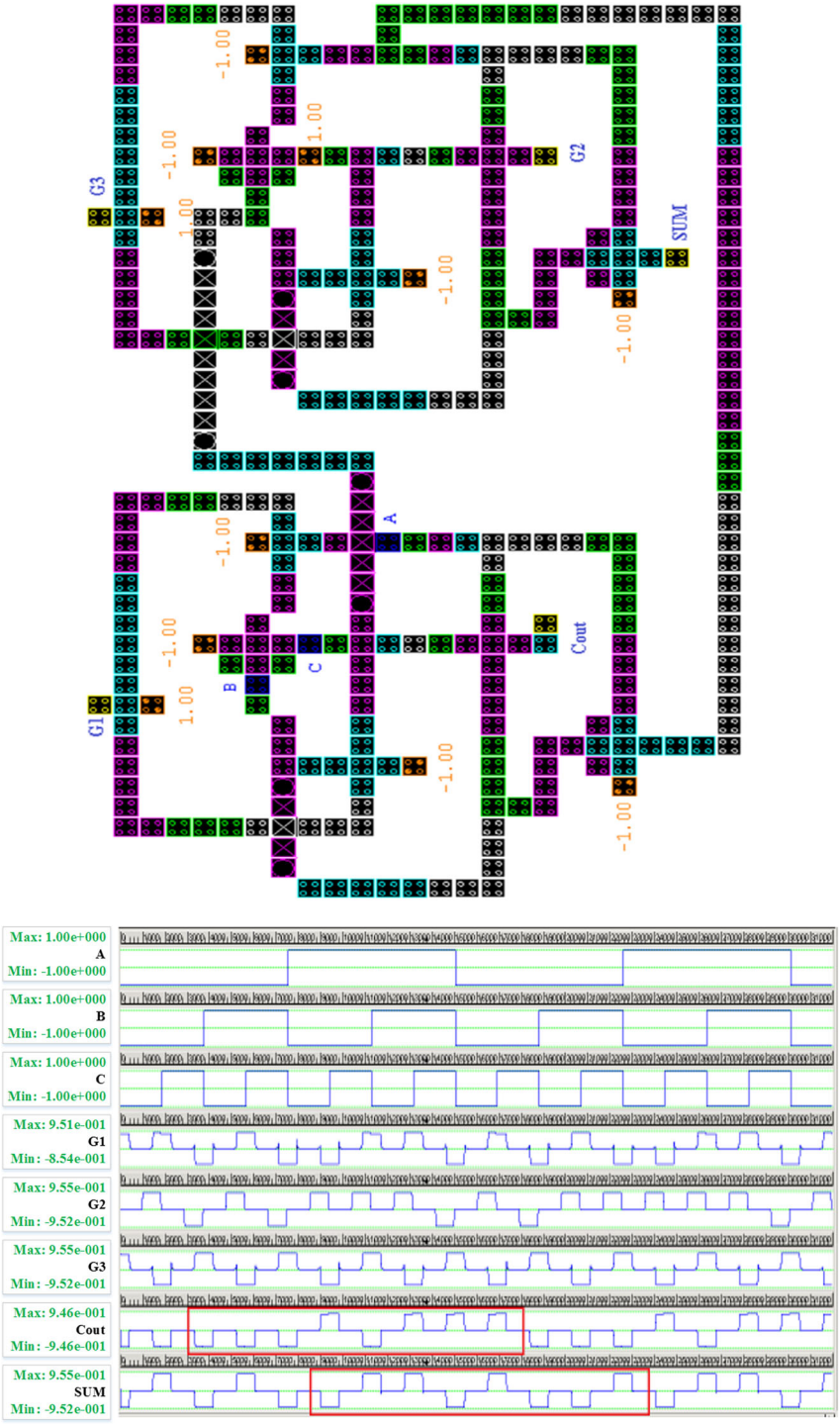

Fig. 8 QCA implementation and simulation waveforms of full adder using proposed RG-QCA gate

Table 5 Performance parameters of full adder design using RG-QCA gate

Parameters	Value
No. of cells	375
Cell area	0.1215 μm^2
Total area	0.37065 μm^2
Latency	4.75
Number of crossovers	4

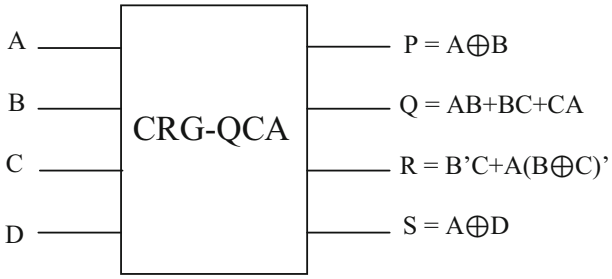

Fig. 9 Block diagram of proposed fault tolerant CRG-QCA gate

Table 6 Truth table of CRG-QCA gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	1	0	0	0
0	1	0	1	1	0	0	1
0	1	1	0	1	1	0	0
0	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1
1	0	0	1	1	0	1	0
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	0	1	0	1
1	1	0	1	0	1	0	0
1	1	1	0	0	1	1	1
1	1	1	1	0	1	1	0

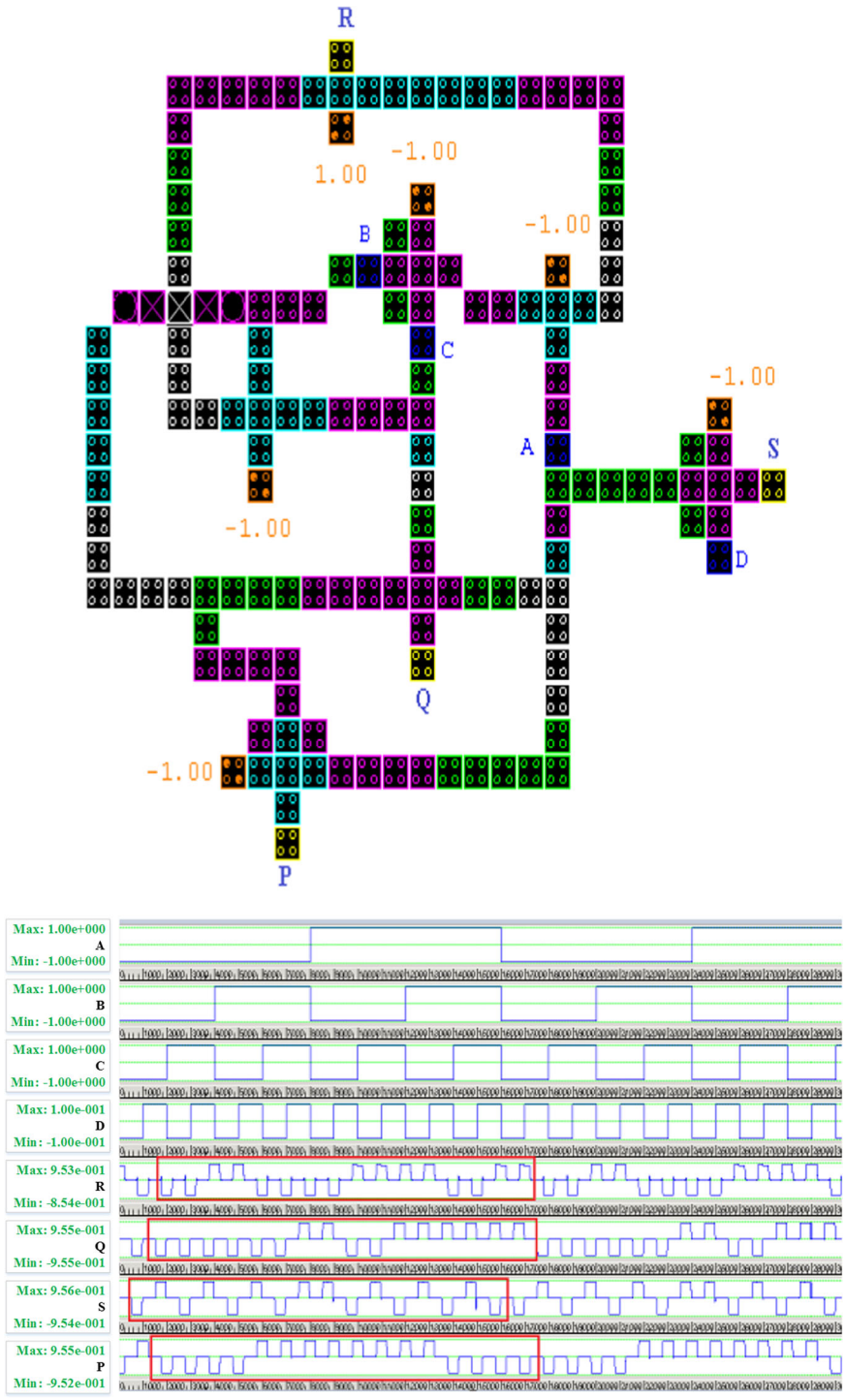

Fig. 10 QCA implementation and simulation waveforms of proposed fault tolerant CRG-QCA gate

Table 7 Performance parameters of fault tolerant CRG-QCA gate

Parameters	Value
No. of cells	157
Cell area	0.0508 μm^2
Total area	0.193 μm^2
Latency	1.75
Number of crossovers	1

The implemented design and simulation results in QCA Designer are shown in Fig. 8. The explicit interaction of cells not only leads to efficient designing but also improved QCA parameter considerations [34, 35]. The performance parameters of the designs of full adder circuit using the proposed RG-QCA are shown in Table 5. The design of the adder in QCA uses the most efficient design techniques. It is observed that the adder has been designed using a cell count of only 375 cells resulting in an area of 0.1215 μm^2 and a total area of 0.37 μm^2.

6 Fault Tolerant Designs Using RG-QCA

One of the most important characteristics of the efficient gate design in both reversible logic as well as the QCA technology is extending the design of the gate to include the fault tolerant characteristics. For the proposed RG-QCA gate, the fault tolerant feature is added by increasing one input and output of the gate and designing the equation accordingly. This means that for fault tolerance the 3 × 3 RG-QCA is converted to 4 × 4 CRG-QCA i.e. Conservative Reversible Gate, shown in Fig. 9. Table 6 shows the parity preserving character of the CRG-QCA. The CRG-QCA design in QCA technology, shown in Fig. 10, increases the cell count by only 14 cells which is highly efficient (Table 7).

6.1 Fault Tolerant Full Adder Circuit Design

The utility of the parity preserving gates is the most important in the digital circuits where operations like addition are perfomed. The conservative nature of the gates is important for error detection in the circuits. Designing the gates with such characteristics is of utmost imporatnce in digital designs. Here the CRG-QCA is extended to show application in the design of the full adder circuit. The design of the fault tolerant adder circuit and simulation results in QCA Designer 2.0.3 are shown in Fig. 11 and the performance parameters in Table 8.

7 Discussions

A number of comparisons have been drawn to prove the efficiency of the proposed designs. Table 9 shows the percentage improvement of the optimized RG-QCA design compared to conventional majority voter based design.

Tables 10 draws the comparisons between the existing 3×3 reversible gates and proposed RG-QCA gate and it is observed that the RG-QCA gate has the least cell count and hence cell area along with highest area utilization.

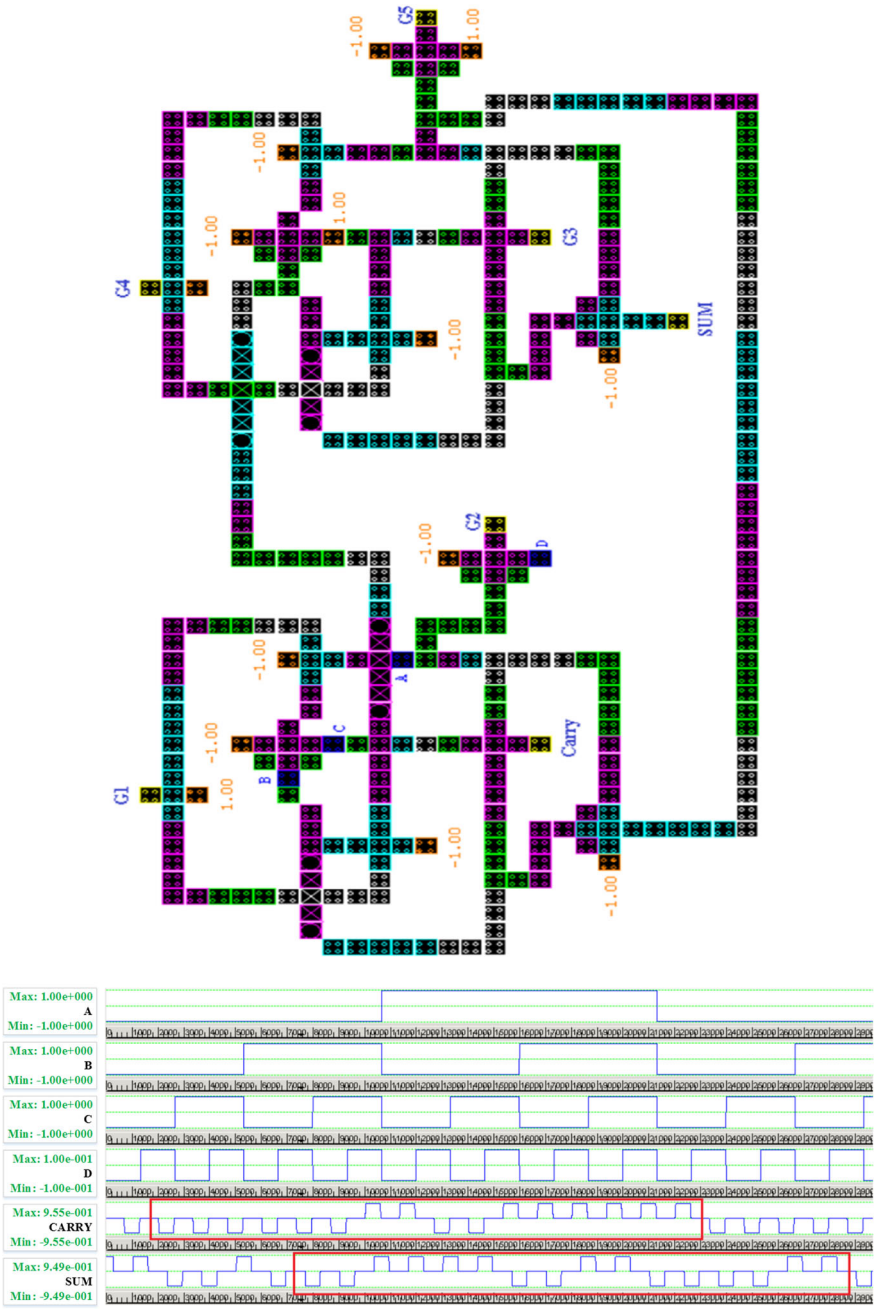

Fig. 11 QCA implementation and simulation waveforms of proposed fault tolerant full adder circuit using CRG-QCA gate

Table 8 Performance parameters of fault tolerant full adder using CRG-QCA gate

Parameters	Value
No. of cells	421
Cell area	0.1364 μm^2
Total area	0.5073 μm^2
Latency	4.75
Number of crossovers	4

Table 9 Comparison between RG-QCA using majority voter approach and optimized RG-QCA

Parameter	RG-QCA using majority voter approach	RG-QCA optimized design	%age Improvement in optimized RG-QCA
Cell count	427	143	66.51
Cell area (μm^2)	0.1383	0.04633	66.5
Total area (μm^2)	0.6065	0.149	75.43
Latency	3	1.75	41.66
Complexity	2 MLC	1 MLC	50
Area delay product	1.81	0.26	85.6

Table 10 Comparison of proposed RG-QCA gate with existing 3 × 3 reversible gates in QCA

Parameter	Fredkin gate [12]	RUG [30]	PPRG [29]	RQCA [31]	Mx-cqca [32]	R-CQCA [28]	Proposed RG-QCA
N_{MG}	6	7	6	6	5	6	4
N_{INV}	8	2	6	4	0	9	2
Cell count	246	211	171	194	218	177	143
Cell area (μm^2)	0.079	0.068	0.055	0.062	0.070	0.057	0.046
Total Area (μm^2)	0.37	0.27	0.19	0.21	0.35	0.24	0.14
Latency	4	3	3	3	-	2.25	1.75
Area delay product	1.48	0.81	0.57	0.63	-	0.54	0.245
Area usage (%)	21.35	25.18	28.94	29.52	20	23.47	32.85

Table 11 Comparison of full adder circuits using different reversible gates in QCA

Parameter	Fredkin gate [12]	Toffoli gate [15]	QCA 1 [27]	RUG [30]	PPRG [29]	RQCA [31]	Proposed RG-QCA	Proposed CRG-QCA
Gate count	5	4	3	2	3	3	2	2
Cell count	955	672	438	594	513	582	375	421
Cell area (μm^2)	0.309	0.2177	0.1419	0.1924	0.166	0.188	0.1215	0.1364
Total area (μm^2)	1.85	1.48	0.48	0.92	0.57	–	0.37	0.5073
Area usage (%)	16.7	14.7	29.56	20.91	29.12	–	32.83	26.89

Table 12 Comparison of proposed CRG-QCA gate with existing fault tolerant and reversible gates in QCA

Parameter	Fredkin gate [12]	PPRG [29]	R-CQCA [28]	Proposed CRG-QCA
Cell count	246	171	177	157
Cell area (μm^2)	0.079	0.055	0.057	0.0508
Total area (μm^2)	0.37	0.19	0.24	0.193
Area utilization (%)	21.35	28.94	23.47	26.32

Table 13 Comparison of RG-QCA and different reversible gates in implementation of 13 standard logic functions

S. No.	Function	CQCA [36]	t-QCA [31]	Toffoli [32]	Fredkin [12]	Proposed RG-QCA
1	ABC	2	2	2	2	2
2	AB	1	1	1	1	1
3	AB+BC+AC	1	1	5	5	1
4	A	1	1	1	1	1
5	A′BC+A′B′	3	8	3	3	2
6	AB+A′B′	4	1	2	2	1
7	ABC′+A′BC+A′B′C′	6	6	6	6	5
8	A′BC+AB′C+ ABC′+ABC	3	2	2	3	1
9	ABC+AB′C′	6	2	5	4	5
10	AB+B′C	3	4	3	1	3
11	AB+BC	2	2	2	2	2
12	AB+A′B′C	5	6	5	5	5
13	AB+BC+A′B′C′	6	2	5	6	5
Total		43	38	42	41	34

Table 14 Cost comparison of full adder circuits using reversible gates in QCA

Parameter	Fredkin gate [12]	RUG [30]	PPRG [29]	Toffoli [32]	Proposed RG-QCA
N_{MG}	6	7	6	4	4
N_{INV}	8	11	6	5	2
C	5	10	3	3	3
T	4	8	4	4	7
N_{RG}	5	2	3	4	2
Cost	1380	2560	522	480	378

The performance comparison of the full adder circuits designed using proposed RG-QCA and CRG-QCA gates with existing state-of-the-art designs is given in Table 11. It is seen that the proposed RG-QCA based optimized full adder has least cell count and highest area usage. Although, the area usage using CRG-QCA gate is relatively low, it is fault tolerant in nature and a 4×4 gate and still achieves lower cell count comparable to the other 3×3 gate based adder designs. Table 12 shows the efficiency of the proposed CRG-QCA with existing parity preserving gates in QCA. In addition to this, comparison of number of gates required to implement the 13 standard logic functions using RG-QCA gate and other reversible gates has been presented in Table 13 and it is observed that the proposed gate requires least number of gates to implement the functions. Finally, a comparative cost analysis, based on the cost function proposed in [29, 37], is utilized to calculate the overall cost which is a function of number of QCA gates (NG), delay/latency (T) and number of crossovers (C) and are expressed as:

$$\text{Cost} = (NG + C^m) \times T \times N_{RG} \tag{10}$$

$$NG = N_{MG}^n + N_{inv} \tag{11}$$

$$T = 4 \times N_{clk} \tag{12}$$

$$C = l \times C_{CP} \tag{13}$$

where N_{MG}, N_{inv}, N_{RG} and N_{clk} are the number of majority voter gates, number of inverters, number of reversible gates used in the design and number of clocks to get output respectively. Also, l denotes the number of number of layers in the design and is usually 1 for single layer design and 3 for multilayer design. In the proposed adder design, l is equal to 3. Since N_{MG} and C have greater effect on complexity, power and fabrication difficulty, therefore cost has a quadratic relationship with N_{MG} and C and thus $n = m = 2$ [29, 37]. It is observed from Table 14 that the overall cost is significantly reduced for the proposed

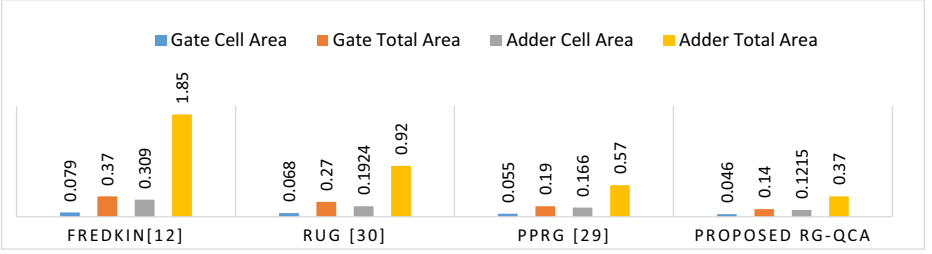

Fig. 12 Graphical comparison of area consumed (in μm^2) by various reversible 3×3 gates in QCA

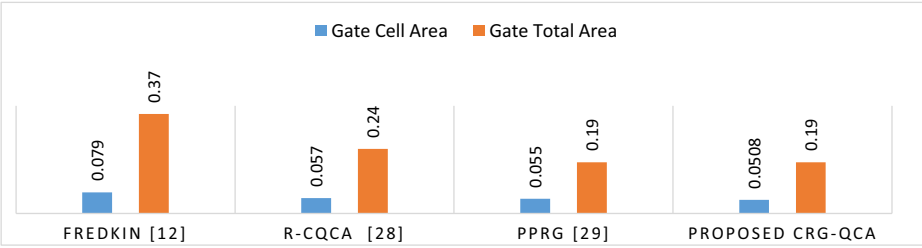

Fig. 13 Graphical comparison of area consumed (in μm^2) by various fault tolerant gates in QCA

full adder design using RG-QCA gate. The graphical area comparisons are also shown in Figs. 12 and 13. Hence, the proposed designs can be used as they show improved behavior in terms of size and complexity.

8 Conclusion

In this paper the alternatives to overcome the limitations that the CMOS technology is facing in the nano regime are discussed. The focus is on two upcoming paradigms namely, the reversible logic and the QCA nanotechnology. The basic theory and preliminaries related to both these paradigms are initially discussed followed by a detailed literature review on both reversible and irreversible circuit designs in QCA technology. The adder circuits which form the main component of maximum digital circuits are chosen as the component of interest here since the need for their efficient designs is of utmost importance. A new Reversible gate RG-QCA which has universal functionality, simplified equations and optimal QCA implementation is first proposed followed by the design of a full adder circuit using the optimal RG-QCA gate. This work also includes the development of fault tolerant designs. All the designs in this paper are based on explicit interaction of cells rather than the conventional majority voter approach. Using this approach a very high percentage improvement has been reported in all our designs. Extensive comparisons of proposed gate, full adder and the fault tolerant designs are drawn with the available designs in the literature. It is envisaged that the proposed designs outperform the existing ones in terms of almost all the QCA parametrs such as cell count, cell area, total area, latency and complexity.

Appendix A: Majority Gate Representations

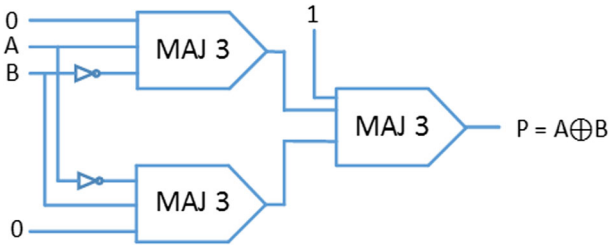

Fig. 14 Majority gate representation of output P in (3) of proposed RG-QCA gate

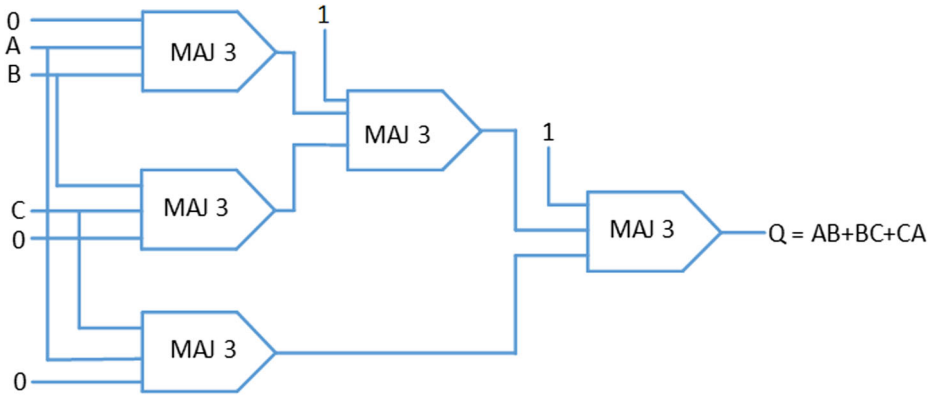

Fig. 15 Majority gate representation of output Q in (4) of proposed RG-QCA gate

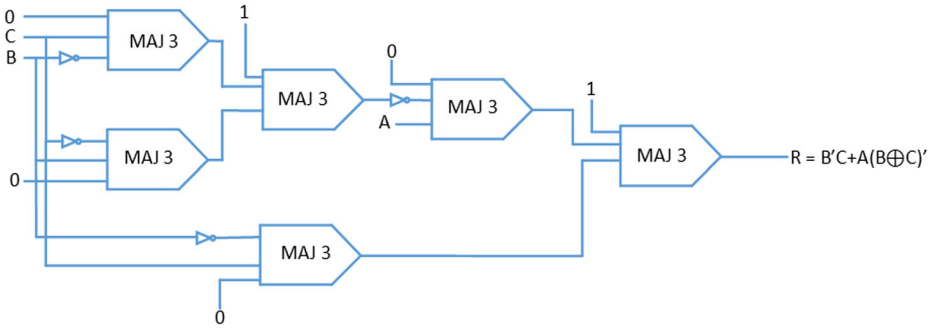

Fig. 16 Majority gate representation of output R in (5) of proposed RG-QCA gate

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