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Reversible Flip-Flops in Quantum-Dot Cellular Automata

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Abstract Quantum-dot cellular automata is a new technology to design the efficient combinational and sequential circuits at the nano-scale. This technology has many desirable advantages compared to the CMOS technology such as low power consumption, less occupation area and low latency. These features make it suitable for use in flip-flop design. In this paper, with knowing the characteristics of reversible logic, we design new structures for flip-flops. The operations of these structures are evaluated with QCADesigner Version 2.0.3 simulator. In addition, we calculate the power dissipation of these structures by QCAPro tool. The results illustrated that proposed structures are efficient compared to the previous ones.

Keywords Nanotechnology · Quantum-dot cellular automata · Reversible logic · Flip-flop

1 Introduction

Recently, studies to find the new technologies to substitute CMOS circuits have increased. Quantum–dot cellular automata (QCA) is one of these technologies for digital logic designs at nano-scale with ultra low power, high performance and least feature size [2, 3]. The basic component in QCA is quantum cell. Each quantum cell is composed of four dots and two excess electrons. These electrons can tunnel between dots due to columbic interaction and diagonally occupy corners of the cell, hence leading to two stable arrangements for quantum cell which are shown in Fig. 1. These two stable states of a quantum cell are named as cell polarizations. Polarizations -1 and $+1$ are encoded as logic "0" and "1", respectively. As shown in Fig. 2a, by placing several quantum cells side by side, a standard QCA wire can be constructed to transmit a logic value. Moreover, a QCA inverter chain can be constructed

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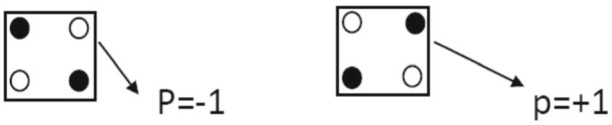


Fig. 1 Two possible polarization states in a quantum cell

exploiting 45° rotated QCA cells. This kind of wire propagates the input signal in odd cells and inversion of the input signal in even cells, as shown in Fig. 2b. Coplanar wire is achieved using these two types of wires as shown in Fig. 3 [2, 25, 26].

Clock scheme in QCA contains four phases. In the Switch phase, cell begins to polarize. In the Hold phase, barrier is kept high. In the Release phase, cells will be allowed to start going in internal polarity state. Finally, in the Relax phase, cell remains in non-polarity state [4–6]. This scheme is shown in Fig. 4.

2 QCA Main Gates

Inverter gate is one of the basic gates in QCA. The structure of this gate is shown in Fig. 5 where columbic repulsion between the corners of the parallel cells makes the polarization of the starred cell to change into the opposite polarity of the input.

The majority gate; majority voter; that is shown in Fig. 6, is the elementary gate in designing QCA based circuits. The majority gate acts as a three input logic function. Assuming that the inputs are A, B and C, the function of the majority gate is shown as (1).

$$M(A,B,C) = AB + AC + BC \tag{1}$$

If one of the input cells in the majority gate is constantly fixed to +1, only one of the other cells is required to be +1, so that the polarity in output cell is +1. In fact, it behaves like an OR gate and is represented as:

$$M(A,B,1) = AB + (A1) + (B1) = AB + A + B = A + B \tag{2}$$

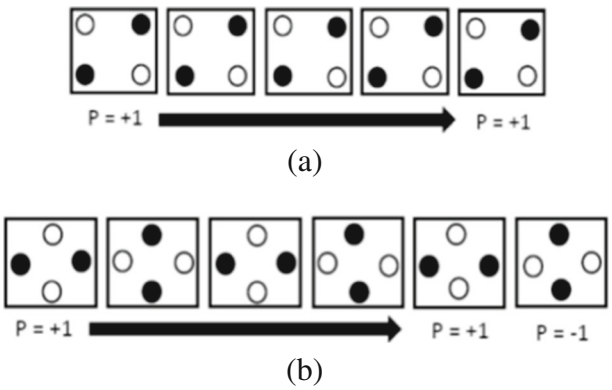


Fig. 2 **a** QCA standard wire and **b** inverter chain

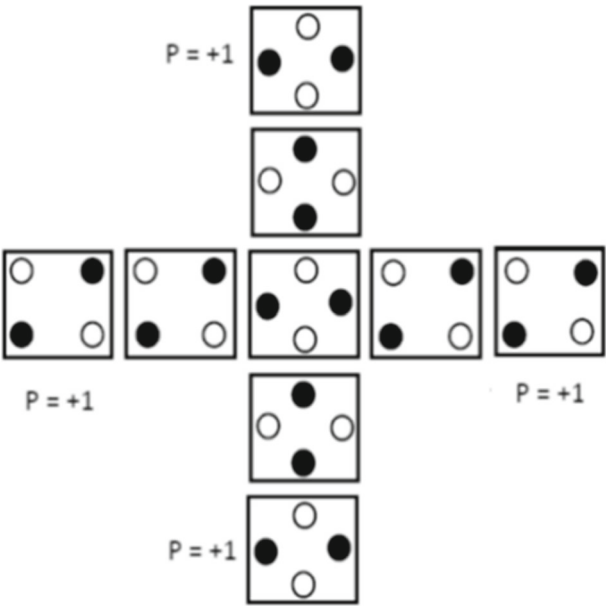


Fig. 3 Coplanar cross wiring

By fixing the polarization of one input cell to -1, it is clear that the other two inputs must be in $+1$ polarization to result in $+1$ polarization in the output cell. In fact, this structure acts like an AND gate and is demonstrated as:

$$\mathrm{M(A,B,0)} = \mathrm{AB} + (\mathrm{A0}) + (\mathrm{B0}) = \mathrm{AB} \tag{3}$$

The logic function of five-input majority gate is as:

$$\begin{aligned}\mathrm{M(A,B,C,D,E)} = {} & \mathrm{ABC} + \mathrm{ABD} + \mathrm{ABE} + \mathrm{ACD} + \mathrm{ACE} + \mathrm{ADE} + \mathrm{BCD} \\ & + \mathrm{BCE} + \mathrm{BDE} + \mathrm{CDE}\end{aligned} \tag{4}$$

The structure of this gate is shown in Fig. 7 [20–24]. By setting two of the input cells' polarization to -1 or $+1$, a three-input AND gate and also a three-input OR gate can be formed, respectively.

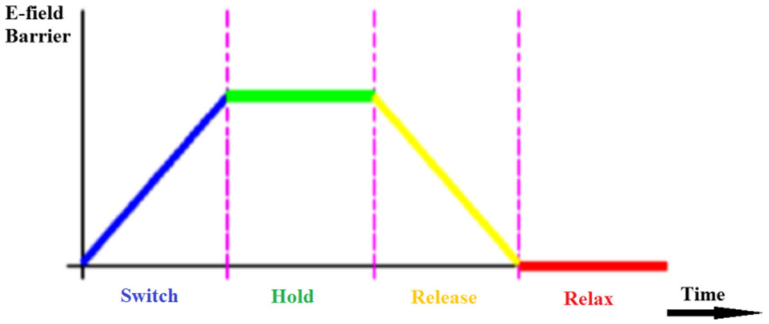


Fig. 4 Clocking scheme

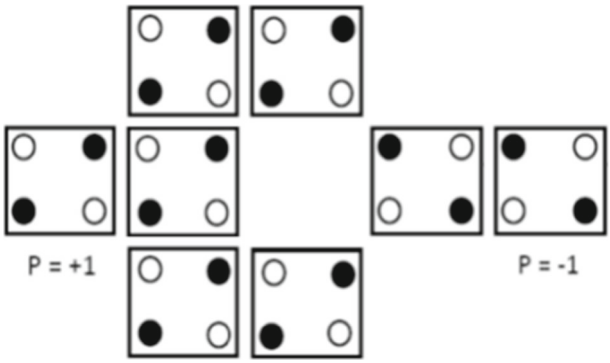


Fig. 5 QCA inverter gate

3 Reversible Logic

Reversible gates are circuits in which number of outputs is equal to the number of inputs and there is a one-to-one correspondence between the vector of inputs and outputs. It not only helps us to determine the outputs from the inputs, but also helps us to uniquely recover the inputs from the outputs [1, 7].

Reversible logic gates are those with zero loss of information. Reversible logic gate reduces the power dissipation and the latency in the manipulation of any logical operation.

4 Related Works

Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other word, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes. There are basically four main types of latches and flip-flops; SR, D, JK and T. The major differences in these flip-flops are the number of inputs and how they change state.

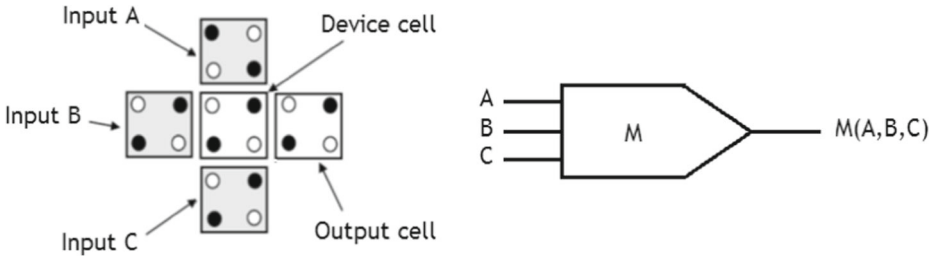


Fig. 6 QCA three-input majority gate

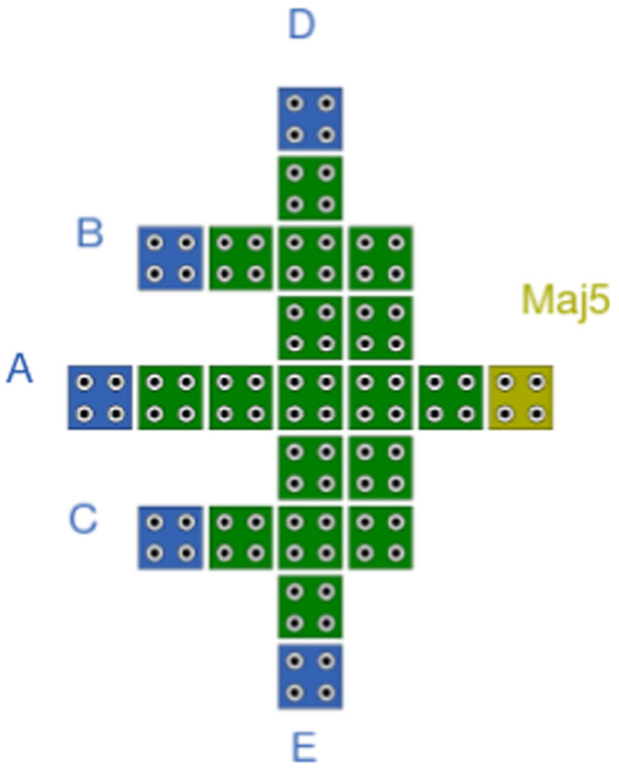


Fig. 7 QCA five-input majority gate

One of the most attractive areas in QCA technology is designing reversible circuits especially flip-flop cells. Several QCA based designs of reversible circuits and reversible flip-flops have been reported previously [8–17]. In [8] different reversible circuits are achieved based on a novel design methodology and implemented through QCA logic device. the work reported in [9], deals with the QCA realization of different latches, such as SR, JK, T and D latches based on reversible approach for molecular QCA. The single missing/additional cell based defect of those latches is also explored in [9]. In [10], several classical logic gates, such as XOR gate and XNOR gate are implemented based on QCA technology. Beside, CNOT gate and Toffoli gate also realized through QCA in [10].

A heuristic model based on cell-cell interactions is presented for ordinary flip-flop in [14]. A theoretical approach for the analysis of QCA power and energy based on density matrix formalism is presented in [15]. It has discussed the approach to analyze the energy flow within QCA architecture and also discussed about the energy relaxation time. However, it is devoid of any derivation and analysis.

A circuit of D flip-flop using seven reversible gates with eight garbage outputs is presented in [16]. Then an improved version of [16] for reversible D flip-flop which was a realization of the conventional D flip-flop sequential circuit is proposed in [17]. This work proposed a new gate; BME gate; which was used to optimize the existing reversible circuit based on the number of reversible gates used and the garbage outputs produced. The number of gates was reduced to four and the number of garbage outputs was also reduced to four.

In [13] the author interested to determine the exact clock energy required to operation of a reversible flip flop architecture consisting of N number of cells. This work optimized 4 to 2 electron two dimensional quantum-dot cellular automata logic reversible flip-flops. The presented structures in this work are shown in Fig. 8. Inputs are in the circle in the presented structures in this paper.

These structures have disadvantages such as large number of cells and large occupation area. In this paper, we propose efficient reversible structures for four flip-flops.

5 Proposed Reversible Structures

In this section, we describe the proposed architectures for the four flip-flops. The proposed architectures of the flip-flops have been shown below.

Table 1 shows the truth table of proposed reversible D flip-flop. This table contains the three input lines and also three output lines. The block structure and QCA design of proposed reversible D flip-flop are illustrated in Fig. 9a and b, respectively. This structure is useful and very simple. The logic functions of outputs of proposed D flip-flop are as:

$$C = C, O1 = D, Q(t+1) = Q(t) \tag{5}$$

Table 2 shows the truth table of proposed reversible T flip-flop. This table contains the three input lines and also three output lines. The block structure and QCA design of proposed

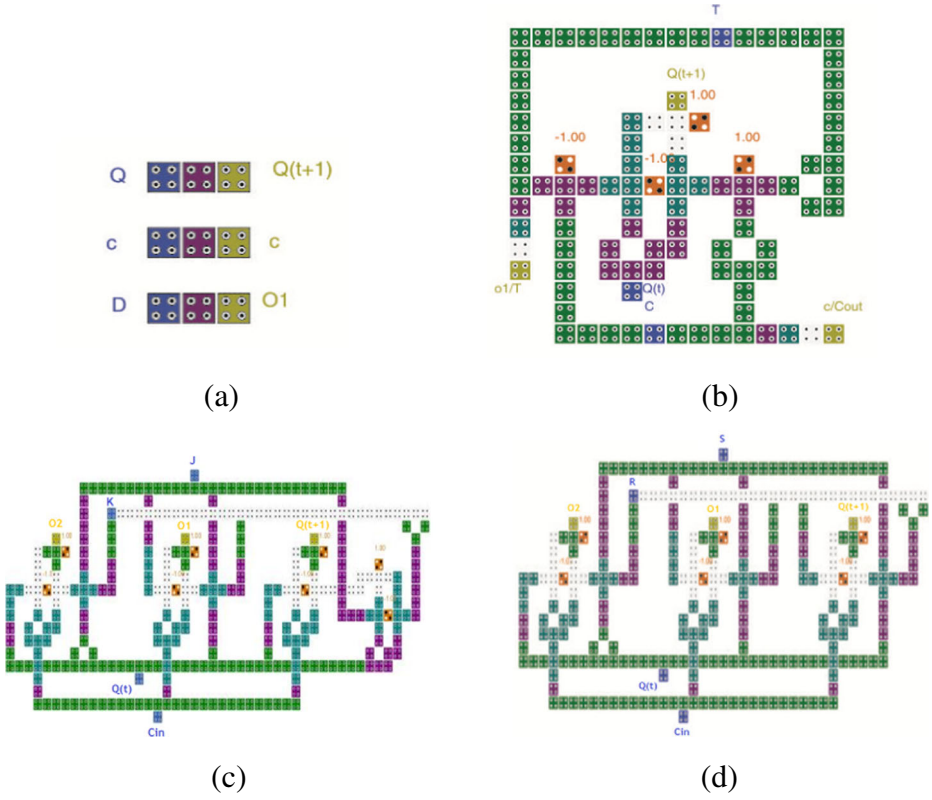


Fig. 8 Reversible flip-flops presented in [13], **a** D, **b** T, **c** JK and **d** SR

Table 1 Truth table of proposed reversible D flip-flop

Inputs			Outputs		
C	D	Q(t)	C	O_1	Q(t+1)
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

reversible T flip-flop are illustrated in Fig. 10a and b, respectively. This structure is constructed from one two-input AND gate and one two-input XOR gate. This structure is similar to the structure of Toffoli gate. The proposed reversible T flip-flop has 23 QCA cells and 0.02 μm^2 occupation area. As it can be seen in Fig. 10, this structure is implemented in a single layer. It uses only 90-degree cells and does not use the coplanar cross-wiring. The logic functions of outputs of proposed T flip-flop are as:

$$C = C, O1 = T, Q(t+1) = (CT)\ XOR\ Q(t) \tag{6}$$

The truth table of proposed JK flip-flop is shown in Table 3. This table contains the four input lines and also four output lines. The block structure and QCA design of proposed reversible JK flip-flop are illustrated in Fig. 11a and b, respectively. This design is composed of six three-input majority gates and three five-input majority gates. The proposed reversible JK flip-flop has 274 QCA cells and 0.29 μm^2 occupied area. It uses only 90-degree cells and also uses the coplanar cross-wiring. The logic functions of outputs of proposed JK flip-flop are as:

$$C = C \tag{7}$$

$$O1 = C'J + CJK + CJQ(t) + JKQ(t) + CJKQ(t) = C'J + Maj(C,J,K,Q(t),0)$$

$$O2 = C'K + CJK + CJQ'(t) + JKQ'(t) + CJKQ'(t) = C'K + Maj(C,J,K,Q'(t),0)$$

$$Q(t+1) = C'Q(t) + CJK' + CJQ(t) + JK'Q(t) + CJK'Q(t) = C'Q(t) + Maj(C,J,K', Q(t),0)$$

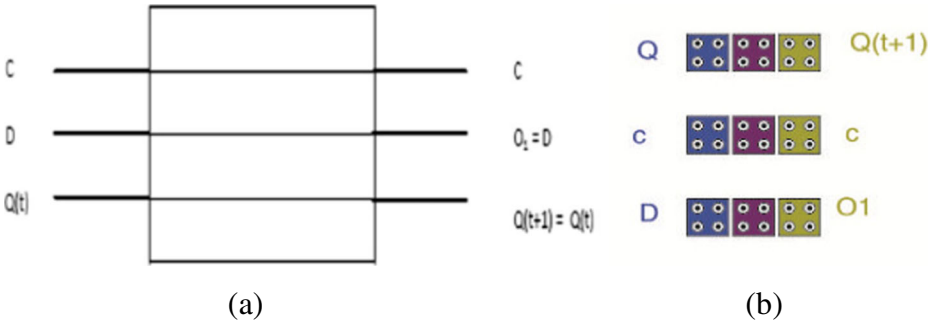


Fig. 9 Proposed reversible D flip-flop, **a** block structure and **b** QCA design

Table 2 Truth table of proposed reversible T flip-flop

Inputs			Outputs		
C	T	Q(t)	C	O_1	Q(t+1)
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

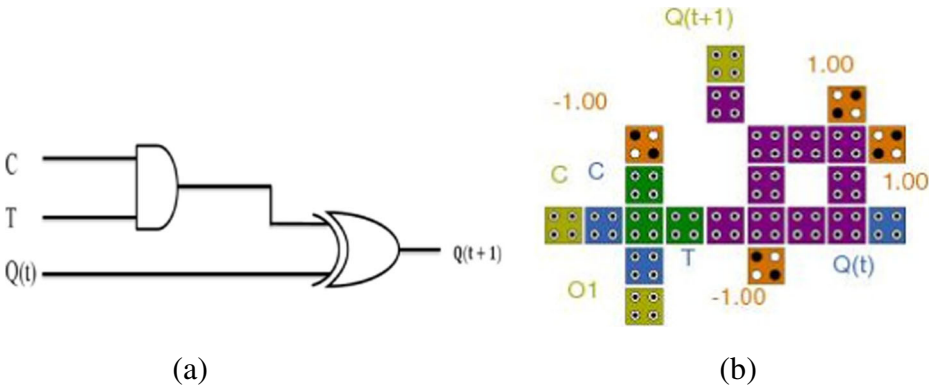
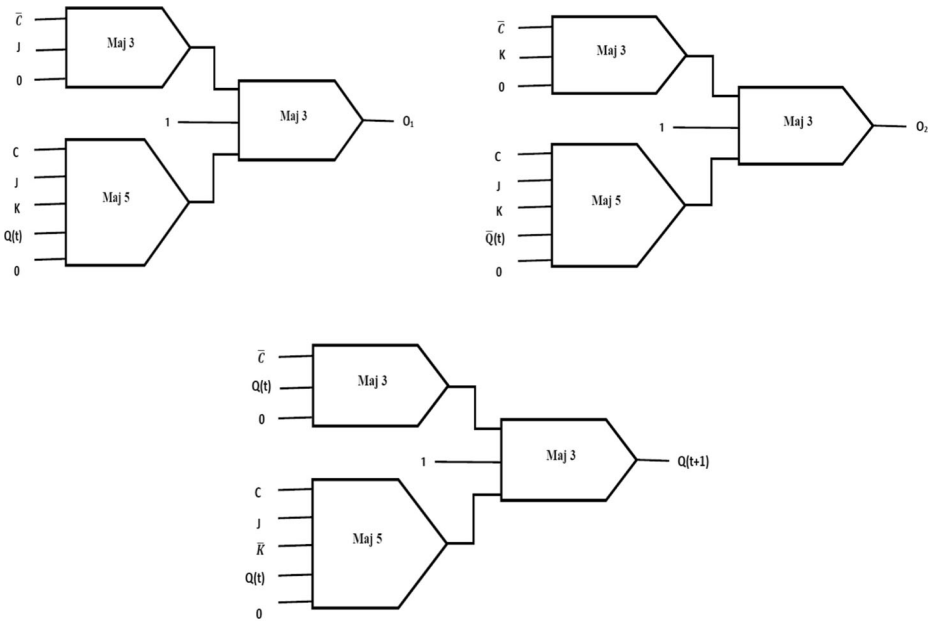


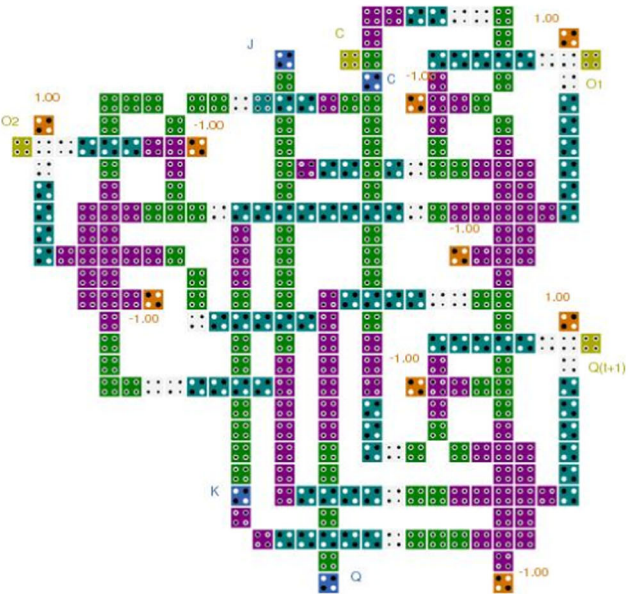
Fig. 10 Proposed reversible T flip-flop, **a** block structure and **b** QCA design

Table 3 Truth table of proposed reversible JK flip-flop

Inputs				Outputs			
C	J	K	Q(t)	C	O1	Q(t+1)	O2
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	0
1	0	1	0	1	0	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1



(a)



(b)

Fig. 11 Proposed reversible JK flip-flop, **a** block structure and **b** QCA design

Table 4 Simulation parameters

Parameter	Value
Cell size	18 nm*18 nm
Dot diameter	5 nm
Cell separation	2 nm
Simulation engine	Bistable approximation/Coherence vector
Radius of effect	65 nm
Number of samples	12800
Convergence Tolerance	0.001000
Temperature	1.000000
Relative Permittivity	12.900000
Clock High	9.800000e-022
Clock Low	3.800000e+023
Clock Shift	0.000000e+000
Clock Amplitude Factor	2.000000
Layer Separation	11.500000
Maximum iterations per sample	100
Relaxation time	1.000000e-015
Time step	1.000000e−016
Total simulation time	7.000000e−011

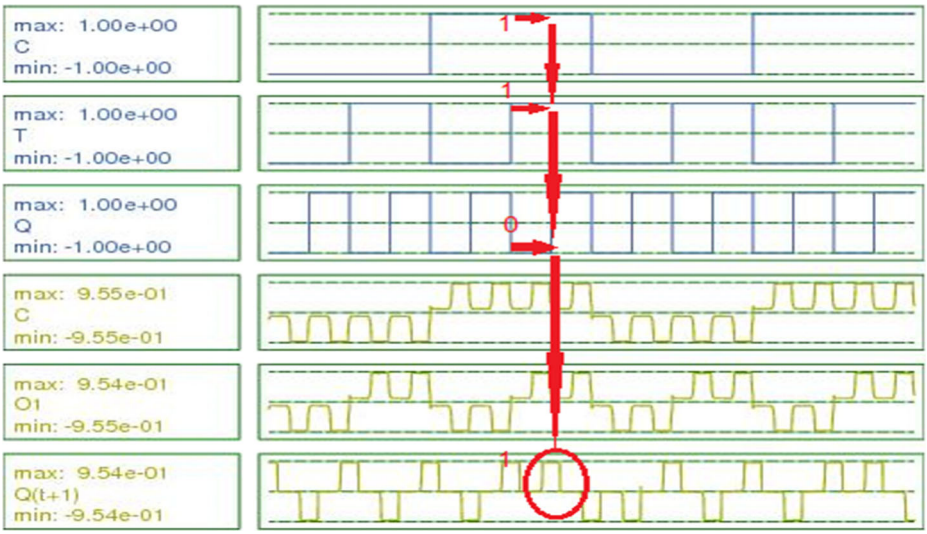


Fig. 12 Simulation result of proposed reversible T flip-flop

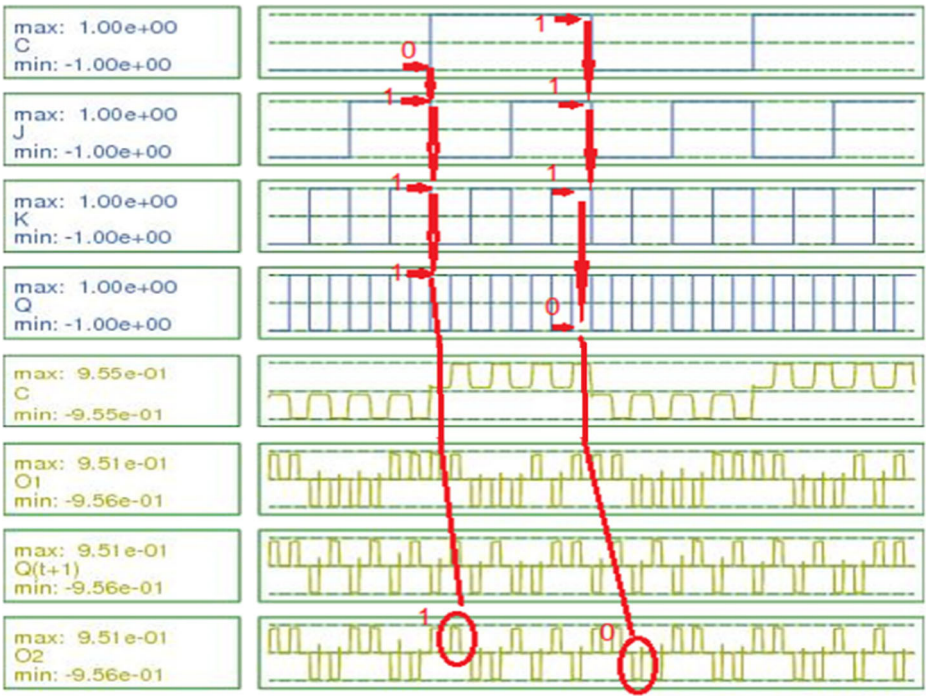


Fig. 13 Simulation result of proposed reversible JK flip-flop

We use the truth table of JK flip-flop to construct the SR flip-flop. These flip-flops have the same behavior in reversible logic in QCA.

6 Simulation Results

In this section, the proposed structures for reversible flip-flops are simulated with QCADesigner version 2.0.3 [18] that is an accurate simulation tool for QCA circuits. Simulation

Table 5 The comparative results for the flip-flops

Structure	Cell count	Area (μm^2)	Latency (clock zone)
Previous D-FF [13]	9	0.01	1
Previous T-FF [13]	98	0.10	4
Previous JK-FF [13]	329	0.39	5
Previous SR-FF [13]	296	0.34	5
Proposed D-FF	9	0.01	1
Proposed T-FF	23	0.02	2
Proposed JK-FF	274	0.29	4
Proposed SR-FF	274	0.29	4

parameters are assumed as Table 4 for all structures. Proposed structures are simulated using the Coherence Vector simulation engine and also Bistable Approximation simulation engine and similar operations were achieved from both simulation engines.

The simulation result of proposed reversible T flip-flop is illustrated in Fig. 12. This result confirms that the proposed structure works correctly and its outputs are achieved only after two clock zones.

Figure 13 Shows the simulation results of the proposed JK flip-flop. This result confirms that the expected operation is correctly achieved with one clock cycle delay.

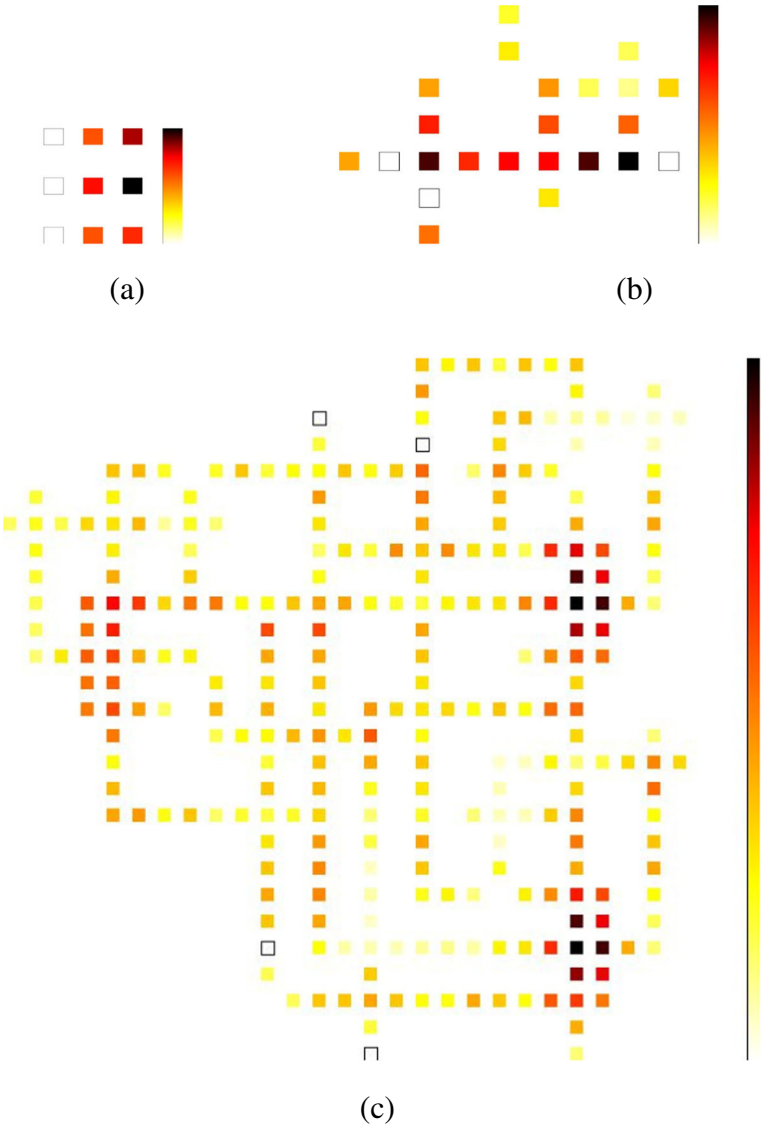


Fig. 14 Power dissipation maps for the proposed reversible flip-flops with 0.5 E_k, **a** D, **b** T and **c** JK

Table 6 Analysis of energy consumption of the flip-flops

	Avg. leakage energy dissipation (ev)			Avg. switching energy dissipation (ev)			Total energy dissipation (ev)		
Structure	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k
Previous D-FF [13]	0.00256	0.00668	0.01126	0.00702	0.00589	0.00448	0.00958	0.01257	0.01574
Previous T-FF [13]	0.02762	0.08710	0.15853	0.16208	0.14034	0.11893	0.18970	0.22744	0.27746
Previous JK-FF [13]	0.09507	0.29891	0.54304	0.55439	0.48030	0.40770	0.64946	0.77921	0.95074
Previous SR-FF [13]	0.08608	0.27101	0.49148	0.49257	0.42453	0.35875	0.57865	0.69554	0.85023
Proposed D-FF	0.00256	0.00668	0.01126	0.00702	0.00589	0.00448	0.00958	0.01257	0.01574
Proposed T-FF	0.00848	0.02211	0.03701	0.01740	0.01504	0.01292	0.02588	0.03715	0.04993
Proposed JK-FF	0.08934	0.26164	0.46076	0.42048	0.36799	0.31864	0.50982	0.62963	0.77940
Proposed SR-FF	0.08934	0.26164	0.46076	0.42048	0.36799	0.31864	0.50982	0.62963	0.77940

Table 5 shows the result of performance analysis of the proposed structures and previous structures [13] in terms of the cell count, area and Latency. As can be inferred from the values of Table 5, the proposed structures provide an improvement in cell count, latency and area compared to the other previous structures.

We use QCAPro tool [19] to evaluate the energy consumption of proposed structures. We evaluate the proposed structures under three different tunneling energy levels (0.5 *Ek*, 1 *Ek* and 1.5 *Ek*) at 2.0 K temperature. The power dissipation maps of our structures with 0.5 *Ek* are shown in Fig. 14. High power dissipating cells are indicated using thermal hotspots with darker colors. Table 6 shows the total dissipated energy divided into leakage and switching energies for the proposed structures and previous structures. It is obvious that we have achieved a consistent reduction in power dissipation.

7 Conclusion

In this paper, we proposed the reversible structures for four flip-flops in QCA. QCADesigner is used to simulate these structures. Simulation results confirmed the operations of proposed structures. The comparison demonstrated that the proposed structure is better than previous designs. We used QCAPro to evaluate the power consumption of QCA structures.

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