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Optimized 4-bit Quantum Reversible Arithmetic Logic Unit

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Abstract Reversible logic has received a great attention in the recent years due to its ability to reduce the power dissipation. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. The arithmetic logic unit (ALU) is an important part of central processing unit (CPU) as the execution unit. This paper presents a complete design of a new reversible arithmetic logic unit (ALU) that can be part of a programmable reversible computing device such as a quantum computer. The proposed ALU based on a reversible low power control unit and small performance parameters full adder named double Peres gates. The presented ALU can produce the largest number (28) of arithmetic and logic functions and have the smallest number of quantum cost and delay compared with existing designs.

Keywords Reversible gates · Quantum computing · Reversible ALU

1 Introduction

Recently, quantum computation has received a lot of attention and interest and has become one of the focal points of theoretical and experimental research. One of the important features of quantum computing is reversibility.

Landauer [1] discovered that the process of erasing information produces heat dissipation. The amount of energy dissipated per bit is equal to $K_B T \ln 2$ where K_B the Boltzmann's constant and T the absolute temperature of the environment. This result was obtained for circuits based on classical gates. Bennet [2] showed that this heat dissipation would not occur if the computation is carried out in a reversible way. He proposed

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that in order to avoid the problem of the energy dissipation, the logic circuit must be built with reversible logic gates. Theoretically we expect that in a classical computer built with reversible gates there no heat loss. A reversible gate is an n-input n-output circuit (denoted by n*n) such that there is a one to one mapping between the input and output values. In other words it is always possible to uniquely recover the input values once the output values are given. A reversible logic based on reversible circuits is a promising area of research which has extensive applications in futuristic technologies such as quantum computation, optical information processing, DNA computing etc. [3]. There are some optimization parameters which have a direct influence of the performance and the speed of the reversible circuit. These parameters include the quantum cost [4–7], the quantum delay [8–10] and the garbage outputs [11–13]. The main challenges in digital design are reducing these parameters.

The network quantum cost (QC) is the sum of the quantum cost of all gates. The quantum cost of a gate is the number of the elementary quantum operations required to realize the function given by the gate. The quantum cost is an important indicator in evaluating the performance of a reversible circuit [14]. The quantum delay (QD)is the maximum number of gates in a path from any input line to any output line.

The unused output of a reversible gate is called garbage output (GO). Garbage outputs are needed to ensure the reversibility of the gate but do not perform any useful operations. In quantum computing, information is not manipulated as in the classical way as a series of zeros and ones called bits, but as a continuous superposition of bits. Such superposition is called quantum bits or qubits.

In this paper we construct reversible arithmetic logic unit (reversible ALU) that is a part of a programmable reversible computing device such as a quantum computer by using the quantum full adder completed double Peres gate [14].

Recently, reversible ALUs, which form the essential component of a computing system, have been designed in binary as well as ternary logic as in [15–25], where cost parameters such as number of garbage outputs (GO), quantum cost (QC) and quantum delay (QD) are considered for optimization.

The goal of this article is to build a multi-functional circuit that conditionally performs one of several possible arithmetic-logical operations on two operands depending on control input data instructions.

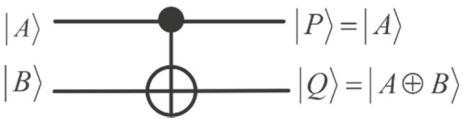
This paper is organized as follows; Section 2 gives an overview of the basic reversible logic gates used to construct adder circuit. In Section 3 we present a reversible full adder based on a double Peres gate. In Section 4 a novel design of reversible ALU is presented. The performance of this ALU and comparison with the existing ones are provided in Section 5. Finally Section 6 concludes the paper.

2 The Basic Reversible Gates

There are a number of commonly used reversible logic gates such as Feynman gate [26], Toffoli gate [27], Fredkin gate [28] and Peres gate [14]. NOT gate is represented in Fig. 1. Since it is a 1×1 gate, its quantum cost is zero.

Fig. 1 Not gate

Fig. 2 Feynman gate



In simple terms, the quantum cost of a reversible gate can be calculated by counting the number of V, $V^+$and CNOT gates used in implementing it, except in few cases. The V and V^+ quantum gates have the following properties:

$$V * V = NOT \tag{1}$$

$$V * V^+ = V^+ * V^+ = I \tag{2}$$

$$V^+ * V = NOT \tag{3}$$

A 2×2 Feynman gate, also known as controlled-NOT (1-CNOT), is depicted in Fig. 2. Its outputs are $P = A$ and $Q = A \oplus$B. The quantum representation of Feynman gate is a 2×2 gate, it has a QC and QD of 1 and 1Δ respectively Fig. 3a shows a 3×3 Toffoli gate in which two of the three outputs (P and Q) are same as two inputs (A and B). Toffoli gate can be treated as universal gate in view of the fact that it is the fundamental gate to be used to realize any 3×3 gate. Logical AND operation can be obtained through the third output by making third input C equal to zero. Implementation of Toffoli gate using quantum gates is shown in Fig. 3b, which shows that its QC and QD is equal to 5 and 5Δ respectively.

A 3×3 Fredkin gate is shown in Fig. 4a. Here the input A is passed as first output. Inputs B and C are swapped to get the second and third outputs, which is controlled by A. If $A = 0$, then the outputs are simply duplicates of the inputs; otherwise, if $A = 1$, then the two input lines (B and C) are swapped. Figure 4b shows its quantum implementation. Note that, each dotted rectangle in Fig. 4b is equivalent to a 2×2.

Feynman gate and so the quantum cost of each dotted rectangle is 1. Hence the QC of Fredkin gate consisting of two dotted rectangles, one V gate and two CNOT gates is 5 and its QD is 5Δ Fig. 5a shows the Peres gate and Fig. 5b its quantum implementation. The QC and QD of the Peres gate is 4 and 4Δ respectively, since it requires two V^+ gates, one V gate and one CNOT gate for its implementation. In the existing literature, among the 3×3 reversible gates, Peres gate has the minimum quantum cost.

If the third input C is equal to zero, this gate can be used as an AND gate through the output R in addition to the XOR function from output Q.

3 Reversible Full Adder

There have been existed a lot of reversible full adder circuits in the literature [29–33] We use Double Peres gate (DPG) [34], which is a combination of two Peres gates as shown in Fig. 6, and his truth table in Table 1. The quantum cost of this full adder is found to be 8 The full adder produces two parts, called a sum (S) and carry (C)

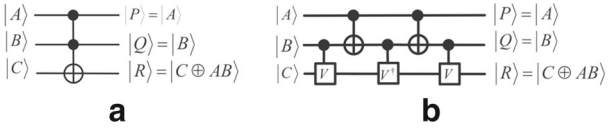


Fig. 3 (**a**) Toffoli gate and (**b**) its quantum implementation

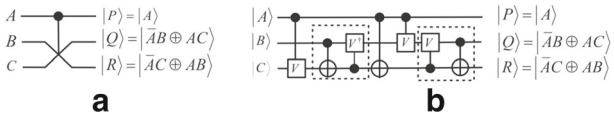


Fig. 4 (**a**) Fredkin gate and (**b**) its quantum implementation

From the truth table, for computing Sum and Carry out(C_{out}), some equations can be obtained as followed

$$C_{out} = (A \oplus B)\, C_{in} \oplus AB \tag{4}$$

$$Sum = A \oplus B \oplus C_{in} \tag{5}$$

In order to design reversible ALU, we assume the two n-bit argument as $A_i = (A_1 A_2 A_3 \ldots A_n)$ and $B_i = (B_1 B_2 B_3 \ldots B_n)$. Let C_i be the ith bit of carry and S_i be the ith bit of sum. Some equations can be obtained as followed according to (4) and (5).

$$C_i = (A_i \oplus B_i) C_{i-1} \oplus A_i B_i \tag{6}$$

$$S_i = A_i \oplus B_i \oplus C_i \tag{7}$$

A 4-bit reversible adder is cascade by the reversible full adder shown in Fig. 6. It is summarized here as Fig. 7.

4 The Design of Reversible Arithmetic Logic Unit

ALU is a data processing component, which is an important part in center process unit (CPU). Different kinds of computers have different ALUs. But all of the ALUs contain arithmetic unit and logic unit, which are the basic structures. In arithmetic operations there are add, minus, while in logical operations there are NOT, OR, AND, XOR and so on. The above operations can be realized by using reversible logic gates, through which can avoid the energy consumption.

In this paper, the multi-function ALU (see Fig. 8) based on reversible logic gates has been designed which contains the reversible control unit and the reversible full adder. The reversible control unit and the reversible full adder are cascaded and arbitrary bit reversible ALU modules can be realized by this way. The A and B inputs of the reversible control unit are altered depending on the $S_0 \ldots S_6$ values and applied as input to reversible full adder using Double Peres gates. By controlling one of the inputs to adder, various arithmetic and logic operations can be realized. The designed circuit has 7 control signals with a provision for realizing 28 arithmetic and logic operations.

The proposed reversible ALU produce in their ith result (R_i) the general expression:

$$\begin{aligned} R_i = {} & \overline{S_6}\left[(A_i \oplus S_2) \oplus (B_i \oplus S_1) \oplus S_3 C_{i-1} \oplus S_4 (A_i \oplus S_2) \oplus S_5\right] \oplus \\ & S_6\left[S_0 \oplus (A_i \oplus S_2)(B_i \oplus S_1) \oplus S_3 C_{i-1} ((A_i \oplus S_2) \oplus (B_i \oplus S_1))\right] \end{aligned} \tag{8}$$

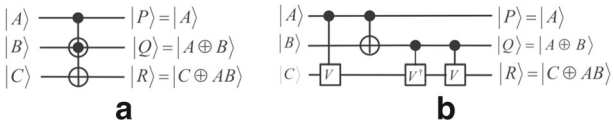


Fig. 5 (**a**) Peres gate and (**b**) its quantum implementation

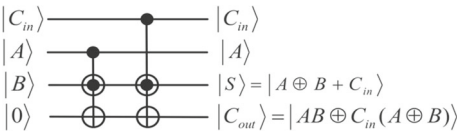


Fig. 6 Reversible full adder based on double Peres gate

4.1 Reversible Arithmetic Operations

Depending on the (8) can obtain (6) and (7). Necessary for addition operation.

When we set $S_3 = 1$ (true) and the rest of control inputs equal to 0 (false) the ALU generates the Sum as result

$$R_i = A_i \oplus B_i \oplus C_{i-1} = S_i \tag{9}$$

When we set $S_3 = S_6 = 1$ and the rest equal to zero. The ALU generates the Carry as result

$$R_i = A_i B_i \oplus C_{i-1}(A_i \oplus B_i) = C_i \tag{10}$$

For subtraction we set $S_2 = S_3 = S_5 = 1$ and the rest of control inputs equal to 0 the ALU generates the difference $A - B$ (D_i) as result

$$R_i = A_i \oplus B_i \oplus C_{i-1} = \overline{\overline{A_i} \oplus B_i \oplus C_{i-1}} = D_i \tag{11}$$

When we set $S_2 = S_3 = S_5 = S_6 = 1$ and the rest of control inputs equal to 0 the ALU generates the borrow C_i as result

$$R_i = \overline{A_i} B_i \oplus C_{i-1}\left(\overline{A_i} \oplus B_i\right) = C_i \tag{12}$$

There are other 10 arithmetic operations when we change the control inputs as summarized in Table 2

4.2 Reversible Logic operations

Depending on the (8) when we set $S_4 = S_5 = 1$ and the rest of control inputs equal to 0 the ALU generates logic operation (AND), when we set $S_0 = S_1 = S_2 = S_6 = 1$ and the rest equal to 0 the ALU produces (OR) and when we set all control inputs equal to 0 (except $S_4 = 1$) the ALU produces B (no operation), see Table 2. There are other 9 logic operation which are summarized in Table 2.

Table 1 Truth table of full adder based on double Peres gates

Inputs				Outputs			
C_{in}	A	B	0	C_{in}	A	Sum	C_{out}
0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0
0	1	0	0	0	1	1	0
1	1	0	0	1	1	0	1
0	0	1	0	0	0	1	0
1	0	1	0	1	0	0	1
0	1	1	0	0	1	0	1
1	1	1	0	1	1	1	1

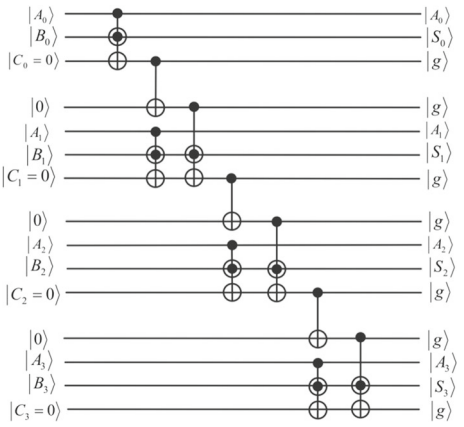


Fig. 7 Reversible 4-bit adder based on Peres gate

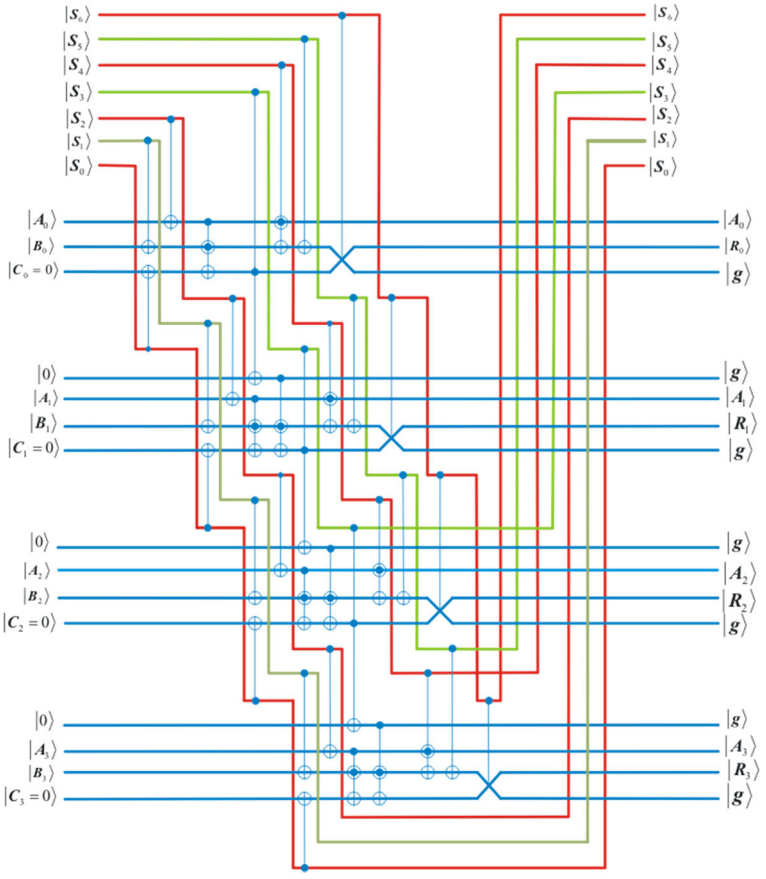


Fig. 8 The proposed reversible 4-bit ALU

Table 2 Selected operations resulting of the proposed ALU

Operations	S_0	S_1	S_2	S_3	S_4	S_5	S_6	Result
(1)	0	0	0	1	0	0	0	$A\ plus\ B$
(2)	0	0	0	1	0	1	0	$\overline{A\ plus\ B}$
(3)	0	0	1	1	0	1	0	$A\ minus\ B$
(4)	0	1	0	1	0	1	0	$B\ minus\ A$
(5)	0	1	1	1	0	1	0	$A\ plus\ B\ plus\ 1$
(6)	0	0	1	1	0	0	0	$A\ minus\ B\ minus\ 1$
(7)	0	1	0	1	0	0	0	$B\ minus\ A\ minus\ 1$
(8)	0	1	1	1	0	0	0	$\overline{A}\ plus = \overline{B}$
(9)	0	0	0	0	0	0	0	$A \oplus B$
(10)	0	0	0	0	0	1	0	$\overline{A \oplus B}$
(11)	0	0	0	0	1	0	0	B
(12)	0	0	0	0	1	1	0	$\overline{B}$
(13)	0	0	0	0	0	0	1	$A\ (AND)\ B$
(14)	0	1	0	0	0	0	1	$A\ (AND)\ \overline{B}$
(15)	0	0	1	0	0	0	1	$\overline{A}\ (AND)\ B$
(16)	0	1	1	0	0	0	1	$\overline{A}\ (AND)\ \overline{B}$
(17)	1	0	0	0	0	0	1	$\overline{A}\ (OR)\ \overline{B}$
(18)	1	0	1	0	0	0	1	$A\ (OR)\ \overline{B}$
(19)	1	1	0	0	0	0	1	$\overline{A}\ (OR)\ B$
(20)	1	1	1	0	0	0	1	$A\ (OR)\ B$
(21)	0	0	0	1	0	0	1	C_i of operations (1,2)
(22)	1	0	0	1	0	0	1	$\overline{C_i}$ of operations (1,2)
(23)	0	0	1	1	0	0	1	C_i of operations (3,4)
(24)	1	0	1	1	0	0	1	$\overline{C_i}$ of operations (3,4)
(25)	0	1	0	1	0	0	1	C_i of operations (5,6)
(26)	1	1	0	1	0	0	1	$\overline{C_i}$ of operations (5,6)
(27)	0	1	1	1	0	0	1	C_i of operations (7,8)
(28)	1	1	1	1	0	0	1	$\overline{C_i}$ of operations (7,8)

5 The Performance Analysis of the Proposed Reversible 4-bit ALU

A 4-bit reversible arithmetic logic unit was presented in [17] and it is based on the Van Rentergem adder. This 4-bit ALU produced 10 operations, having a QC of 78, QD of 57Δ and GO of 0. Another design of ALU was presented in [25] which can produce 19 operations is better than [18] but the 4-bit ALU requires at least the QC of 120, QD of 65Δ and GO of 18. In [35] three designs of 1-bit reversible ALU are presented. We choose for the sake of comparison the design 2 because it has the best results. Depending of 1-bit ALU results we can conclude that the 4-bit of [35] produces 10 operations with the number of QC, QD and GO are 48, 48Δ and 0 respectively.

The proposed design can produce 28 operations and requires at least QC, QD and GO of 95, 40Δ and 7 respectively. These results are summarized in Table 3.

Table 3 Comparative results of different reversible 4-bit ALU

Parameters / designs	Quantum cost	Quantum delay	Quantum garbage	Number of operations
Ref [18]	78	57	0	10
Ref [25]	120	65	6	18
Ref [35] Design 2	48	48	0	10
Ref [20]	116	116	32	12
Ref [17]	48	48	8	6
Ref [24]	108	60	44	12
Proposed design	95	40	7	28

In order to compare this work with the previous ones we must select the points of comparison. The first point is the number of operations of the design; this number must be big compared to existing design The second point is the optimization of the circuit parameters QC, QD and GO which have to be low compared to the previous designs. To achieve both of the two points we introduce the improvement factor (If) which is defined as follows:

$$If = \frac{number\ of\ operations}{Q\ cost + Q\ delay + Q\ garbage} \tag{13}$$

The design 4-bit ALU in [18, 20, 23, 25, 35] and [24] has the If equal to 0.074, 0.094, 0.104, 0.045, 0.057 and 0.056 respectively. The proposed design has the If equal to 0.197. Hence the percentages of improvement of the proposed design over [18, 20, 23, 25, 35] and [24] are 166, 109, 89, 338, 245 and 252% respectively. The results are summarized in Table 4.

For more explanation of 4 bit reversible ALU given by Fig. 8 we present a new figure (Fig. 9) where we depict one primary circuit of 1 bit (for example $i = 2$) with the explicit output for each step of calculation.

Table 4 Improvement percentages of the proposed design over existing designs

Designs / improvements	Ref [18]	Ref [25]	Ref [35] Design2	Ref [20]	Ref [17]	Ref [24]	Proposed design
Improvement factor If	0.074	0.094	0.104	0.045	0.57	0.056	0.197
% improvement of proposed design over the one cited in Ref.	166%	109%	89%	338%	245%	252%	

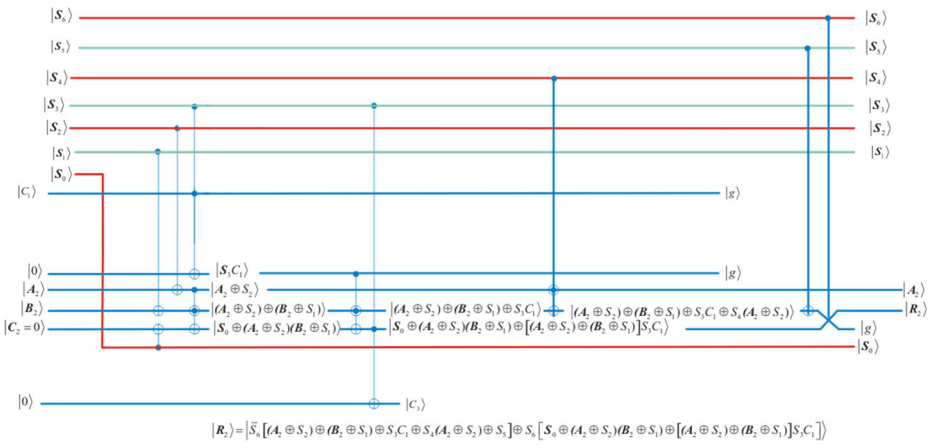


Fig. 9 The proposed 1-bit ALU ($exemple\ i = 2$)

6 Conclusion

This work presents the complete design of a 4-bit reversible arithmetic logic unit (ALU) that can be part of a programmable reversible computing device such quantum computer. We provide explicit construction of this quantum ALU that performs various arithmetic and logic operations such as addition, subtraction, AND, NAND, OR, NOR, XOR, NOP, Negation. This ALU is designed using double Peres adder and can perform up to 28 logic and arithmetic operations

We have compared the proposed design with the existing designs in terms of the quantum cost, quantum delay, garbage outputs and the number of operations.

The proposed ALU could handle more operations and has better performance in terms of quantum delay, quantum cost and garbage outputs as compared to some existing designs.

The implementation of the proposed ALU design favors low delay and high logical calculation output, which are desirable for realization of a reversible central processing unit.

For a complete realization of reversible computer architecture with the help of the proposed design, more fundamental elements must be designed. These include a reversible control unit and a new approach to reversible memory.

References

1. Landauer, R.: Irreversibility and heat generation in the computing process. IBM J. Res. Dev. **5**(3), 183–191 (1961)
2. Bennett, C.H.: Logical reversibility of computation. IBM J. Res. Dev. **17**, 525–532 (1973)
3. Nielsen, M., Chuang, I.L.: Quantum computation and quantum information. Cambridge University Press, Cambridge (2000)
4. Grobe, D., Wille, R., Dueck, G.W., Drechsler, R.: Exact synthesis of elementary quantum gate circuits for reversible functions with don't cares. In: 38th International Symposium on Multiple Valued Logic, 2008. ISMVL 2008, pp. 214–219. IEEE (2008)

5. Weste, N.H.E., Harris, D.: CMOS VLSI Design, A Circuits And Systems Perspective. Published by Person Education, 3rd edn., pp. 715–738. Boston, Addison Wesley (2005)
6. Wille, R., Drechsler, R.: Towards a Design Flow for Reversible Logic. Springer, Dordrecht, Heidelberg (2010)
7. Hung, W.N.N., Song, X., Yang, G., Yang, J., Perkowski, M.: Quantum logic synthesis by symbolic reachability analysis. In: Proceedings of the 41st Annual Design Automation Conference, pp. 838–841. ACM (2004)
8. Arabzadeh, M., Saheb Zamani, M., Sedighi, M., Saeedi, M.: Depth-optimized reversible circuit synthesis. Quantum Inf. Process 1–23 (2012)
9. Arabzadeh, M., Zamani, M., Sedighi, M., Saeedi, M.: Logical-depth-oriented reversible logic synthesis. In: International Workshop on Logic and Synthesis (2011)
10. Amy, M., Maslov, D., Mosca, M., Roetteler, M.: A meet-in-the-middle algorithm for fast synthesis of depth-optimal quantum circuits. arXiv: 1206.0758 (2012)
11. Kerntopf, P., Perkowski, M.A., Khan, M.H.A.: On universality of general reversible multiple valued logic gates. In: Proceedings of the 34th IEEE International Symposium on Multiple Valued Logic, pp. 68–73 (2004)
12. Smolin, J.A., Divincenzo, D.P.: Five two-bit quantum gates are sufficient to implement the quantum Fredkin gate. Phys. Rev. A **53**, 2855–2856 (1996)
13. Maslov, D., Dueck, G.W.: Reversible cascades with minimal garbage. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **23**(11), 1497–1509 (2004)
14. Peres, A.: Reversible logic and quantum computers. Phys. Rev. A **32**, 3266–3276 (1985)
15. Oskin, M., Chong, F.T., Chuang, I.L.: A practical architecture for reliable quantum computers. Computer **35**, 79–87 (2002)
16. Morrison, M.A.: Design of a reversible ALU based on novel reversible logic structures. PhD thesis, Graduate School Theses and Dissertations, University of South Florida (2012)
17. Morrison, M., Ranganathan, N.: Design of a reversible ALU based on novel programmable reversible logic gate structures. In: 2011 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp.126–131 (2011)
18. Thomsen, M.K., Glück, R., Axelsen, H.B.: Reversible arithmetic logic unit for quantum arithmetic. J. Phys. A: Math. Theor. **43**(38), 382002 (2010)
19. Safari, P., Haghparast, M., Azari, A., Branch, A.: A design of fault tolerant reversible arithmetic logic unit. Life Science J. **3**, 9 (2012)
20. Dixit, A., Kapse, V.: Arithmetic & logic unit (ALU) design using reversible control unit. Int. J. Eng. Innov. Technol. (IJEIT) **1**(6), 55–60 (2012). ISSN:2277-3754
21. Syamala, Y., Tilak, A.V.N.: Reversible arithmetic logic unit. In: 2011 3rd International Conference on Electronics Computer Technology (ICECT), vol. 5. IEEE (2011)
22. Morrison, M., Lewandowski, M., Meana, R., Ranganathan, N.: Design of a novel reversible ALU using an enhanced carry look-ahead adder. In: 2011 11Th IEEE Conference on Nanotechnology (IEEE-NANO), pp. 1436–1440. IEEE (2011)
23. Guan, Z., Li, W., Ding, W., Hang, Y., Ni, L.: An arithmetic logic unit design based on reversible logic gates. In: 2011 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing (Pacrim), pp. 925–931. IEEE (2011)
24. Mamatag, S., Das, B., Rahaman, A.: An optimized realization of ALU for 12-operations by using a control unit of reversible gates. Int. J. Adv. Res. Comput. Sci. Softw. Eng. **4**(1), 496–502 (2014). ISSN: 2277 128X A
25. Zhou, R., Li, Y., Zhang, M., Hu, B.: Novel design for reversible arithmetic logic unit. Int. J. Theor. Phys. 1–15 (2014)
26. Feynman, R.: Quantum mechanical computers. Optics, News **11**, 11–20 (1985)
27. Toffoli, T.: Reversible computing. Technical Memo MIT/LCS/TM-151, MIT Laboratory for Computer Science (February) (1980)
28. Fredkin, E., Toffoli. T.: Conservative logic. Int. J. Theor. Phys. **21**, 219–253 (1982)
29. Babu, H.M.H., Islam, M.R., Chowdhury, A.R., Chowdhury, S.M.A.: Reversible logic synthesis for minimization of full-adder circuit. In: IEEE Conference on Digital and System Design, pp. 50 54 (2003)
30. Thapliyal, H., Srinivas, M.B.: A novel reversible TSG gate and its application for designing reversible carry look ahead adder and other adder architectures. In: 10th Asia-Pacific Computer Systems Architecture Conference (2005)
31. Zhou, R.G., Li, Y.C., Zhang, M.Q.: Novel designs for fault tolerant reversible binary coded decimal adders. In: International Journal of Electronics, pp. 1–21 (Ahead-Of-Print) (2013)
32. Krishnaveni, D., Geetha, P.M.: A novel design of reversible serial and parallel adder/subtractor. Int. J. Eng. Sci. Technol. (IJEST) **3**(3), 2280–2288 (2010)

33. Biswas, A.K., Hasan, Md.M., Chowdhury, A.R.: Hafiz Md.Hasan Babu, efficient approaches for designing reversible binary coded decimal adders. Microelectron. J. **39**, 1693–1703 (2008)
34. Bhagyalakshmi, H.R., Venkatesha, M.K.: An improved design of a multiplier using reversible logic gates. Int. J. Eng. Sci. Technol. **2**(8), 3838–3845 (2010)
35. Majid, H., Bolhassani, A.: Optimization approaches for designing quantum reversible arithmetic logic unit. Int. J. Theor. Phys. **55**, 1423–1437 (2016)