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Novel Designs of Quantum Reversible Counters

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Abstract Reversible logic, as an interesting and important issue, has been widely used in designing combinational and sequential circuits for low-power and high-speed computation. Though a significant number of works have been done on reversible combinational logic, the realization of reversible sequential circuit is still at premature stage. Reversible counter is not only an important part of the sequential circuit but also an essential part of the quantum circuit system. In this paper, we designed two kinds of novel reversible counters. In order to construct counter, the innovative reversible T Flip-flop Gate (TFG), T Flip-flop block (T_FF) and JK flip-flop block (JK_FF) are proposed. Based on the above blocks and some existing reversible gates, the 4-bit binary-coded decimal (BCD) counter and controlled Up/Down synchronous counter are designed. With the help of Verilog hardware description language (Verilog HDL), these counters above have been modeled and confirmed. According to the simulation results, our circuits' logic structures are validated. Compared to the existing ones in terms of quantum cost (QC), delay (DL) and garbage outputs (GBO), it can be concluded that our designs perform better than the others. There is no doubt that they can be used as a kind of important storage components to be applied in future low-power computing systems.

Keywords Reversible logic · TFG gate · BCD counter · Controlled up/down synchronous counter · Simulation

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1 Introduction

Reversible logic is a burgeoning technology which provides logic design platform for low-power and high-speed computing. In 1973, Bennett [1] showed that no energy would be dissipated in a system only if the system were able to return to its initial state from its final state regardless of what happened in the process. It made clear that, in order to prevent power from dissipating, the circuit must be built using reversible logic gate. Reversible logic is the research foundation for many disciplines. It has shown a great potential in many applications such as quantum computing, optical computing, bioinformatics, deoxyribonucleic acid(DNA) computing, nanotechnology, low-power complementary metal oxide semiconductor (CMOS) design, quantum-dot cellular automata, information security and digital signal processing, etc. [2–4].

A large amount of research work is mainly concentrated in the design of reversible combinational circuits [5–7], but the reversible sequential circuits such as flip-flops and counters are reported less [8]. Researchers [9–13] put forward the realization of various types of latches, flip-flops and other related design. These studies have opened a door for the design of reversible sequential circuits such as counters. The authors [14–17] have successfully designed a number of reversible counters. All of these works show that there is a scope for the design and realization of large sequential circuits like counter.

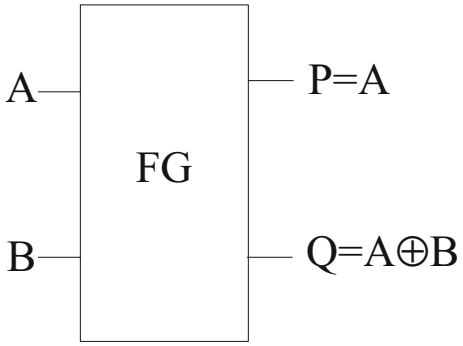
The counter is one of the most important parts in a digital system. It is mainly used for frequency division, timer and sequence generation, etc. The counter is an essential part of any digital instrument or digital system. In digital circuits, the operation of recording the number of clock pulses (CP) is called counting, and the electronic circuit for implementing the counting operation is called counter. The output of the counter is not only related to the current input, but also related to the original state of system, and the realization of quantum reversible circuit feedback is difficult in itself, for which the design of quantum reversible counter becomes more difficult. At present, most of designs are binary reversible counters which only can count up or count down. Moreover, reversible decimal counters widely used in many fields are rarely designed. To make up for their deficiencies, the BCD decimal counter and controlled Up/Down synchronous counter are designed using reversible gates.

In reversible circuits, the important cost metrics are the quantum cost (QC), the delay (DL), and the number of garbage outputs (GBO). We introduce novel design methods of counters based on the above metrics.

There are two kinds of available counter: ripple counter and synchronous counter. A ripple counter is an asynchronous sequential circuit, and the output of a flip-flop is used to trigger other flip-flops. However, in a synchronous counter, all flip-flops receive a common input clock signal [18]. This study proposed innovative TFG gate and two novel designs of counters including BCD ripple counter and controlled Up/Down synchronous counter. The performance of designs is compared with existing ones. Our proposed circuits adopt the Verilog HDL modeling. All of the code is executed on the Xilinx integrated software environment (ISE) Design Suite 12.4. The simulation results show that the logical structures of the designs are completely correct.

The rest of the paper is organized as follows. Section 2 is the brief review of some quantum reversible gates required in proposed designs. The novel reversible gates, flip-flop block and their equivalent quantum implementation are also presented. Section 3 presents the innovative reversible design methods for 4-bit BCD ripple counter and controlled Up/Down

Fig. 1 FG gate



synchronous counter, and performances of the proposed designs are evaluated. Simulation experimental results are in Section 4. The final concludes the whole paper and puts forward the future work.

2 Quantum Reversible Gates

2.1 Existing Quantum Reversible Gates

Currently, there are a lot of reversible logic gates. We now review some of the quantum reversible gates used in the paper. As is depicted in below figures, various gates have been shown, namely 2 × 2 Feynman Gate (FG) [19], 3 × 3 Feynman Double Gate (F2G) [20], 3 × 3 Toffoli Gate (TG) [21], 3 × 3 Peres Gate (PG) [22], 3 × 3 Modified Fredkin Gate (MFRG) [23], and 3 × 3 Modified Toffoli Gate (MTG) [24]. The QC of above gates is 1, 2, 5, 4, 4 and 5 from Figs. 1, 2, 3, 4, 5 and 6, while the DL of these ones is 1Δ, 2Δ, 5Δ, 4Δ, 4Δ, and 5.Δ correspondingly (the delay of each 1 × 1 or 2 × 2 reversible gate is a unit of delay(DL), which is denoted as 1Δ).

2.2 Novel Quantum Reversible Gate

2.2.1 Reversible T Flip-Flop Gate

In Fig. 7, a 4 × 4 quantum reversible gate called T flip-flop gate (TFG) is proposed, and its equivalent quantum implementation is depicted in Fig. 8. The input vector is I(A,B,C,D)

Fig. 2 F2G gate

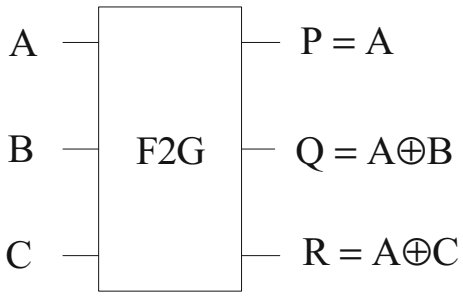


Fig. 3 TG gate

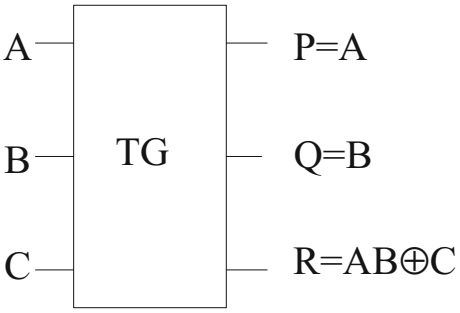


Fig. 4 PG gate

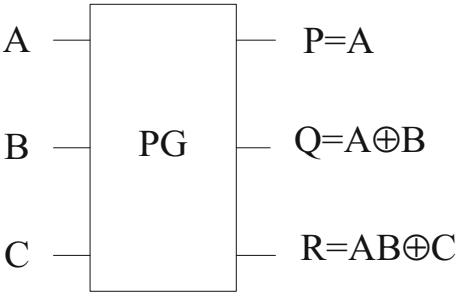


Fig. 5 MFRG gate

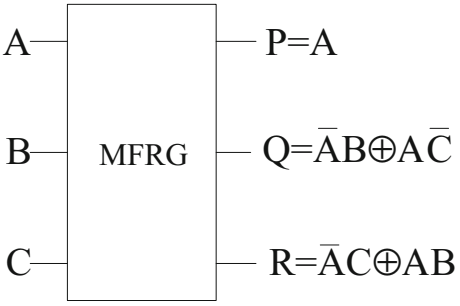


Fig. 6 MTG gate

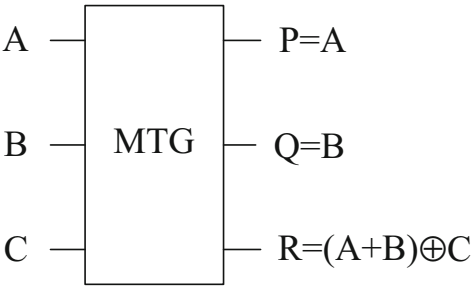
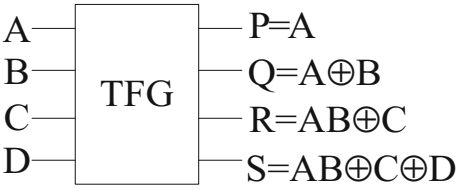


Fig. 7 Function diagram of the TFG gate



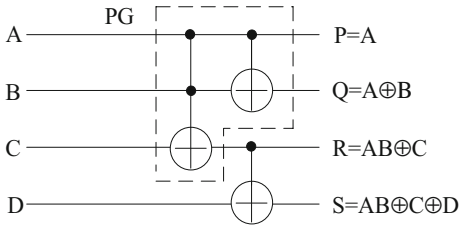


Fig. 8 Equivalent quantum implementation of the TFG gate

and the output vector is O(P,Q,R,S).The output is denoted as $P = A$, $Q = A \oplus B$, $R = AB \oplus C$, $S = AB \oplus C \oplus D$. The optimized QC of a TFG is 5 and the DL is 5Δ. The corresponding truth table of the TFG is illustrated in Table 1. From Table 1, it can be confirmed that the input pattern corresponding to a particular output pattern will be uniquely determined. The TFG can achieve the function of T flip-flop.

2.2.2 Reversible Flip-Flop Block

The block of T flip-flop (T_FF) designed by TFG gate and FG gate is shown in Fig. 9. The optimized QC and DL of a T flip-flop is 6 and 6Δ. An integrated block of JK flip-flop (JK_FF) is achieved by cascading the MFRG and F2G gate in Fig. 10. It can complete JK flip-flop functions independently. The optimized QC and DL of a JK_FF is 10 and 10Δ, respectively. T_FF and JK_FF are all important components of counters.

Table 1 Truth table of the TFG gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	1
1	1	0	1	1	0	1	0
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	1

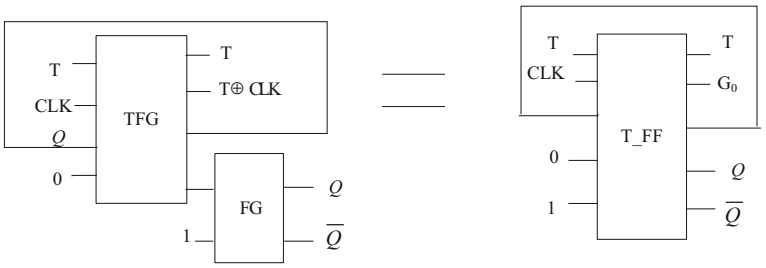


Fig. 9 Block of reversible T Flip-flop

3 Quantum Reversible Counter

3.1 Convention Counter

Ripple counter and synchronous counter are two kinds of traditional counters. BCD ripple counter follows a sequence of ten states and return to 0 after the count of 9. Such a counter must have at least four flip-flops to stand for each decimal digit. Convention BCD ripple counter is shown as Fig. 11 [18]. Synchronous counters, in which clock pulses are applied to the inputs of all flip-flops, are different from ripple counters. A common clock triggers all flip-flops simultaneously rather than one at a time in succession as in a ripple counter. In Fig. 12, convention 4-bit synchronous Up/Down binary counter is illustrated [18]. It consists of an Up control input and a Down control input. When the Up input is 1, the circuit counts up. When the Up input is 0 and the Down input is 1, the circuit counts down.

3.2 Quantum Reversible Counter

3.2.1 4-bit BCD Ripple Counter

(1) Circuit Structure

In Fig. 13, the novel reversible design of 4-bit BCD ripple counter is presented. It counts from 0000 to 1001 and back to 0000 in binary coded decimal. In Fig. 14, the state diagram of a decimal BCD ripper counter is depicted. Since the return to 0 after a count of 9, a BCD ripper counter has an irregular pattern as in a straight binary count. To achieve the derivation of the circuit for a BCD ripple counter, it should undergo a sequential circuit design procedure.

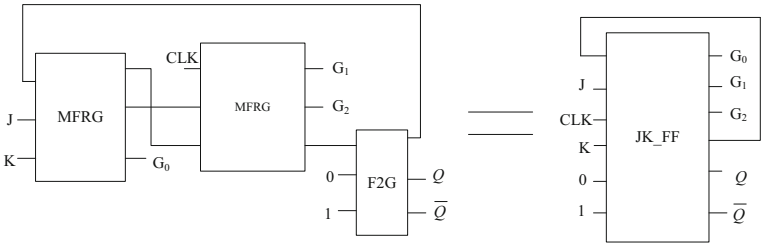


Fig. 10 Block of reversible JK flip-flop

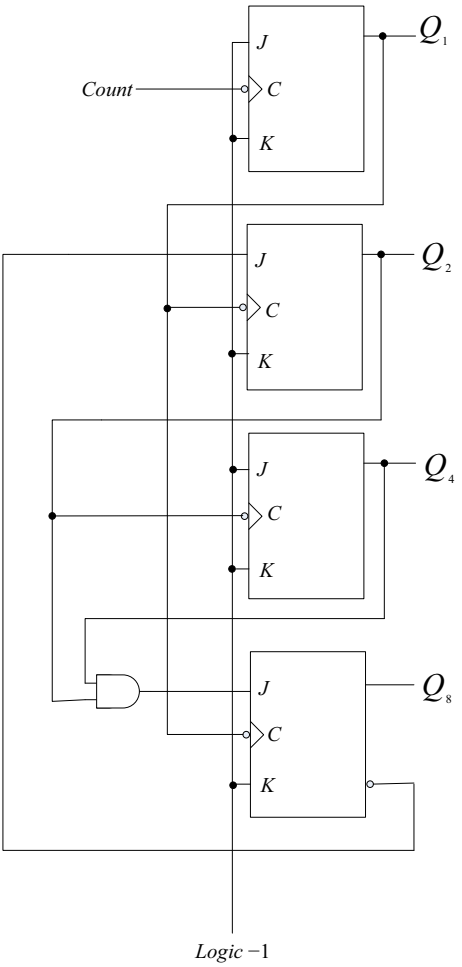


Fig. 11 4-bit BCD ripple counter

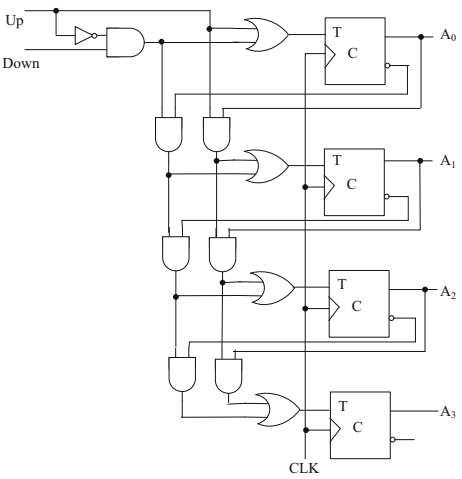


Fig. 12 4-bit Up/Down binary counter

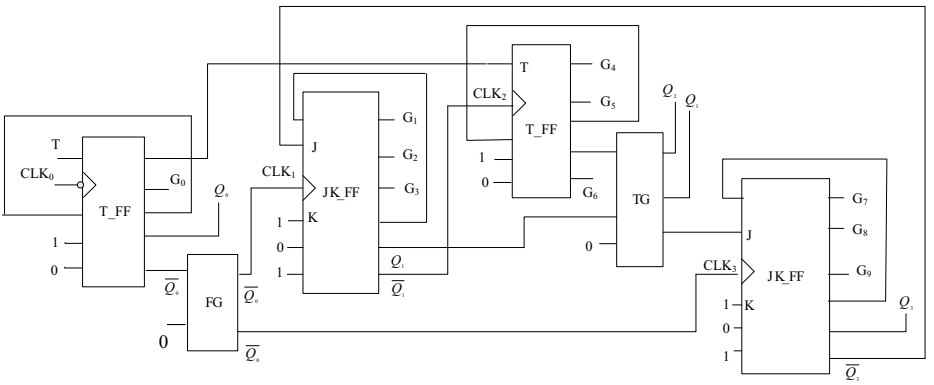


Fig. 13 Reversible 4-bit BCD ripple counter

Fig. 14 State diagram of a decimal BCD counter

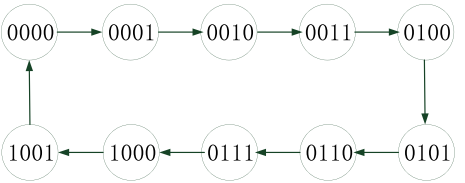


Table 2 Performance of reversible 4-bit BCD ripple counter

	QC	DL	CI	GBO
Proposed circuit	38	38Δ	12	10

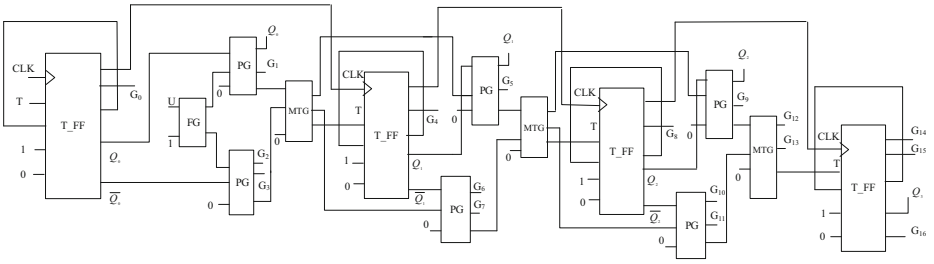


Fig. 15 Reversible 4-bit controlled Up/Down synchronous counter

Table 3 Performance comparison of different type of reversible 4-bit Up/Down synchronous counters

	QC	DL	CI	GBO
Proposed circuit	64	64Δ	18	17
Existing circuit [15]	96	96Δ	23	20
Improvement with respect to [15]	34.33 %	34.33 %	21.74 %	15 %

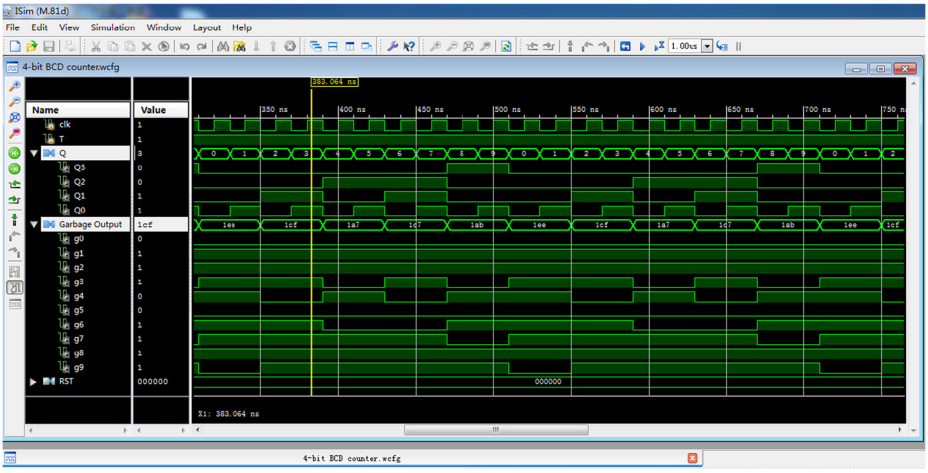


Fig. 16 Functional simulation of reversible 4-bit BCD ripple counter

Figure 13 consists of some reversible flip-flop blocks, such as T_FF and JK_FF, as well as some reversible gates like FG and TG. The T_FF and JK_FF blocks are responsible for outputting Q and $\overline{Q}$ by trigging with negative clock pulse, while the FG and TG gate are used to produce the copy of the Q or $\overline{Q}$. And the TG gate is also used to realize the AND function.

(2) Performance Evaluation

In synthesis of quantum reversible circuits, it is an important issue to evaluate the designed circuits. In Table 2, the performance of our reversible BCD ripple counter is shown.

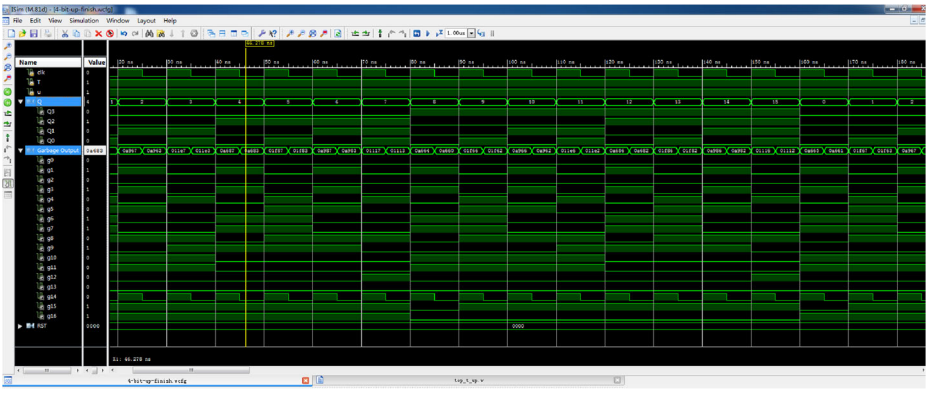


Fig. 17 Functional simulation of reversible 4-bit Up synchronous counter (U=1)

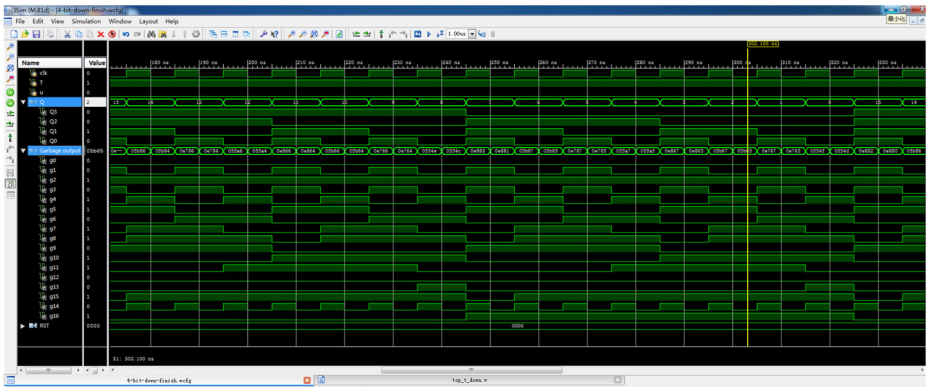


Fig. 18 Functional simulation of reversible 4-bit Down synchronous counter (U = 0)

3.2.2 4-bit Synchronous Up/Down Counter

(1) Circuit Structure

The reversible design of 4-bit controlled Up/Down synchronous counter is shown in Fig. 15. The proposed T_FF block is used to realize function of the T flip-flops. To perform AND and OR operations, the PG gate and the MTG gate are applied. The U is the control input. The FG gate is used to produce U and the NOT of U.

The Up/Down operation of this reversible counter is controlled by the control input U. The T_FF blocks are responsible for outputting Q by trigging on rising edge of each clock. When U is 1, the reversible design operator is similar to an Up counter. And when U is 0, the reversible design operator is same as a Down counter correspondingly.

(2) Performance Evaluation

The performance of reversible 4-bit controlled Up/Down synchronous counter can be illustrated easily after referring to the results in Table 3. Its total QC is 64, DL is 64Δ, CI

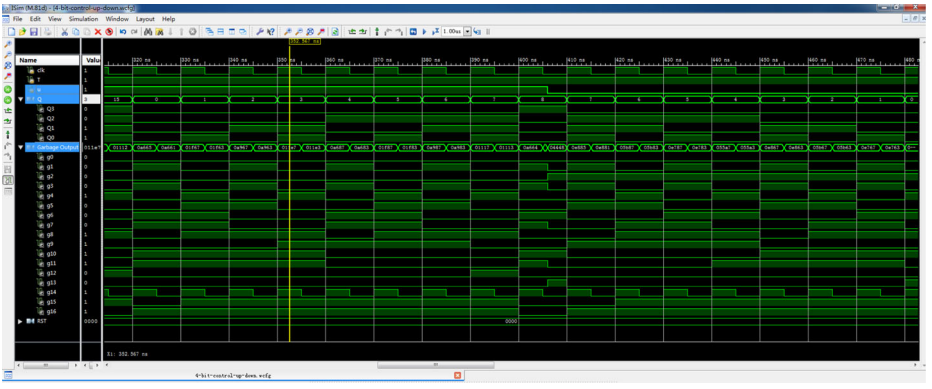


Fig. 19 Functional simulation of reversible 4-bit controlled Up or Down synchronous counter (U=1 or U=0)

is 18 and GBO is 17. It is obvious that the proposed design performs significantly better in terms of QC, DL, CI and GBO.

3.2.3 Performance Analysis of n-bit Up/Down Synchronous Counter

N-bit Up/Down synchronous counter can be implemented by cascade method. When the counter is increased by 1 bit, it must increase 1 T_FF block, 2 PG and 1 MTG. There are n T_FF blocks, 1FG, 2(n-1) PG and (n-1) MTG in the n-bit Up/Down synchronous counter, the number of which is totally 4n-2 and it produces 6+5(n-2) +2 = 5n-2 input constants, $6n + 1 + 2(n - 1) \times 4 + (n - 1) \times 5 = 19n - 12$ unit of delays, $n + 2 + 3(n - 1) + 2 = 4n + 1$ garbage outputs and $6n + 1 + 2(n - 1) \times 4 + (n - 1) \times 5 = 19n - 12$ quantum costs.

4 Functional Simulations

To verify the correctness of logic functions in our circuit according to its logic expression, the functional simulations are implemented. The architectures of two counters are successfully modeled via Verilog HDL. All of the codes are carried out on Xilinx ISE Design Suite 12.4.

Simulation results of two 4-bit counters are revealed in Figs. 16, 17, 18 and 19. In Fig. 16, a 4-bit BCD counter counts in binary coded decimal from 0000 to 1001 and back to 0000 repeatedly on the falling edge of each clock. In Fig. 17, when the control input U is 1, 4-bit Up/Down synchronous counter counts in binary coded from 0000 to 1111 and back to 0000 repeatedly on the rising edge of each clock. In Fig. 18, when the control input U is 0, it counts in binary coded from 1111 to 0000 and back to 1111 repeatedly on the rising edge of each clock. In Fig. 19, the control input U is 1 before a period of time and U is 0 after a period of time. As a result, the counter begins to be an Up counter, and then as a Down counter. In the simulation, the output Q is expressed in decimal form, and the Garbage Output is expressed in hexadecimal. The whole test results demonstrate that the logic functions of two reversible 4-bit counters are correct.

5 Conclusions and Future Work

This paper provides more efficient methods to design quantum reversible 4-bit BCD counter and controlled Up/Down synchronous counter. To my knowledge, the 4-bit BCD counter is the first attempt to apply reversible logic to counter design in the literature. Better than the existing Up/Down synchronous counter, the proposed designs are optimized in terms of QC, GBO and DL. Furthermore, by means of simulator tools, their correctness has been validated. This research method can be extended to the reversible logic design on n-bit counters.

Several research issues deserve further investigation. First, it would be interesting to further optimize the proposed reversible counters using meta-heuristics algorithm. Second, exploring the related applications of reversible counters is a potential research direction. Finally, combining reversible counters with other reversible components for constructing more complex system, such as quantum central processing unit (CPU) could be an interesting topic for our future research efforts.

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