

Optimization Approaches for Designing Quantum Reversible Arithmetic Logic Unit

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Abstract Reversible logic is emerging as a promising alternative for applications in low-power design and quantum computation in recent years due to its ability to reduce power dissipation, which is an important research area in low power VLSI and ULSI designs. Many important contributions have been made in the literatures towards the reversible implementations of arithmetic and logical structures; however, there have not been many efforts directed towards efficient approaches for designing reversible Arithmetic Logic Unit (ALU). In this study, three efficient approaches are presented and their implementations in the design of reversible ALUs are demonstrated. Three new designs of reversible one-digit arithmetic logic unit for quantum arithmetic has been presented in this article. This paper provides explicit construction of reversible ALU effecting basic arithmetic operations with respect to the minimization of cost metrics. The architectures of the designs have been proposed in which each block is realized using elementary quantum logic gates. Then, reversible implementations of the proposed designs are analyzed and evaluated. The results demonstrate that the proposed designs are cost-effective compared with the existing counterparts. All the scales are in the NANO-metric area.

Keywords Reversible logic · Quantum computation · Quantum gates · Quantum cost · Reversible ALU · Low power design · Quantum computer

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1 Introduction

In recent years, reversible logic has emerged as a major factor to improve algorithms and designs for corresponding quantum computers in modern Nanotechnology and quantum computing with minimal impact on physical entropy [1, 2]. Consistent with increasing advances in various sciences, high speed computers are required, as well as, designers of the integrated circuits have tried to draw more functional circuits to increase computers' processing power [3, 4]. Arithmetic logic unit is one of the most important components of the central processing unit, which is a significant portion of any programmable computing system like quantum computing [1, 5, 6]. The CMOS technology is called low power technology because the voltage is applied to current in insulated gate controls [7]. In modern VLSI system, power dissipation is proportional to the number of bits lost during computation [7–9]. This technology has two important features, namely, high noise immunity and low static power [7]. Power consumption is the main concern for realization of integrated circuits [2–4]. Reversible logic can be used as an alternative to reduce entropy increase and the subsequent power consumption that occurs in classical logic circuits by preventing the loss of information. Nanotechnology as a branch of technology appears to be promising due to the design and manufacture of NANO electronic devices at the molecular level of matter. Power consumption causes energy to dissipate [4], which cannot be ignored in NANO-scale devices that are the technology of future designs. Accordingly, the realization of quantum logic circuits based on the properties of fundamental particles is explored. Reversible computing is a possible solution in quantum computations [10] that is beneficial to the development of future quantum technologies. In 1965, Moore pointed out a theory, subsequently known as Moore's law, to predict the development of computer architecture in coming years [8]. According to this law, computers' power will roughly double every two years; but one of the major problems in implementing very large scalable integrated circuits design is the elimination of thermal energy [4], which is created by circuit transistors. Low power circuit with increasing portable electronic devices such as cell phones and handheld computers has become a major issue for designers of the digital circuits [8]. In 1961, Landauer [11] proved that if a circuit performs data processing on the classical trend, $KT \ln 2$ Joules of heat energy would be generated for every bit of information loss, where K is the Boltzmann's constant of 1.38×10^{-23} J/K and T is the absolute temperature at which computation was performed. The dissipating heat at room temperature is around 2.9×10^{-21} J. Energy dissipation was much lower than the static and dynamic powers of the transistors. The energy loss causes chip heat in classical computer, which greatly influences the speed and life of VLSI circuits. In 1973, Bennett [12] showed that the amount of power dissipated in the form of heat, i.e., $KT \ln 2$ Joules for each bit of information lost, would not occur if the circuit is constructed based on reversible logic gates. If a device can actually be run backwards then it is called physically reversible [51]. In fact, the second law of thermodynamics guarantees that it dissipates no heat [51]. However, up to the present, nobody has been successful in coming up with a physical implementation that significantly reduces energy consumption due to reversibility [51]. Quantum computer comprises reversible logic circuits containing wires and quantum gates analogous to how an irreversible computer is constructed from electrical circuits containing wires and gates [10, 17, 18]. A quantum computer is viewed as a quantum network composed of quantum gates, where logic gates perform an elementary unitary operation on one, two or more than two-state quantum systems called 'Qubit' [10, 14, 17, 19]. Synthesis of quantum logic deals with general unitary matrices and

is more challenging than the synthesis of reversible logic [10, 20]. There are some major parameters for determining the complexity and performance of quantum reversible circuits. Firstly, the quantum cost must be minimized. Secondly, the delay caused by considering the longest path from input to output of circuit must also be reduced. Third, the number of constant inputs and garbage outputs, which are utilized for maintaining the reversibility of the circuit, must ideally be omitted or diminished. A high number of lines or qubits decreases the reliability of the system. Thus, keeping the number of circuit lines to a minimum is an important issue [15]. Reversible arithmetic logic unit is a significant unit of programmable computing devices that will be the key components of a quantum processor [1, 5, 6, 22]. Recently, reversible ALUs, which form the essential component of a computing system, have been designed in binary as well as ternary logic as in [1, 5, 6, 22–27], where cost parameters such as number of garbage outputs, quantum cost, number of constant inputs are considered for optimization. These designs are based on the multiplexer method. The aim of this paper is to build three quantum reversible ALUs reasonably that conditionally performs one of several possible arithmetic and logical operations on two operands $|A\rangle$ and $|B\rangle$ depending on control select input data instructions. The rest of the paper is organized as follow: In Section 2, we outline the goals of reversible design, the basic principles and some fundamental quantum logic gates. Section 3 introduces a portion of existing works on reversible ALUs. Section 4 introduces the three new proposed designs of reversible ALU circuits by using the elementary quantum gates. Section 5 gives a brief introduction of the performance analysis and evaluation of the proposed reversible ALUs. Section 6 concludes the present work.

2 Preliminaries

In this section, we will have a brief revision of the definitions and principles of reversible logic.

2.1 Quantum Computing

Quantum computation is defined as the study of information processing tasks accomplished by using quantum mechanical systems. A quantum device must create and maintain these quantum connections in order to have a speed and storage advantage over any conventional computer [10, 17, 18, 20]. Let $|0\rangle$ and $|1\rangle$ are orthogonal, two dimensional complex numbers [13, 14, 19, 21, 27–29]. A qubit $|\psi\rangle$ is a vector whose two pure logic states can be written as $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$, where $|0\rangle$ and $|1\rangle$ denote zero and one digits, respectively [13, 14, 19, 21, 28, 29]. There are complex vectors such that $|\alpha|^2 + |\beta|^2 = 1$. The $|\psi\rangle$ may be expressed in a traditional vector notation as $|\psi\rangle = [a, b]$ (e.g. [13, 21]). More precisely, in quantum computation [21], the state of the computer is described by a complex linear superposition of all binary states of the qubit as $Z_m \in \{0, 1\}$, we have:

$$q(t) = \sum_{Z \in \{0,1\}^m} \partial_z |z_1, \dots, z_m\rangle \quad (1)$$

$$\sum_{Z \in \{0,1\}^m} |\partial_z^2| = 1 \quad (2)$$

Definition 2.1 A QUBIT is the quantum analogue of a classical bit in computation, which can be in a state of superimposition of both 0 and 1. Specifically, the state of a ‘Qubit’ is limited to two numbers, 1 and 0.

Definition 2.2 A promising application of reversible logic is quantum computation. Every quantum circuit works on qubit [14], which is described by a two dimensional complex Hilbert space and is a two level quantum system. The (3) represents the Boolean values 0 and 1 for states of quantum bits [13, 14, 21].

$$|0\rangle \equiv \begin{pmatrix} 1 \\ 0 \end{pmatrix}, |1\rangle \equiv \begin{pmatrix} 0 \\ 1 \end{pmatrix} \tag{3}$$

Definition 2.3 Quantum gates are described in matrix form, which is an efficient method for formulation of quantum computers. A quantum circuit is a cascade of quantum gates (q_i) i.e. $Q = q_0 q_1 \dots q_{d-1}$ In general, a quantum $n \times n$ gate is defined by a $2^n \times 2^n$ matrix. This paper introduces four matrices of quantum gates: NOT, CNOT, Controlled-V and V+ [10, 13, 14, 19, 21, 28, 29].

Definition 2.4 The most common quantum gates act on the spaces of one or two qubits. The quantum 1×1 NOT gate is shown by the following 2×2 matrix. A single qubit is inverted by NOT gate [16]. We have:

$$NOT : \begin{matrix} |0\rangle \rightarrow |1\rangle \equiv \begin{pmatrix} 0 \\ 1 \end{pmatrix} \\ |1\rangle \rightarrow |0\rangle \equiv \begin{pmatrix} 1 \\ 0 \end{pmatrix} \end{matrix} \implies NOT \equiv \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \tag{4}$$

To apply the NOT gate to a state $\begin{pmatrix} \alpha \\ \beta \end{pmatrix}$ vector, we multiply the corresponding state vector on the left by the matrix representation of the gate:

$$NOT \begin{pmatrix} \alpha \\ \beta \end{pmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{pmatrix} \alpha \\ \beta \end{pmatrix} = \begin{pmatrix} \beta \\ \alpha \end{pmatrix} \tag{5}$$

A NOT gate is a 1×1 quantum gate represented as shown in Fig. 1. Since it is the NOT gate, its quantum cost and delay is unity.

Definition 2.5 The CNOT gate can be represented by the 4×4 matrix, which can be expressed in (6) as follows [13, 14, 18, 21]:

$$\begin{matrix} CNOT|00\rangle = |00\rangle \\ CNOT|01\rangle = |01\rangle \\ CNOT|10\rangle = |11\rangle \\ CNOT|11\rangle = |10\rangle \end{matrix} \implies \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} \tag{6}$$

The CNOT gate (Feynman gate) acts on two qubits labeled the control and the target bit [14, 18] The target qubit is inverted if the control is one, which is illustrated in Fig. 2.



Fig. 1 The symbol of 1×1 elementary quantum gate

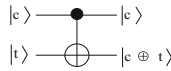


Fig. 2 Feynman gate

Definition 2.6 Controlled-V and controlled-V+ are other fundamental 2×2 quantum gates with the quantum cost of one [19, 21]. Controlled-V+ gate is the hermitian conjugate of Controlled-V, shown in Fig. 3. The V gate named square root of NOT and V+ is hermitian of V with properties presented in (7)~(11) [13, 14, 17, 21, 29].

In the controlled-V gate shown in Fig. 3, when $(A=0)$, $(Q=B)$ and if $(A=1)$, then unitary operations for input B will be as $Q=V(B)$. When the control input is 0, the second input is propagated to the output in both Controlled-V and V+ gates. If the control line is 1, the values on their target lines using the transformation are given by the unitary matrix that can be expressed in (7) and (8) as follows [13, 14, 17, 19, 21]:

$$V = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}^{\frac{1}{2}} = \frac{1+i}{2} \begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix} \tag{7}$$

$$V+ = \frac{1-i}{2} \begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix} \tag{8}$$

When $(A=1)$, $(Q=B)$ and if $(A=0)$, the operation $V+ = V^{-1}$ is performed, i.e. $Q = V + (B)$. A matrix U is unitary if $VV+ = I$, where V+ is the conjugate transpose of V and I is the identity matrix [19, 21, 28, 29]. The Controlled-V and Controlled-V+ quantum gates have some features, which are represented in function in (9)~(11) as follows: [19, 28–30]:

$$V + *V+ = NOT \tag{9}$$

$$V *V+ = I \tag{10}$$

$$V *V = NOT \tag{11}$$

Definition 2.7 The Quantum Cost of a Reversible gate can be calculated by counting the number of the 2×2 reversible logic gates such as Controlled-NOT, Controlled-V and Controlled-V+ gates [1, 2, 19, 28, 29, 31]. This means that any reversible gate can be optimized with 1×1 and 2×2 Reversible logic gates [13, 14, 17, 21]. The quantum realizations of four integrated qubit gates (see [1, 2, 17]) are shown in Fig. 4. In this case, a NOT or CNOT gate, the Controlled-V and Controlled-V+ gates share the same input and output lines. The quantum cost of these structures is one (see list in Fig. 4).

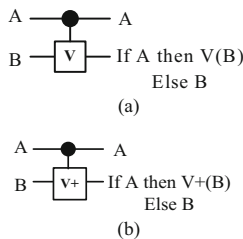


Fig. 3 Quantum realization of integrated Qubit Gates: **a** Square root of NOT (SRN), **b** Hermitian matrix of SRN

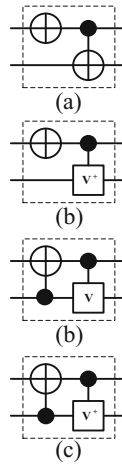


Fig. 4 Quantum Representation of four integrated qubit gates

2.2 Reversible Logic Gates

In a reversible logic gate, there is unique one-to-one mapping between the input vectors; $I_v = \{I_1, I_2, \dots, I_{n-1}, I_n\}$ and the corresponding output vectors; $O_v = \{O_1, O_2, \dots, O_{n-1}, O_n\}$ [15, 16, 32]. According to this definition, in the $n \times n$ reversible logic gate, for each particular (n), there exist a relationship that can be represented as $I_v \leftrightarrow O_v$ [33–35]. Figure 5 shows a block diagram of reversible logic gate that is an $n \times n$ circuit [22, 36–38].

Definition 2.8 In reversible logic circuit, feedback and direct fan-out are not permitted [39–41].

2.3 Cost Metrics

There are some significant differences in this regard, which when used for the synthesis and performance of reversible circuits should minimize the following [22, 30, 32–35, 37–48]:

Constant Inputs This refers to ancillary inputs that are kept constant by the values of 0 or 1 in order to get the required logical function [45–48]. In a reversible logic circuit, inputs that must remain constant, as ‘0’ or ‘1’ are termed as constant inputs. Constant inputs refer to the number of inputs that are to be maintained constant (either at 0 or 1) in order to synthesize a given reversible logical expression using the reversible logic gates [47, 48].

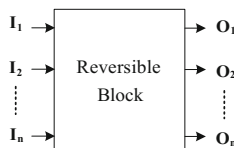


Fig. 5 An $n \times n$ Reversible logic gate

Garbage Outputs The garbage outputs refer to the number of unwanted outputs, which add up to make a logical function in reversible logic circuit [47, 48]. Garbage outputs are used to maintain the reversibility but are not primary or useful outputs [47]. Heavy price is paid off for each garbage output that are not expected only serve to keep the reversibility of the logic circuit [47].

Quantum Cost The quantum cost (QC) is computed knowing the number of elementary quantum operations, which are required to realize quantum circuits that are inherently reversible and manipulate qubits rather than pure logic values. For every reversible circuit that is realized using the number of 1×1 or 2×2 primitive reversible gates, the cost of circuit is the minimum number of these unitary gates [3, 7, 16, 17, 36].

Circuit Lines This refers to the number of lines that can be implemented in a quantum reversible circuit [16, 35].

2.4 The Arithmetic Logic Unit

An ALU performs one of the different micro operations for executing the instructions on two operands A and B depending on control signal inputs, which is suitable for quantum technology and embedded processors [1, 5, 6, 22–27]. The arithmetic logic unit (ALU) can be produced to Boolean functions, such as XOR, AND, OR, NOT, NAND, NOR, MUX (Multiplexer), as well as, basic arithmetic operations, like ADD and SUB. The main basic operations that required to realize ALU are as follows [1, 5, 6, 22–27]:

- ADD (Addition): $(A,B) \rightarrow (A, A + B)$
- SUB (Subtraction): $(A,B) \rightarrow (A, A - B)$
- XOR (Bitwise exclusive-OR): $(A,B) \rightarrow (A, A \oplus B)$
- AND (Bitwise AND): $(A,B) \rightarrow (A, A \wedge B)$
- OR (Bitwise OR): $(A,B) \rightarrow (A, A \vee B)$
- NOP (No-operation): $(A) \rightarrow (A)$

3 Related Works

Related to the classical ALU, a reversible ALU can be designed using a multiplexer to select one of the operations of ALU. In a conventional ALU, ADD and SUB are basic arithmetic operations, while NOT, OR, AND, NOR, NAND & XOR are basic logical operations. In this approach, arithmetic operations are first carried out in parallel and the desired product called result or product is selected using a multiplexer. The other main outputs are Carry out and SUM. On this basis, we present two optimized designs for reversible ALU. Researchers have studied various aspects of reversible ALU based on this approach, such as designing of one bit ALU [5, 6, 23–27, 50]. In [5], two reversible ALU were proposed. These circuits have a quantum cost of 24. They produce 2 garbage outputs and require 2 constant inputs. These circuits produce 8 inputs and 8 outputs. Inputs of S3, S0, A and S4 propagate to the outputs. It generates 6 Boolean functions and includes 7 fixed inputs as selector. In [24], two types of reversible ALUs are presented. The Type1 comprises 5 constant inputs and produces 6 garbage outputs. The quantum cost is 35. Type2 has 5 constant inputs, produces 6 garbage outputs and the quantum cost of the circuit is 30. These two circuits have

10 inputs and generate 10 outputs and include 6 fixed inputs as selectors. In [25], a one-bit reversible ALU is presented that is realized using four 3×3 Fredkin gates [49], two Feynman gates [18], one HNG gate [43] and proposes a reversible logic gate, namely, MG gate [25]. This circuit has a quantum cost of 35, which produces 4 garbage outputs and requires 2 constant inputs. The circuit has 8 inputs and produces 8 outputs. Inputs of S3, S0, A and S4 propagate to the outputs. It generates 6 Boolean functions and includes 7 fixed inputs as selectors. In [23], a new type of one-bit reversible ALU was presented. The structure is a multi-operations ALU based on reversible gates. It contains the reversible control unit and full adder, which are cascaded. The quantum cost of this ALU is 29 and is composed of 4 constant inputs. It produces 8 garbage outputs. This circuit has 10 inputs, which includes 6 fixed inputs as selectors and generates 10 outputs. This ALU circuit can produce 8 arithmetic operations and 4 logic operations. In [26], an n-bit reversible ALU is suggested. The design is cascaded with reversible function generators, reversible controlled units or DXOR circuit and several 3×3 Toffoli gates [9]. The reversible ALU circuit performs logical operations on 2 binary numbers A and B. In evaluation results section, we evaluated this circuit as one bit. It has a quantum cost of 53. The design produces 12 garbage outputs and has 10 constant inputs. In [27], a novel reversible ALU is proposed. The circuits have a quantum cost of 27. They produce 11 garbage outputs and require 6 constant inputs. These circuits produce 10 inputs and 10 outputs. Inputs of S3, S0, A and S4 propagate to the outputs. It generates 12 Boolean functions and includes 6 fixed inputs as selectors. The characteristics of different reversible ALU are tabulated in Table 4. We know that the best design of 1-digit reversible ALU has been presented by Thomsen et al. [6] which is a useful circuit in a quantum computer. The free-garbage ALU circuit in [6] for (n=1) has a quantum cost of 22, which requires no constant inputs. The circuit has 7 inputs and produces 7 outputs. Inputs of S, S1 S2, S3, S4 and A propagate to the outputs. It generates 10 logical and arithmetic operations and includes 5 fixed inputs as selectors. The same strategy was followed in [50]. Recently, in [50], novel design of an n-bit reversible arithmetic logic unit based on a controlled quantum full adder completed Peres gate and Toffoli gate with a sequential arrangement of operations is presented. The design is primarily focus on the selected operations resulting from the combinations of the control lines for the reversible ALU. The costs of the proposed reversible ALUs and the existing designs are giving in Table 4, including the number of circuit lines, garbage outputs, constant inputs, quantum cost, selector inputs and the logical and arithmetic operations.

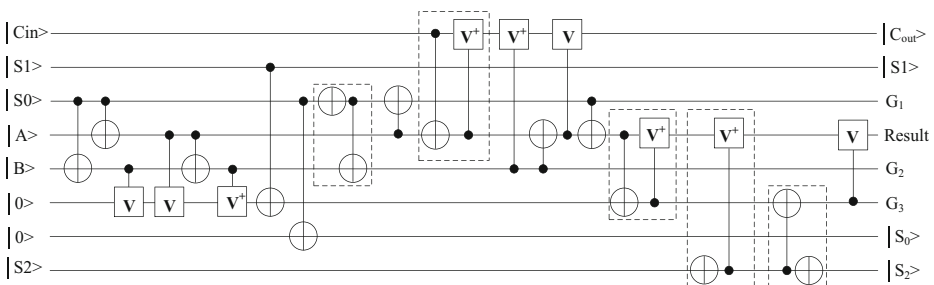


Fig. 6 The Proposed 1-digit reversible ALU by using elementary quantum logic gates (Approach #1)

Table 1 Different functions of the proposed reversible ALU

S_2	S_1	S_0	Result	Functions
0	0	0	(AB)	AND
0	0	1	$(A + B)'$	NOR
0	1	0	$(AB)'$	NAND
0	1	1	$(A + B)$	OR
1	0	0	$A \oplus B \oplus Cin$	ADD
1	0	1	$A \oplus B \oplus Cin$	SUB

4 Proposed Designs

The part of the computer that performs the bulk of data-processing operations is called the central processing unit (CPU) [1, 6, 22]. The CPU is made up of three major parts consisting of control unit, arithmetic and logic unit and processor unit [5, 23–27]. The ALU has an important role and performs the required micro operations for executing the instructions [1, 22, 26, 27]. In order to design an effective reversible ALU, the number of logical and arithmetic calculations produced on the outputs must be considered in addition to the quantum cost and other evaluation parameters. The proposed reversible ALU circuits produce the greatest number of calculations at the lowest quantum cost. This paper presents three approaches for the design of reversible ALUs, which are as follow:

In the first design, the proposed reversible ALU has 8 inputs and 8 outputs. The elementary quantum gates are utilized in the implementation of the proposed ALUs. The first presented circuit is used to produce six logical calculations in the result output: ADD, SUB, AND, NAND, OR and NOR. The inputs consist of three data inputs (A, B and C_{in}), three select lines (S_0, S_1, S_2) and two constant inputs. The circuit can regenerate all selector inputs on the outputs (S_0, S_1, S_2). The 8 outputs are: S_0, S_1 and S_2 propagated to the output, C_{out} /Borrow, Result and three garbage outputs. It produces two arithmetic and four logical calculations. The first design for one-bit reversible ALU is shown in Fig. 6, which requires five dotted rectangles, four V, two V+ and eight CNOT gates. Dotted rectangle is equivalent to a CNOT gate with cost of one. The total QC equals 19. The functions produced by the first approach are given in Table 1. According to the Table 1, depending on existence values in select inputs, the circuit produces six functions, namely, ADD and SUB, which are arithmetic functions, and AND, NAND, OR and NOR, which are logical functions, in the result output.

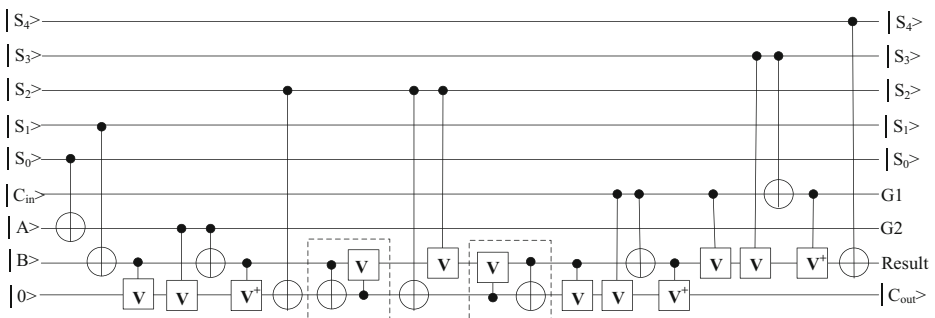


Fig. 7 TheProposed1-digit reversible ALU using with elementary quantum gates (Approach#2)

Table 2 Elementary Operation of reversible ALU

Result	C_{in}	S_0	S_1	S_2	S_3	S_4	Transformations	Description
$A + B$	0	0	0	0	0	0	$F = A + B + 0$	ADD without carry
$A + B + 1$	1	0	0	0	0	0	$F = A + B + 1$	ADD with carry
$A - B$	1	0	1	0	0	0	$F = A + B' + 1$	SUB
$A \oplus B$	0	0	0	0	1	0	$F = A \oplus B$	Exclusive-OR
$A \wedge B$	0	0	0	1	1	0	$F = A \wedge B$	Bitwise-AND
$A \vee B$	0	1	1	1	1	1	$F = (A' \wedge B')'$	Bitwise-OR
$(A \oplus B)'$	0	0	0	0	1	1	$F = (A \oplus B)'$	Exclusive-NOR
$A + 1$	1	0	0	0	0	0	$F = A + 0 + 1$	Self-increment of A
$A - 1$	1	0	1	0	0	0	$F = A + 1' + 1$	Self-decrement of A
A'	0	1	0	0	0	0	$F = A' + 0 + 0$	Bitwise negation of A
A'	1	1	0	0	0	0	$F = A' + 0 + 1$	Complement of A
A	0	0	0	0	0	0	$F = A + 0 + 0$	NOP (No operation)

In the second design, the proposed reversible ALU has 9 inputs and 9 outputs. The second design of one bit reversible ALU is illustrated in Fig. 7. We have designed the reversible ALU by quantum logic gates. We have used two dotted rectangles, eight V, four V+ and six CNOT gates. From the ALU, we get three input values (A, B and C_{in}), three select lines (S_0, S_1, S_2, S_3, S_4) and one constant input. The main outputs are: F (as product output) and C_{out} . In the second design, the total QC equals 24. There are 2 garbage values and 1 constant input. It has 9 circuit lines and 5 selection lines. The presented design can be implemented with 7 gates. We can construct n-bit ALU by cascading n number of this 1-bit ALU circuit. We can see that the inputs A, B and C_{in} can be controlled depending upon the values of the selection and carry input lines. The product output is F (as a final output), which will be obtained from 12 different operations, either arithmetic or logical, depending upon the values of C_{in} (as carry input) and selection lines. The other main output is carry out (C_{out}). The 12 operations generated in the second design are given in Table 2. A particular function is selected through (S_0, S_1, S_2, S_3, S_4). The presented circuit has two main outputs (Result and C_{out}). This circuit has 5 select control signals with a provision for realizing 12 logical and arithmetic operations. The total elementary operations of the second ALU design are tabulated in Table 2. By transforming the expressions based on the second approach, an extension of ALU can perform other operations (such as NAND, NOR), which are universal functions. Therefore, the second presented ALU circuit can implement several universal and arithmetic operations like ADD, SUB, AND, NAND, OR, NOR, EX-OR, EX-NOR, etc.

In the third design, the proposed reversible ALU has 7 inputs and 7 outputs. The third design of one bit reversible ALU is as shown in Fig. 8. We have used four V, two V+ and six CNOT gates. From the ALU, we get two input values (A, B), five selectors (S_0, S_1, S_2, S_3, S_4). The main outputs are result. In the design 3, the total QC equals 12. There is no garbage values and constant inputs. The product output (Result) will be obtained from 10 different operations that are Table 3. By transforming the expressions based on the third approach, an extension of ALU can perform basic arithmetic–logical operations (ADD, SUB, NSUB, XOR, NOP). The presented design 3 is the garbage-free reversible quantum ALU, which has not constant inputs.

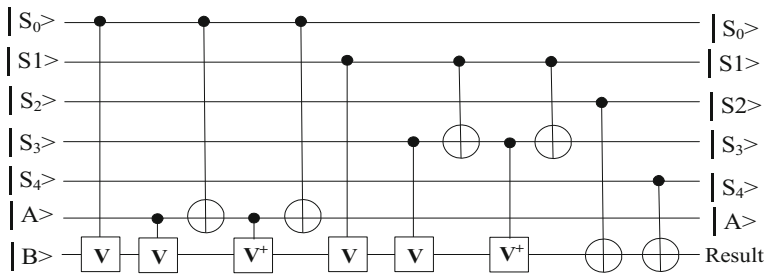


Fig. 8 TheProposed 1-digit reversible ALU using with elementary quantum gates (Approach#3)

5 Evaluation Results and Performance Analysis

Table 4 shows the comparison of the two proposed reversible ALU with other designed circuits in [5, 6, 23–27] references. The presented reversible arithmetic and logic units have four major advantages compared with the previous works. First, the presented circuits produced lowest quantum cost, which is one of the most important parameters in the evaluation of quantum circuits. The second advantage is the number of produced functions. The third advantage is the circuit lines. As shown in Table 1, our proposed circuit based on the first approach produces 6 functions, and according to Table 2, the second proposed circuit produces 12 operations, which are more than the functions of the existing works in [5, 23–27]. Table 3 show that the third circuit produces 5 basic operations and 5 Boolean functions. In the last column, parameters with star (*) symbol indicate the number of arithmetic functions. Furthermore, keeping the number of lines in reversible circuits as small as possible is a significant subject, particularly in the design of quantum circuits [4, 16]. In [25, 26] references, the number of lines is 13 while our design has 10 lines, which is equal to [5, 23–27] references. M. Morrison et al. in [25] presented a reversible ALU that produces 8 functions with 7 select inputs, while we reduced the number of select inputs to 5 lines with 9 functions. The number of garbage outputs, constant inputs and number of gates are better compared to [23–27] references and are equal to those in the existing circuit in [5]. The circuit in [23] produces high garbage outputs with high constant inputs, quantum cost and gates count. To the best of our knowledge, hitherto one reversible quantum ALU circuit was suggested in previous researches, as that is now referred to [6] reference. For $n=1$, It does not constant inputs and garbage outputs, which has quantum cost of 22 The presented reversible n -bit ALU in [6] producing 10 basic operations, having a quantum cost of at least 22, provided that the statement holds for the base case $n=1$. It has 7 circuit lines and 5 control select inputs. Among the existing works shown in Table 4 for the design of n -digit reversible ALU, the design presented in [6] has the minimum number of garbage outputs and constant inputs, while the design presented in [50] has the 19 operations resulting from the combinations of control lines that is better than [6]. In [50], reversible an n -bit ALU requires $26n$ quantum cost, $(n+2)$ garbage outputs where n is the number of data bits. Since $n=1$, thus, the existing design in the literature [50] has require at least the quantum cost of 26, 2 constant inputs, and also requires 1 garbage outputs. The design has 10 circuit lines, 6 control select inputs and produces 19 operations, which two operations are clearly irreversible. The constant inputs of [6] and [50] are also declared as “unknown” in [6, 50] but there are equal to zero and $2n$ respectively. Thus we have shown the comparison of our proposed works with the design presented in [6] and [50] in Tables 4 in terms of number of constant

Table 3 Basic Operations for the reversible ALU

S_0	S_1	S_2	S_3	S_4	ALU operations	Description
1	1	0	0	0	$F = A + B$	ADD
1	1	1	0	1	$F = B - A$	SUB
1	1	0	1	1	$F = A - B$	NSUB
1	0	0	0	0	$F = A \oplus B$	EX-OR
0	0	0	0	0	$F = B$	NOP
1	1	0	1	0	$F = B + A + 1$	ADD with carry
1	1	1	1	1	$F = B - A - 1$	SUB with borrow
1	1	0	0	1	$F = A - B - 1$	NSUB with borrow
1	0	1	0	0	$F = (A \oplus B)'$	EX-NOR
0	0	1	0	0	$F = B'$	Negation of B

inputs, number of garbage outputs, quantum cost, circuit lines, control inputs, basic operations and quantum cost respectively for value of $n=1$ digit. Increase circuit lines should not lead to increased circuit cost. Another point to be noted with regard to this case is that the number of reversible gates is not a good metric of optimization as each reversible logic gate is of different type and computational complexity, and thus will have a different quantum cost. The computational complexity of a reversible gate can be represented by its quantum cost. So, the quantum cost is more important. As the optimization of constant input bits and the garbage output bits may impact the design in terms of the quantum cost, thus quantum cost issue is also considered for optimization with primary focus towards the optimization of number of constant input bits and the garbage outputs. Beside the much more logical and arithmetic operations offered by the quantum ALU circuits suggested in this study, they are better than the existing counterparts [5, 6, 24–27, 50]. The proposed first design is better than [6] in terms of the number of select inputs and quantum cost. The first design

Table 4 Comparative experimental results of different one-digit reversible ALU circuits

Designs	Circuit lines	Constant inputs	Garbage outputs	Select inputs	Quantum cost	Produced functions
Design I	8	2	3	3	19	$4 + 2^* = 6$
Design II	9	1	2	5	20	$4 + 8^* = 12$
Design III	7	0	0	5	12	$5 + 5^* = 10$
Existing Design in [50]	10	2	2	6	26	$17 + 2 = 19$
Existing Design in [6]	7	0	0	5	22	$5 + 5^* = 10$
Existing Design in [5]	10	2	2	5	24	$4 + 2^* = 6$
Existing Design in [23]	10	4	8	4	29	$4 + 8^* = 12$
Existing Design in [24]	10	5	6	3	30	$3 + 1^* = 4$
Existing Design in [25]	13	2	4	7	35	$6 + 2^* = 8$
Existing Design in [26]	13	10	12	4	53	$8 + 4^* = 12$
Existing Design in [27]	10	6	11	3	27	$4 + 8^* = 12$

is also better than [50] in terms of the number of circuit lines, control selector inputs and the quantum cost. The proposed second design is better than the earlier designs [5, 23–27] in terms of constant inputs and also better than [6] in terms of quantum cost. The second design is also better than [50] in terms of the number of constant inputs, circuit lines, select inputs and quantum cost. The third design is much better than the earlier designs [5, 23–27] in terms of constant inputs, garbage outputs, circuit line and the quantum cost. The presented ALU based on the third approach is garbage free and does not use constant inputs. It has quantum cost of 12 that is better than the existing designs [5, 6, 23–27]. The third design uses much fewer constant inputs for five basic arithmetic–logical operations and five Boolean functions. Inputs of A, S0, S1, S2, S3 and S4 propagate to the outputs. This free-garbage design is possible with much fewer garbage outputs than the existing designs in [5, 23–27]. It is optimized in terms of the quantum cost than previously thought. Table 4 gives a detailed list of the cost metrics of the presented designs. The proposed circuit based on third approach is improved in terms of quantum cost than the existing circuit in [6]. Resultantly, our proposed designs are better than the existing circuits [5, 6, 23–27] in terms of number of circuit lines, quantum cost. The proposed third design is better than [6] in terms of quantum cost. The design also is better than [50], in terms of the number of circuit lines, control inputs, garbage outputs, constant inputs and quantum cost.

6 Conclusions

In this paper, we put forward three new approaches for one-bit reversible ALU design, which were constructed by the combination of elementary quantum gates. The proposed ALU designs could handle many elementary logical and arithmetic operations such as addition, subtraction, exclusive-OR, bitwise AND, NAND, bitwise OR, NOR, exclusive-NOR, negation, complement, etc. In order to design the cost-effective reversible ALU, the number of logical and arithmetic calculations produced on the outputs, must be considered in addition to the quantum cost and other evaluation issues. The quantum cost of the proposed designs is very attractive. The proposed designs were evaluated in terms of number of circuit lines, garbage outputs, constant inputs, quantum cost. The reported results indicated the superiority of the proposed circuit compared with previous circuits. It can be said that the presented designs have better logic cost efficiency than those prevalent in the literature, with due considerations given to cost metrics like quantum cost and circuit lines, etc. The proposed designs are versatile approaches for the realization of quantum computing with having both a remarkable low power consumption and NANO-scaling. Therefore, the designs will be implemented with elementary quantum gates, which have their scope to be realized in the nanotechnology based systems, like the quantum cellular automata; there are definitely NANO-metric architectures. The presented circuits can be used in the wide variety of large reversible systems and enhance the performance of quantum computers. Moreover, many quantum logic operations as well as classical logic operations should be of concern in the complete reversible ALU. Consequently, an optimized ALU is on demand in computer system and Digital Signal Processor for the design of the instruction set of the more complex systems and low-power VLSI design in nanotechnology, quantum computers and programmable computing devices.

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