Optimization Approaches for Designing a Novel 4-Bit Reversible Comparator

Ri-gui Zhou · Man-qun Zhang · Qian Wu · Yan-cheng Li

Abstract Reversible logic is a new rapidly developed research field in recent years, which has been receiving much attention for calculating with minimizing the energy consumption. This paper constructs a 4×4 new reversible gate called ZRQ gate to build quantum adder and subtraction. Meanwhile, a novel 1-bit reversible comparator by using the proposed ZRQC module on the basis of ZRQ gate is proposed as the minimum number of reversible gates and quantum costs. In addition, this paper presents a novel 4-bit reversible comparator based on the 1-bit reversible comparator. One of the vital important for optimizing reversible logic is to design reversible logic circuits with the minimum number of parameters. The proposed reversible comparators in this paper can obtain superiority in terms of the number of reversible gates, input constants, garbage outputs, unit delays and quantum costs compared with the existed circuits. Finally, MATLAB simulation software is used to test and verify the correctness of the proposed 4-bit reversible comparator.

Keywords Reversible comparator · ZRQ gate · ZRQC module · MATLAB · Reversible logic

1 Introduction

As for interdisciplinary of quantum mechanics and information science, quantum information has offered new technology of last Moore era for people, and has been one of the focuses for strategic competition all over the world. At present, the integration of computer chips increases double for a year and a half. However, in fact, Moore's law is losing of function when the line width of integration circuit keeps reducing. Along with the advancement in large-scale integrated circuit, especially VLSI (Very Large Scale Integration), emerged

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in better logic circuits, the energy dissipation of integration circuit has been a severe challenge to the electronics industry. Therefore, for high technology circuits and systems, one of the most urgent problems need to be solved how to decrease the energy dissipation of integration. Considering of the above problems, the designing of quantum reversible logic based on quantum calculation has been gradually received much attention by international academic community. In 1960s, Landauer's [1] principle stated that regardless of the high level of integration and realization technique, the conventional combinational logic circuits would inevitably lead to energy dissipation due to information loss in the running process. It was proved that the loss of each bit of information dissipated $kT \ln 2$ Joules of heat energy, where k was Boltzmann's constant of 1.38×10^{-23} J/K and T was the absolute temperature at which computation was performed. At room temperature, the dissipating heat was around 2.9×10^{-21} J. Energy dissipation cause chip heat of irreversible computer which brings big influence on the speed and life of CMOS devices. But in the 1973, Bennett [2] found that energy dissipation came from irreversible operation in the process of calculation. If the network consisted of reversible logic circuits only, zero energy dissipation would be possible. Thus, reversible logic is likely to be in demand in high speed power aware circuits.

In fact, classic computer is an irreversible Universal Turing Machine and those can be replay by the corresponding reversible Turing Machine due to the same calculation ability and calculation efficiency [3]. It is theoretically proved that [4], quantum computer can be equivalent to reversible Turing Machine which can also be equivalent to quantum reversible logic circuit. A quantum computer constitutes of quantum circuits containing wires and quantum gates as analogous to the way that a classical computer is built from electrical circuits containing wires and logic gates [3]. But the biggest difference between bits of classical computer and qubits of quantum computer is that a qubit can form linear combinations of states $|0\rangle$ and $|1\rangle$ called superposition, while the basic states $|0\rangle$ and $|1\rangle$ are an orthonormal basic of a two-dimensional complex vector space [3]. A superposition can be denoted as $|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle$ that stands for the probability of the paper being measured in state 0 is $|\alpha|^2$, or the result 1, with the probability of $|\beta|^2$, and $|\alpha|^2 + |\beta|^2 = 1$.

Quantum computer composes of reversible logic circuit. Reversible logic circuit will become an essential property in future circuit design for calculation with minimum energy dissipation. In reversible logic circuit, reversible function has a one-to-one mapping between patterns of its inputs and outputs. That is to say, the number of inputs must be equal to the number of outputs [5]. It is inevitable that reversible logic circuit may have a number of unwanted outputs called garbage outputs [6]. Obviously, the influence is smaller in process of reversible circuit design when proposed circuit using fewer garbage outputs. To minimize garbage outputs, the outputs of each gate should be full used as inputs for other gates as many as possible. What's more, other parameters such as the number of gates and quantum costs are considered to measure the complexity of a reversible logic design. Reversible logic can not only be in application of quantum computer but also are of high interest in optical computing [7], nanotechnology [8] and low-power CMOS design [9].

Comparator is a synthetic circuit used to compare the two numbers of n-bit. The existing papers [10–13] have designed some reversible comparators, but these comparators required a considerable amount of resources (circuit complexity, garbage outputs and quantum costs). The goal of designing quantum logic network is to complete specific features in low-power network, with the calculation ability of powerful quantum theory to implement network's fast storage and fast calculation. The premise of instructing reversible logic network is to engage for the usage of optimization method to design the specific function of quantum logic circuit. This paper constructs a new 4×4 reversible gate called ZRQ (Here ZRQ stands for an acronym for which we just want to keep the names of the proposed reversible full adder

as short as possible so that it is easy to remember, no other special meanings), to build quantum adder and subtraction. Meanwhile, reversible ZRQC module for completing 1-bit comparator is designed by using the proposed ZRQ gate. What's more, this paper designs 4-bit reversible comparator based on the proposed ZRQC module. The author presents 1-bit and 4-bit reversible comparator with six different goals: the minimum number of gates, input constants, garbage outputs, quantum costs, unit delays and the optimum circuit in terms of all the above parameters. MATLAB simulation software is also used to test and verify the correctness of the proposed 4-bit reversible comparator.

The rest of the paper is organized as follows. Section 2 proposes a portion of existed reversible gates; Sect. 3 introduces the analogous applications of the proposed ZRQ gate, and designs novel 1-bit and 4-bit reversible comparator by using the proposed ZRQC module based on ZRQ gate; Sect. 4 makes brief introduction of performance analysis of the proposed reversible comparator. Section 5 shows the correctness of the proposed 4-bit reversible comparator by MATLAB simulation. Section 6 concludes the work at present and briefs the future work as well.

2 Basic Reversible Logic Gates

2.1 Reversible Logic Gate

Reversible logic gate is the circuit of n-bit inputs and n-bit outputs which is a one-to-one correspondence between its inputs vectors and outputs vectors. That is to say, the input vector states can always be reconstructed from the output vector states uniquely in reversible computing system. For content of reversible requirements, reversible gates have some features as follows:

1. The number of inputs must be equal to the number of outputs;
2. Do not allow feedback from part line to another part line;
3. Do not allow fan-in or fan-out [14, 15].

2.2 Optimization Parameters

In research of reversible logic circuit, we can not only find the method of completing the reversible of quantum circuit, but also look for the optimization of reversible circuit in the consolidated results. Optimization parameters have direct influences over the performance and the running speed of reversible logic circuit. The factors to take into consideration for optimization parameters are as follows:

1. Use the minimum number of input constants that are the input logic expression of reversible gates.
2. Use the minimum number of reversible gates that realize the function of reversible logic circuits.
3. Use the minimum number of garbage outputs that are not necessary in the synthesis of a given function.
4. Use the minimum number of quantum costs which is calculated as a total sum of 1×1 gates and 2×2 gates used.
5. Use the minimum number of unit delays which are the time interval of information transferring from input to output with a gate as the unit of time to calculate.

Fig. 1 FG and quantum equivalent circuit of FG
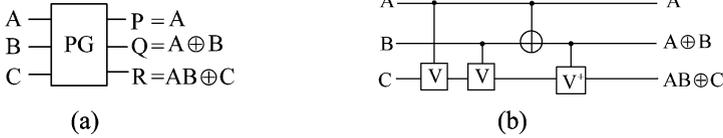
Fig. 2 PG and quantum equivalent circuit of PG
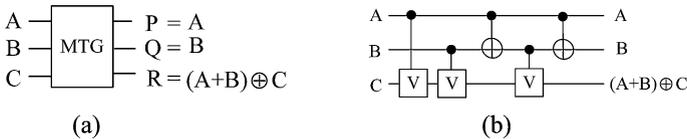
Fig. 3 MTG and quantum equivalent circuit of MTG

2.3 Basic Reversible Logic Gates

There have existed a number of reversible logic gates in literature. Here just introduces some parts of them which will be used in the proposed reversible circuit below. FG (Feynman gate) [16], known as controlled NOT (1-CNOT), has two input bits, which are the control quantum bit and target quantum bit respectively. FG implements the logic functions as $P = A$ and $Q = A \oplus B$, depicted in Fig. 1(a). FG can implement the logic function of XOR gate. If the second input of FG is set to 0, then FG will copy the first input to both outputs of the gate. So FG is the most suitable gate to realize the copy for a single quantum bit. FG is a 2×2 reversible gate, and its quantum cost is 1. The quantum equivalent circuit of FG is depicted in Fig. 1(b). PG [17] and MTG [18] are quantum gates with three input bits and three output bits. The block diagram for 3×3 PG (Peres gate), known as New Toffoli gate, is shown in Fig. 2(a). It implements the logic functions as follows $P = A$, $Q = A \oplus B$ and $R = AB \oplus C$. When the third input of PG is set to 0, PG can implement the function of AND gate. Equivalent quantum realization of PG is depicted in Fig. 2(b). In Fig. 2(b), V is a square-root-of NOT gate and V^+ is its Hermitian. Thus, VV or $V^+ V^+$ creates a unitary matrix of NOT gate and $VV^+ = I$ or $V^+V = I$ (an identity matrix, describing just a quantum wire). So the quantum cost of PG is 4. MTG (Modified Toffoli gate) is a 3×3 reversible logic gate and is drawn in Fig. 3(a). It implements the logic functions as $P = A$, $Q = B$ and $R = (A + B) \oplus C$. When the third input of MTG is set to 0, MTG can implement the function of OR gate. Equivalent quantum realization of MTG is depicted in Fig. 3(b), and the quantum cost of MTG is 5.
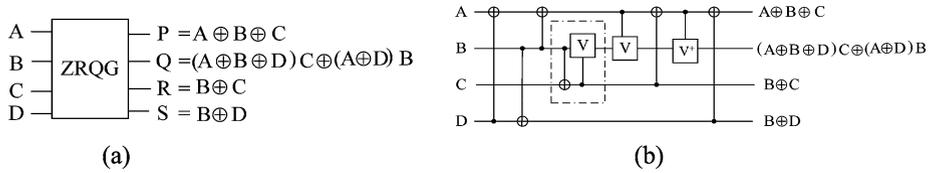
Fig. 4 ZRQG and quantum equivalent circuit of ZRQG

Table 1 Truth table of the proposed ZRQ gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	1	1	1	1
0	1	0	0	1	0	1	1
0	1	0	1	1	1	1	0
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	1	0
1	0	1	1	0	0	1	1
1	1	0	0	0	1	1	1
1	1	0	1	0	0	1	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	0	0

3 The Proposed New ZRQ Gate and the Design of Novel Reversible Comparator

3.1 The Proposed New ZRQ Gate

The proposed new ZRQ gate is drawn in Fig. 4(a). It is a 4×4 reversible logic gate. The corresponding truth table of proposed ZRQ gate is shown in Table 1, from which can be verified that a corresponding output pattern can be uniquely determined from the input pattern. ZRQ gate is a reversible gate from its truth table. Equivalent quantum realization of ZRQG is depicted in Fig. 4(b), and each dotted rectangle in Fig. 4(b) is equivalent to a 2×2 CNOT gate. So the quantum cost of ZRQG is 8.

3.2 Some Applications of ZRQ Gate

The proposed ZRQ gate, a universal gate, can implement all Boolean functions [21, 22]. When the third input C and the fourth input D (in Fig. 4(a)) are set to 0, the ZRQ gate simultaneously implements the AND function and the XOR function, depicted in Fig. 5a. Similarly, setting $C = 1$ and $D = 0$ (in Fig. 4(a)), the ZRQ gate implements the XNOR, OR and NOT functions as depicted in Fig. 5b.

ZRQ gate can work by itself as a reversible full adder and a reversible full subtraction, depicted in Fig. 6a and Fig. 6b respectively. If input $D = 0$, the proposed gate works as a reversible full adder, and if input $D = 1$, then it works as a reversible full subtraction.

Fig. 5a AND and XOR gates
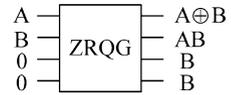
Fig. 5b XNOR, OR and NOT gates
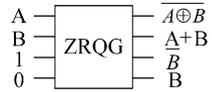
Fig. 6a ZRQG gate implemented as full adder
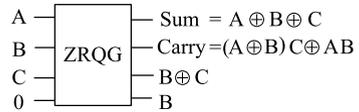
Fig. 6b ZRQG gate implemented as full subtraction
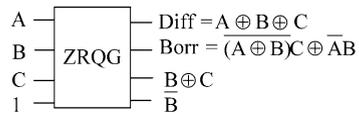
Table 2 The truth table of 1-bit comparator

Input		Output		
A	B	$F_{A>B}$	$F_{A=B}$	$F_{A<B}$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

3.3 The Design of Novel 1-Bit Reversible Comparator

There are tremendous calculation functions in digital system especially computer system. One of the easiest calculation functions is to compare the two numbers A and B. Magnitude comparator is a logic circuit that compares the size of A and B, then determines the result among A > B, A < B and A = B. When the two numbers in comparator circuit are two 1-bit numbers, the result will be only one bit from 0 and 1, so the circuit is called for 1-bit magnitude comparator which is a basic of the two numbers of n-bit. The truth table of 1-bit conventional comparator is listed in Table 2 as follows:

From the truth table of connectional comparator in Table 2, the logical expressions of 1-bit comparator is as follows:

$$F_{A>B} = A\overline{B} \tag{1}$$

$$F_{A=B} = \overline{A \oplus B} \tag{2}$$

$$F_{A<B} = \overline{A}B \tag{3}$$

According to the logical expression, we can represent logic diagram of 1-bit irreversible comparator as illustrated in Fig. 7 which makes cascaded connection by two NOR gates, two AND gates and one XNOR gate. In conference [13], the research gets the 1-bit reversible comparator shown in Fig. 8 by using two Feynman gates to copy two inputs A and B, by

Fig. 7 1-bit irreversible comparator
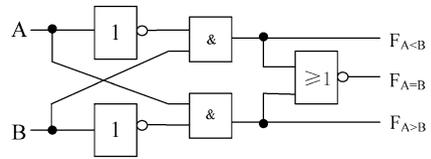
Fig. 8 The existing 1-bit reversible comparator
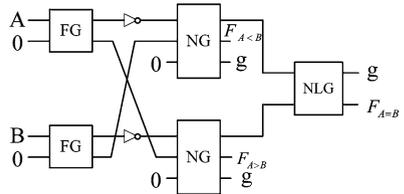
Fig. 9 ZRQC module with complementing 1-bit reversible comparator
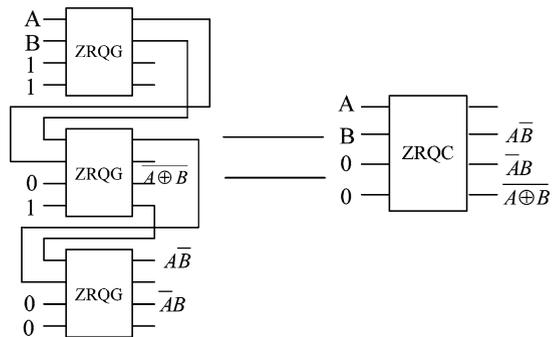
using NG gates [19] take replace of the classical AND gates and by using NLG gate replaces the classical OR gate.

The existed 1-bit reversible comparator in conference [13] uses a great number of reversible gates to complement the design of 1-bit reversible comparator, which apparently influences the performance of the circuit network. In order to use optimal parameters with the least cost, this paper constructs the 1-bit reversible comparator with optimal parameters by means of cascade connection of the proposed ZRQ gate as it can complement all Boolean functions. But the proposed ZRQ gate could not directly illustrate the logical expression of 1-bit comparator, so we make some change to the proposed ZRQ gate and three of them are cascaded to produce the $F_{A>B}$, $F_{A<B}$, and $F_{A=B}$ blocks which is called for ZRQC module to accomplish 1-bit reversible comparator, shown in Fig. 9.

According to Fig. 9, we could design the quantum equivalent circuit of ZRQC module, depicted in Fig. 10. It is obvious that ZRQC module is actually a reversible gate with 4-bit inputs and 4-bit outputs. It implements the logic functions as follows: $P = A$, $Q = \overline{A \oplus B}$, $R = A\overline{B} \oplus C$, and $S = \overline{A}B \oplus C \oplus D$. Its quantum cost is 7. When we set the third input and the fourth input into 0, ZRQC has only one garbage output produced from the 1-bit reversible comparator circuit. The corresponding truth table of ZRQC module is listed in Table 3 as follow. That the corresponding inputs and outputs meet the requirement of reversible logic circuit from the truth table of the proposed ZRQC module.

Fig. 10 The quantum equivalent circuit of ZRQC module
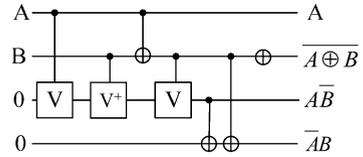
Table 3 The truth table of ZRQC module

A	B	C	D	A	$\overline{A \oplus B}$	$A\overline{B} \oplus C$	$\overline{A}B \oplus C \oplus D$
0	0	0	0	0	1	0	0
0	0	0	1	0	1	0	1
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	0
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

3.4 The Design of 4-Bit Reversible Comparator

The conventional 4-bit comparator is used for comparing two 4-bit numbers like $A_3 A_2 A_1 A_0$ and $B_3 B_2 B_1 B_0$. The corresponding truth table of 4-bit comparator is shown in Table 4.

We can receive the logical expression of 4-bit comparator as follows from Table 4:

$$F_{A>B} = (A_3 > B_3) + (A_3 = B_3)(A_2 > B_2) + \cdots + (A_3 = B_3)(A_2 = B_2)(A_1 = B_1)(A_0 > B_0) \tag{4}$$

$$F_{A<B} = (A_3 < B_3) + (A_3 = B_3)(A_2 < B_2) + \cdots + (A_3 = B_3)(A_2 = B_2)(A_1 = B_1)(A_0 < B_0) \tag{5}$$

$$F_{A=B} = (A_3 = B_3)(A_2 = B_2)(A_1 = B_1)(A_0 = B_0) \tag{6}$$

The comparator principles drawn from the above logical expressions of 4-bit comparator are that, firstly, comparing A_3 to B_3, if A_3 is not equal to B_3, we will clearly obtain the result from Table 4. But if A_3 equals to B_3, we need to compare A_2 and B_2 to get the result. If A_2 and B_2 are the same, then we can't get the result until comparing their lowest bits A_0 and B_0.

This paper presents the 4-bit reversible comparator according to the proposed 1-bit reversible comparator with least quantum cost. Firstly, n-bit OR gates will be designed by using the proposed FG in Fig. 1. However, take an example of $F_{A>B}$, it is easy to note that $(A_3 > B_3)$, $(A_3 = B_3)(A_2 > B_2)$, $(A_3 = B_3)(A_2 = B_2)(A_1 > B_1)$ and $(A_3 = B_3)(A_2 = B_2)$

Table 4 The truth table of conventional 4-bit comparator

Input				Output		
$A_3\ B_3$	$A_2\ B_2$	$A_1\ B_1$	$A_0\ B_0$	$F_{A>B}$	$F_{A<B}$	$F_{A=B}$
$A_3 > B_3$	×	×	×	1	0	0
$A_3 < B_3$	×	×	×	0	1	0
$A_3 = B_3$	$A_2 > B_2$	×	×	1	0	0
$A_3 = B_3$	$A_2 < B_2$	×	×	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	×	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	×	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	0	1

Fig. 11 N-bit XOR gate
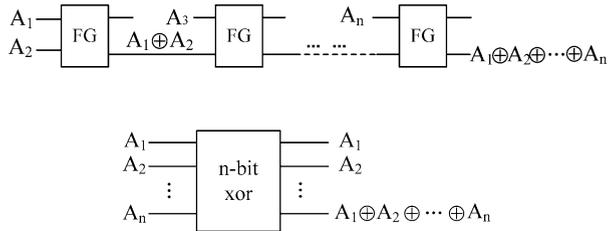
$(A_1 = B_1)\ (A_0 > B_0)$ cannot be set at the same time. So the logical expressions of 4-bit comparator will also be changed as follows:

$$F_{A>B} = (A_3 > B_3) \oplus (A_3 = B_3)(A_2 > B_2) \oplus \cdots \oplus (A_3 = B_3)(A_2 = B_2)(A_1 = B_1)(A_0 > B_0) \tag{7}$$

$$F_{A<B} = (A_3 < B_3) \oplus (A_3 = B_3)(A_2 < B_2) \oplus \cdots \oplus (A_3 = B_3)(A_2 = B_2)(A_1 = B_1)(A_0 < B_0) \tag{8}$$

$$F_{A=B} = (A_3 = B_3)(A_2 = B_2)(A_1 = B_1)(A_0 = B_0) \tag{9}$$

So we need to design n-bit XOR gates at first. As mentioned above that FG can accomplish XOR function, this paper cascades connection of $n-1$ FG gates to replace n-bit XOR gate, shown in Fig. 11 which could be applied to the construction of the 4-bit reversible comparator.

This paper proposes a novel reversible 4-bit comparator with the optimal parameters by using 4-bit XOR gates, the proposed ZRQC module and PG, shown in Fig. 12. Also, in accordance with standards that fan-in and fan-out are not allowed in a reversible logic circuit, full consideration has given to out circuit structure.

According to logical expression of 4-bit conventional binary comparator, equation of $F_{A<B}$ also can be obtained as followed:

$$F_{A<B} = \overline{F_{A>B} \oplus F_{A=B}} \tag{10}$$

From Eq. (10), it is apparently that the complement of 4-bit $F_{A<B}$ just has a close relationship with $F_{A<B}$ and $F_{A=B}$. So some changes are given to the proposed ZRQC module for only producing $F_{A<B}$ and $F_{A=B}$, called for ZRQC1, as shown in Fig. 13, and the changed circuit
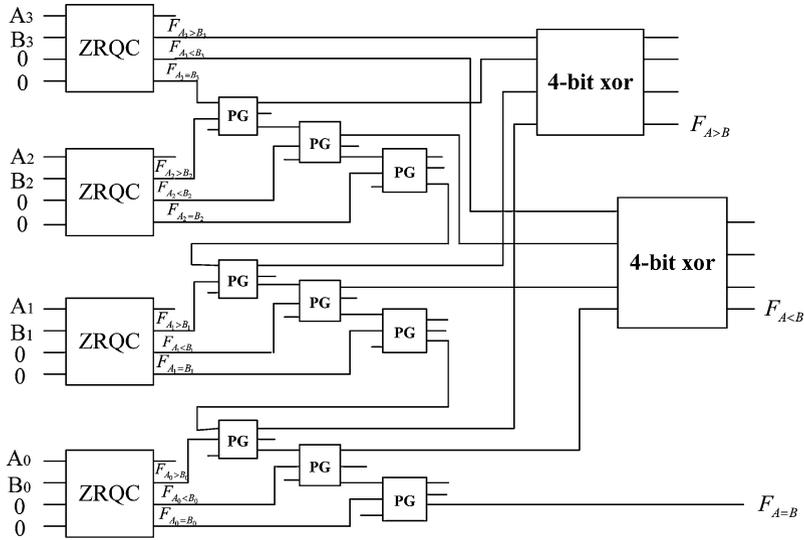
Fig. 12 A novel 4-bit reversible comparator
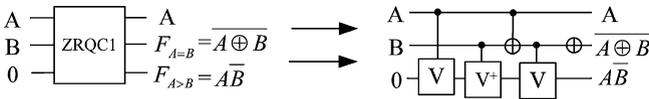
Fig. 13 The changed ZRQC module
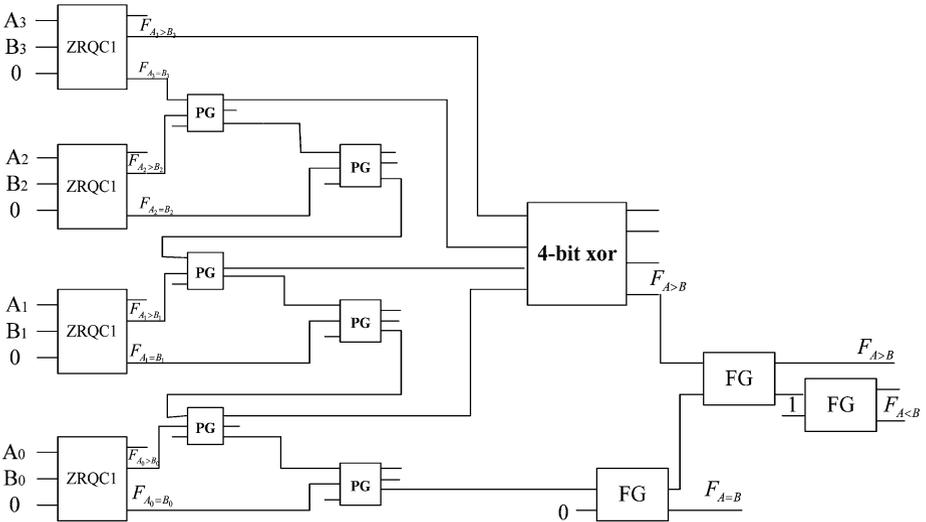
Fig. 14 The optimal 4-bit reversible comparator

of 4-bit reversible comparator is shown in Fig. 14 with the $F_{A<B}$ of 4-bit reversible binary comparator is cascaded connected by using two FG. The changed circuit is much better and optimal than the proposed circuit in Fig. 12 in terms of the number of quantum costs and garbage outputs. The correctness of proposed circuit will be tested and verified through MATLAB simulation software.

4 The Performance Analysis of the Proposed Circuit

4.1 The Performance Analysis of the Proposed Novel 1-Bit Reversible Comparator

The proposed ZRQ gate not only complements reversible adder and subtraction by only one, but also is cascaded to receive ZRQC module which can realize 1-bit reversible binary comparator. What's more, the proposed 1-bit reversible binary comparator can produce the least input constants, garbage outputs, unit delays with the optimal quantum costs. Meanwhile, this logic circuit is much better and optimal than researchers' counterparts in terms of input constants, garbage outputs, the number of kind of reversible gates, unit delays and quantum costs, those optimal designing will be convenient for the optimization of quantum reversible logic network. The performance of the proposed circuit can be comprehended easily with the help of the comparative results in Table 5.

In Ref. [13], five reversible gates of two FG, two NG and one NLG are in need, 6 input constants, 3 unit delays and 3 garbage outputs are produced apparently. The used NLG in Ref. [13] is a 2×2 reversible gate with complementing functions of NXOR, the quantum cost of which is yet to be calculated, so we show the detailed description of quantum equivalent circuit of NLG in Fig. 15 first ever. The quantum cost of NLG is 2 from Fig. 15 and the total quantum cost of Ref. [13] of 1-bit reversible comparator is 26.

Reference [10] proposed a lot of 1-bit reversible comparators, two of which are presented in this paper. The first 1-bit reversible comparator used three reversible gates of one FG, one PG and one BJNG which implemented the functions of OR gate with the same as the functions of MTG in Fig. 3, and produced 5 input constants, 3 unit delays, 10 quantum costs and 2 garbage outputs. The second 1-bit reversible comparator used four reversible gates of one FG, one BJNG and two TG, and produced 5 input constants, 4 unit delays, 16 quantum costs and 2 garbage outputs. Undoubtedly, Refs. [10, 13] used a large number of reversible gates, input constants, unit delays and produced a great many quantum costs and garbage outputs which increased the burden of quantum reversible network. And the increasing burden was an influence on performance of the entire circuit in the reversible

Table 5 The performance analysis of 1-bit reversible comparator

References	Quantum costs	Unit delays	Reversible gates	Input constants	Garbage outputs
Reference [13]	26	3	5	6	3
Circuit 1 of Reference [10]	10	3	3	5	2
Circuit 2 of Reference [10]	16	4	4	5	2
This paper	7	1	1	4	1

Fig. 15 Quantum equivalent circuit of NLG
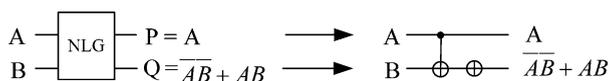
Fig. 16 A 3 × 3 1-bit reversible comparator
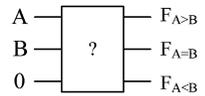
Table 6 The truth table of a 3 × 3 1-bit reversible comparator

A	B	$F_{A>B}$	$F_{A=B}$	$F_{A<B}$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

integrated circuit especially very large-scale reversible integrated circuit. Also imagine that if it was used in the design of quantum reversible network, such complex price will not be accepted in the design of quantum reversible network.

This paper proposes 1-bit reversible binary comparator which only produced 4 input constants, 1 unit delays, 7 quantum costs, 1 garbage outputs with one ZRQC module. Through comparison, it is obvious that the proposed 1-bit reversible comparator is optimal and brings much convenience for quantum reversible logic network.

4.2 The Least Standards Analysis of 1-Bit Reversible Comparator

As previous reversible logic criteria described, the biggest problem of reversible logic circuit designing is to have garbage outputs and input constants as minimum as possible. But so far the existing papers have not discussed the theoretical proof in detail to lower bound of garbage outputs and input constants of 1-bit reversible comparator. This paper will present the lower bound of garbage outputs and input instants of 1-bit reversible comparator from the view of logic analysis method point, and this lower bound explains that the proposed 1-bit reversible comparator is a reversible optimization circuit.

Theorem 1 1-*bit reversible binary comparator needs four inputs instants and one garbage output at least.*

Proof According to the logical expression with $F_{A>B}$, $F_{A=B}$ and $F_{A<B}$ of 1-bit reversible comparator and the reversible theory of one-to-one correspondence with inputs and outputs, 1-bit reversible comparator has three bit inputs and three bit outputs at least. We assume that 1-bit reversible comparator has only three bit inputs and three bit outputs, and when the third input set to 0 the 1-bit, then reversible comparator can be realized, shown in Fig. 16. The corresponding truth table of the comparator is shown in Table 6.

From the truth Table 6, when inputting is (0, 0, 0) and (1, 1, 0), the 1-bit reversible comparator will produce the same output (0, 1, 0) which obviously violate the reversible request of quantum reversible logic. That is to say, 1-bit reversible comparator with only three bit inputs and three bit outputs and no garbage outputs does not exist. We have to add one input and one output to modify the reversible circuit. So we have the theorem: 1-bit reversible binary comparator needs four inputs instants and one garbage output at least.   □

4.3 The Performance Analysis of the Proposed 4-Bit Reversible Comparator

This section will analyze the proposed 4-bit reversible binary comparator in the aspect of the number of reversible gates, input constants, unit delays, garbage outputs and quantum

Table 7 The performance analysis of 4-bit reversible comparator

References	Input constants	Quantum costs	Unit delays	Reversible gates	Garbage outputs
Reference [13]	59	311	13	53	23
Reference [12]	21	90	15	32	18
This paper	20	50	11	16	17
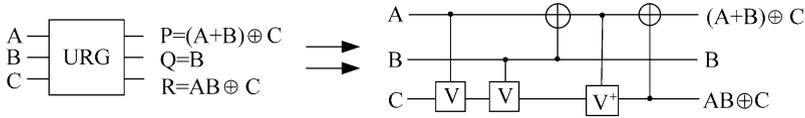
Fig. 17 Quantum equivalent circuit of URG

costs. References [12, 13] introduced the existing 4-bit reversible comparator and the corresponding truth Table 7 shows the comparative results of the three circuits.

In Ref. [13], in order to construct the quantum 4-bit reversible comparator, the researcher used 53 reversible gates, 59 input constants, 13 unit delays, 23 garbage outputs, and the quantum cost of the proposed URG gate [20] is yet to be calculated. This paper shows the detailed description of quantum equivalent circuit of URG gate according to the inputs and the outputs expression, shown in Fig. 17. Its quantum cost is 5, and the NLG mentioned above produces 2 quantum costs. So the quantum 4-bit reversible comparator of Refs. [13] produces 311 quantum costs.

In Ref. [12], the design of quantum 8-bit reversible comparator is proposed and the quantum 4-bit reversible comparator is not directly designed. However, according to the circuit design principle of 8-bit reversible comparator, it is easy to get the 4-bit reversible comparator consisted of three 2-bit R-comps and one R-O/P ckt. That paper proposed 18 quantum costs of 2-bit R-comp, but analyzing that quantum cost of the 2-bit R-comp circuit is 27 rather than 18. So 4-bit reversible comparator in Ref. [12] uses 32 reversible gates, 21 input constants, 15 unit delays, $27 \times 3 + 9 = 90$ quantum costs, produces 18 garbage outputs.

According to Fig. 14 in this paper, 4 ZRQC1 modules, 6 PG and 6 FG are needed to design the novel 4-bit reversible comparator. 4 ZRQC1 module produces 12 input constants, 1 unit delays, 4 garbage output, and uses $5 \times 4 = 20$ quantum costs; 6 PG produces 6 input constants, 9 garbage outputs, and uses $6 \times 4 = 24$ quantum costs; 3 FG complementing function of $F_{A<B}$ produces 2 input constants, 1 garbage output, and uses 3 quantum costs; 3 FG called for 4-bit XOR gate produces 0 input constants, 3 garbage outputs, and uses $1 \times 3 = 3$ quantum costs; 6 PG and 6 FG produce 10 unit delays. As a consequence, the novel 4-bit reversible comparator in this paper will use 20 input constants, 11 unit delays, 16 reversible gates, 50 quantum costs, and produces the total number of 17 garbage outputs. Because the primary concern is to keep numbers of input constants, unit delays, reversible gates, garbage outputs, and quantum costs as minimum as possible in the design of reversible 4-bit comparator, so the proposed 4-bit reversible comparator in this paper uses the minimum input constants, unit delays, reversible gates, garbage outputs and quantum costs compared to the comparator in Refs. [12, 13], and greatly increases performance and calculation speed of logic circuit.
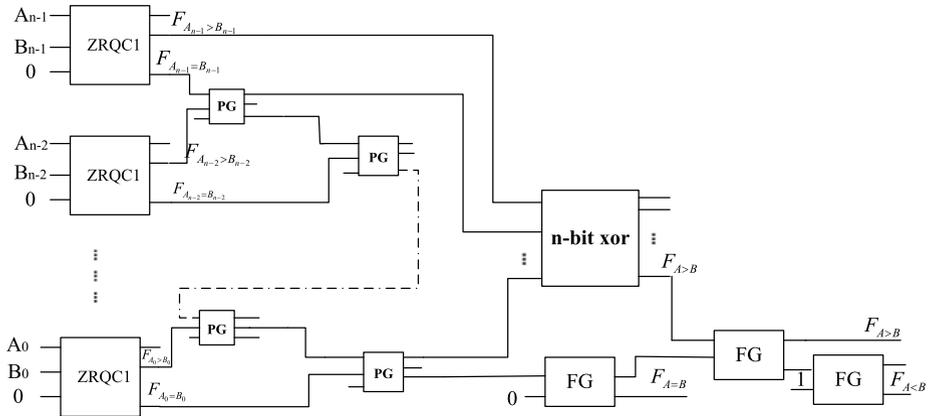
Fig. 18 *N*-bit reversible comparator

4.4 The Performance Analysis of *n*-Bit Reversible Comparator

N-bit reversible comparator cascading connection by the proposed ZRQC1 module and the basic gates is also proposed in this paper as shown in Fig. 18. The proposed *n*-bit reversible comparator consists of *n* ZRQC1 module, $2(n-1)$ PG and $n+2$ FG, the number of which is totally $4n$ and produces the number of $3n + 2(n-1) + 2 = 5n$ input constants, $1 + 2(n-1) + n - 1 - 2 + 3 = 3n - 1$ unit delays, $n + 3 \times (n-1) + (n-1) + 1 = 5n - 3$ garbage outputs and the number of $5n + 4 \times 2(n-1) + 1 \times (n+2) = 14n - 6$ quantum costs.

5 Test and Verify the Correctness of Proposed 4-Bit Reversible Comparator

This paper uses MATLAB simulation software to test and verify the correctness of proposed reversible comparator. MATLAB is released a high-tech computing environment in the face of scientific computing, visualization and interactive programming by the U.S mathworks. The numerical analysis, matrix computation, scientific data visualization, as well as nonlinear dynamic system modeling and simulation, and many other powerful features are integrated in the Windows environment which is easy to use in the MATLAB. It also provides a comprehensive solution for many scientific fields in scientific research, engineering design and the need for effective numerical calculation. MATLAB is largely out of the edit mode of the traditional non-interactive programming language (such as C, Fortran) and represents the advanced level of the international scientific computing software.

This section shows the performance of the proposed 4-bit reversible comparator by, MATLAB simulation and the realizing steps are as follows:

Step 1: Using MATLAB software to program the gates procedure which will be used in the main program to design the 4-bit reversible comparator. The code of ZRQC module of complementing 1-bit reversible comparator is detailed given as follows:

```
function zrqc=ZRQC(x) %ZRQC module

y=x;
```

```
[a,b]=size(x);

    if b==4

if
(y(1)=='0'||y(1)=='1')&&(y(2)=='0'||y(2)=='1')&&(y(3)=='0'||
y(3)=='1')&&(y(4)=='0'||y(4)=='1')        %Input to determine

    c=num2str($\sim$xor(str2num(y(1)),str2num(y(2))));

    d=num2str(xor(str2num(y(3)),and(str2num(y(1)),
            ~str2num(y(2)))));

    e=num2str(xor(str2num(y(4)),xor(str2num(y(3)),
            and(str2num(y(2)),~str2num(y(1))))));

    zrqc=[y(1) c d e];

    else

    disp('Please enter the four 0,1 character combinations')

    end

else

    disp('ZRQC module can not be the role of quantum states')

end
```

Step 2: With the combination of the design circuit of 4-bit reversible comparator in Fig. 14, we can function call the programming procedure of reversible gates as step 1 in main programming procedure of logic circuit. It is of great importance for the main programming procedure to assign binary numbers to each pin of reversible gates, and specify the connection relationship of each pin in order to connect the corresponding lower gates and higher gates. Finally, we can get the logical expression of 4-bit reversible comparator among $F_{A>B}$, $F_{A<B}$ and $F_{A=B}$.

Step 3: In order to test and verify the correctness of logic circuit, we randomly select 100 samples of 4-bit points to illustrate the comparing results of the proposed 4-bit reversible comparator in Fig. 19 and see that the design of the proposed circuit is a correct circuit. In Fig. 19, A and B present two 4-bit numbers respectively and each of them ranges from 0 to 15, the red square presents the result of $F_{A>B}$, the blue triangle presents the result of $F_{A=B}$, and the green criss-cross presents the result of $F_{A<B}$.

6 Conclusions and the Future Work

In this paper, the author proposes a new 4×4 reversible logic called ZRQ gate to build the reversible adder and subtraction, and also designs a ZRQC module of complementing 1-bit

Fig. 19 The comparing result of 4-bit reversible comparator by MATLAB
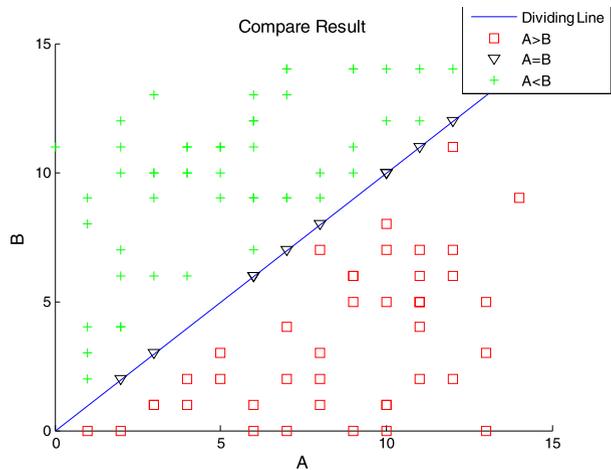
reversible comparator based on ZRQ gate. Besides, a novel 4-bit reversible comparator with least cost is also designed by using ZRQC module and the basic gates, and the comparative result shows that the proposed reversible comparator is more optimized in terms of the number of input constants, unit delays, reversible gates, garbage gates and quantum costs than the existing designs. What's more, MATLAB simulation software is used to test and verify the correctness of the proposed reversible comparator circuit. In the future work, we will focus on how to decrease the number of reversible gates and quantum costs in the design of reversible logic circuit. Moreover, we believe that the proposed reversible comparator will make a contribution to more complicated system, such as ALU of quantum CPU.

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