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Guest Editor's Introduction

This special issue is the second in a pair of issues devoted to the subject of Testing of Embedded Systems. The papers in this issue explore both hardware and software verification, as well as simulation-based validation and formal verification techniques.

The first paper discusses the verification approach incorporated into the Metropolis design framework for embedded systems. Metropolis enables system specification using their meta-model which includes formal property constraints. Formal verification is performed by automatically converting their meta-model into Promela and using the Spin verification tool. Simulation-based validation is performed by converting LTL properties into assertions to be used during simulation.

The second paper seeks to eliminate the need for explicit equivalence checking by defining a Model Algebra to describe the specification and a set of transformations to use for design. Each design transformation is proven to maintain functional equivalence. By using a broad set of transformations to perform design, the final implementation is guaranteed to be functionally equivalent to the original specification.

The third paper applies hardware equivalence checking techniques to embedded software. A formal representation of the software function is created using symbolic simulation to generate a set of symbolic expressions. Common data operations are represented as uninterpreted functions to manage verification complexity with little loss of precision.

The final paper in the issue presents a genetic algorithm to enhance the fault detection ability of existing test sequences used during simulation. The existing test sequences act as starting points for the algorithm. The algorithm can be configured to use a number of coverage metrics as its fitness function. Using existing sequences as a starting point effectively reduces the time needed to arrive at a final, high quality test sequence.

We hope that you find this special issue to be a useful guide to current research in the verification and validation of embedded systems.

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