




Wideband Phase-Compensated VGA with PMOS Switch in 40-nm CMOS for 120-GHz Band

Tae Hwan Jang^{1,2} · Seung Hun Kim² · Chul Woo Byeon³  · Chul Soon Park²

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Abstract

This paper presents a 120-GHz wideband phase-compensated variable gain amplifier (VGA) with a p-type metal–oxide–semiconductor (PMOS) switch using a 40-nm CMOS process. By applying a PMOS switch to the common source (CS) amplifier, the gain of the CS amplifier can be controlled by as much as 6.1 dB with 2° phase variations in 15.1-GHz bandwidth ranging from 100.9 to 115 GHz. The measured gain and 3-dB bandwidth of the VGA are 19.1 dB and 33.8 GHz for high-gain state, and 13 dB and 44.2 GHz for low gain state, respectively. Meanwhile, the DC power consumption in the high-gain state is 45 mW, and the OP1dB is −2.7 dBm.

Keywords CMOS · 120 GHz · Variable gain amplifier · PMOS

1 Introduction

Recently, wireless systems that use millimeter wave and sub-terahertz spectrum have rapidly evolved [1–3]. For these applications, a variable gain amplifier (VGA) is needed to improve the dynamic range. A VGA is also used as a main component of the vector-summing phase shifter [4, 5]. In addition, when a VGA is applied to a phased array for a beam-tapering function, the multi-path effect caused by the side lobe level (SLL) can be improved by

✉ Chul Woo Byeon
cwbyeon@wku.ac.kr

Tae Hwan Jang
th0617.jang@samsung.com

Seung Hun Kim
tmdgns901@kaist.ac.kr

¹ Nano Electronics Lab, Samsung Advanced Institute of Technology, Suwon, South Korea

² Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 34141, South Korea

³ Department of Electronic Engineering, Wonkwang University, Iksan 54538, South Korea

reducing the SLL [6]. Moreover, controlling the polarization of an antenna by installing a VGA on each port of a dual-polarized antenna can improve the signal-to-noise ratio of the receiver [7, 8]. In particular, in the case of a phase shifter, tapered beam former, and polarization control unit for high-speed communication, minimizing the phase variation is important to prevent distorted radiation pattern or poor cross-polarization.

For these applications, a VGA is typically realized using a cascode topology. For instance, gain-control mechanisms are implemented using a PMOS switch [9], current-splitting technique [10], a variable-transistor transconductance [11], and a current-steering technique [12–16]. The varactor control technique [17] is also applied to a cascode amplifier to achieve a variable-gain function. However, the cascode amplifier suffers from several drawbacks compared with a CS topology, including the following: (1) narrow bandwidth owing to the rapidly changing input/output impedance with frequency and (2) low linearity by assuming that the V_{DD} voltage is constant. Therefore, the CS topology is advantageous in this respect. However, CS VGAs, which exhibit wideband characteristics with minimized phase variation, have not been reported so far.

In this study, we demonstrate a wideband and compact 120-GHz phase-compensated VGA with a p-type metal–oxide–semiconductor (PMOS) switch. In sect. 2, analysis of the gain-control mechanism using the PMOS switch is presented. In sect. 3, the measurement results are provided, and the conclusion of this work is presented in sect. 4.

2 Phase-Compensated VGA with PMOS Switch

The 120-GHz VGA is designed for wireless chip-to-chip communication, and the detailed scenario is described in [18–20]. In the current work, the phase-compensated technique has been recently applied to CS VGA to obtain a flat gain in high gain (HG) and low gain (LG) modes and low phase variation.

Figure 1 shows the schematic of the 120-GHz VGA with a PMOS switch. The inter-stage matching network is designed with a single parallel inductor for low insertion loss. For the variable-gain function, the PMOS switch is installed parallel to the inductor from the 4th to the 8th stages. To prevent degradation of the noise figure of the overall amplifier, the PMOS switch is not connected from the 1st to the 3rd stages. The PMOS switches are connected in

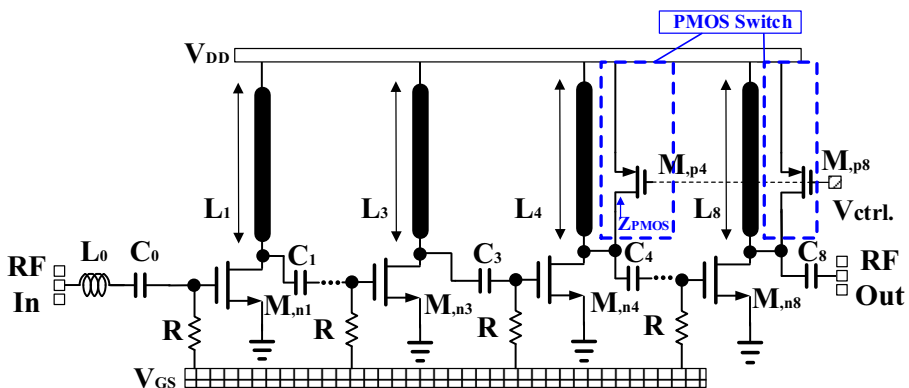


Fig. 1 Schematic of the 120 GHz VGA with PMOS switch

Table 1 Variables of the proposed 120 GHz VGA

Parameter	Value	Parameter	Value
L_0	80 pH	$M_{,n1} = M_{,n2} = \dots = M_{,n8}$	$1 \mu\text{m} \times 28$
L_1	37 pH	L_2	24 pH
L_3	38 pH	L_4	25 pH
L_5	26 pH	L_6	17.5 pH
L_7	38 pH	L_8	38 pH
C_0	690 fF	$C_1 = \dots = C_8$	200 fF
V_{GS}	0.52 V	V_{DD}	1 V
R	5 k Ω	$M_{,p4} = M_{,p5} = \dots = M_{,p8}$	$0.6 \mu\text{m} \times 7$
$V_{ctrl,on}(\text{low gain})$	0	$V_{ctrl,off}(\text{high gain})$	1

parallel to the inter-stage matching inductor. Meanwhile, the source is connected to the V_{DD} , and the drain is connected to the drain of the NMOS amplifier. By turning the PMOS switch on and off, the overall gain of the amplifier is controlled by adjusting the parallel resistance of the PMOS. The variables of the VGA are listed in Table 1. Figure 2 shows the schematic and equivalent circuit of the PMOS switch when the latter is turned on and off. The equivalent circuit can be modeled as a parallel resistor and parallel capacitor. When the switch is turned off, the switch operates as an open circuit. When the switch is turned on, the turn-on resistance (R_{on}) is considerably smaller than the turn-off resistance (R_{off}). The parallel resistance contributes to the reduction in the unit stage gain of the amplifier due to increment of the damping factor of the amplifier (ζ).

Table 2 lists the simulated real and imaginary impedances and calculated resistance and capacitance when the PMOS transistor is on and off at 120-GHz. R_{on} , R_{off} , C_{on} , and C_{off} are calculated as 186 Ω , 535 Ω , 3.5 fF, and 2.7 fF, respectively, where R_{on} is approximately three times smaller than R_{off} .

Generally, the gain of the n th-stage amplifier ($G_n(s)$) is expressed as follows:

$$G_n(s) = A_n \frac{\omega_n^2 s}{s^2 + 2\zeta_n \omega_n s + \omega_n^2} \tag{1}$$

where $s = j\omega$, $A_n = g_m L_n$, $\omega_n \left(= \sqrt{\frac{1}{L_n(C_{n,n+1} + C_{PMOS})}} \right)$ is the resonant frequency, and ζ_n is the damping factor. L_n and C_{PMOS} are inductance of the n th stage of the amplifier and parasitic capacitance of the PMOS switch, respectively. The damping factors in the HG and LG modes are given by

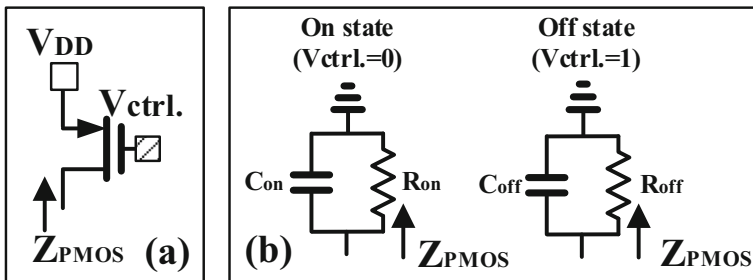


Fig. 2 a Schematic and b Equivalent circuit of the PMOS switch when the PMOS switch is tuned on and off ($Z_{PMOS}(s) = \frac{1}{sC_{on}} \parallel R_{on} = \frac{R_{on}}{1-j\omega C_{on}} R_{on}$)

Table 2 Simulated real and imaginary impedance and calculated resistance and capacitance when the PMOS transistor is on and off at 120 GHz

State	$R (\Omega)$	$C (fF)$
On	186	3.5
Off	535	2.7

$$\zeta_{n,HG} = \frac{1}{2R_{n,n+1} \parallel R_{off}} \sqrt{\frac{L_n}{C_{n,n+1} + C_{off}}} \tag{2}$$

$$\zeta_{n,LG} = \frac{1}{2R_{n,n+1} \parallel R_{on}} \sqrt{\frac{L_n}{C_{n,n+1} + C_{on}}} \tag{3}$$

where C_{off} and C_{on} is parasitic capacitance of the high-gain mode and low gain mode of the PMOS transistor, respectively. $R_{n,n+1}$ is equivalent resistance of the n th stage of the amplifier.

Fig. 3 Simulated **a** relative gain and **b** phase variation in the LG and HG modes for the 4th, 5th, 6th, 7th, and 8th stages

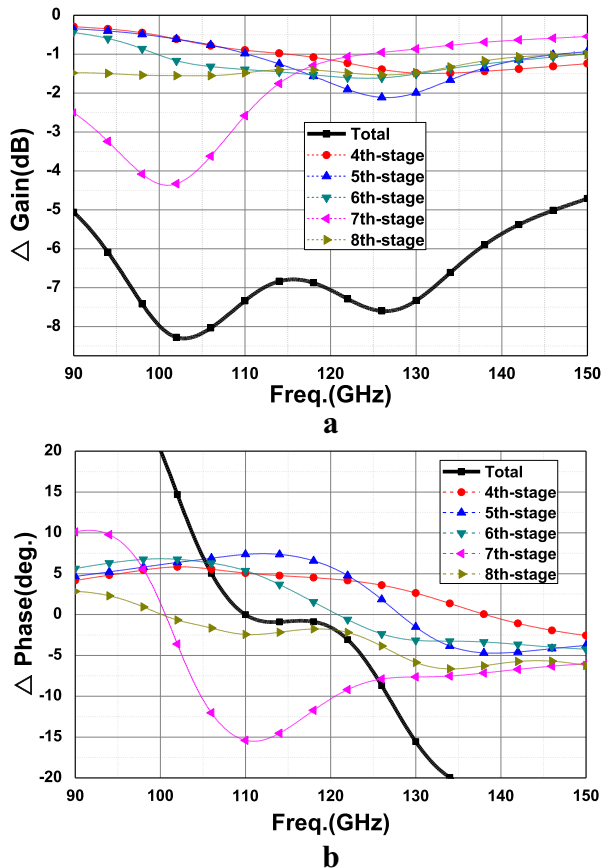
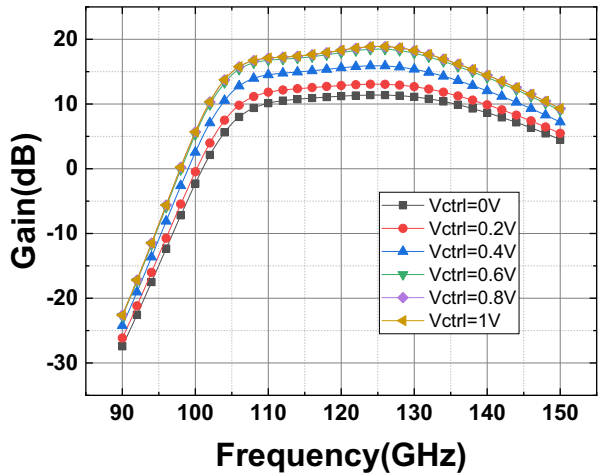


Fig. 4 Gain frequency response with continuous bias tuning

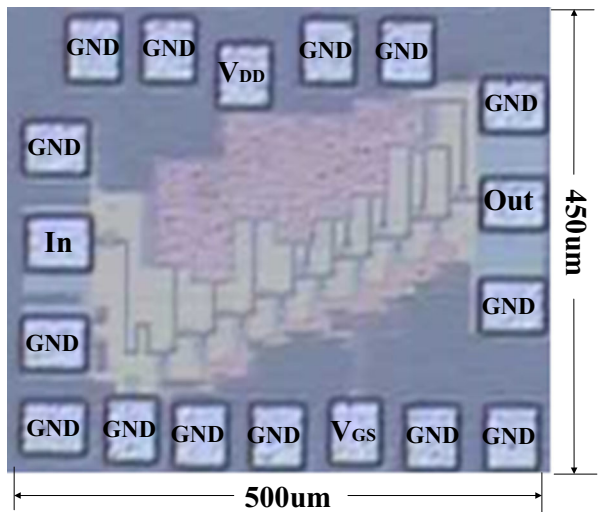


From Eqs. (1) to (3), the relative gain ($\frac{G_{n,LG}(s)}{G_{n,HG}(s)}$) of the n th stage is expressed as follows:

$$\frac{G_{n,LG}(s)}{G_{n,HG}(s)} = \frac{s^2 + 2\zeta_{n,LG}\omega_n s + \omega_n^2}{s^2 + 2\zeta_{n,HG}\omega_n s + \omega_n^2} \tag{4}$$

In the LG mode, the gain is dominantly reduced because $\zeta_{n,LG}$ is higher than $\zeta_{n,HG}$ due to the additional parallel resistance from the PMOS switch. Figure 3 shows the simulated relative gain and phase variation in the LG and HG modes in the 4th, 5th, 6th, 7th, and 8th stages. The relative gain and phase variation represent the gain and phase variation between the HG and LG modes, respectively. From Eq. (4), the relative gain at the n th stage at frequency ω_n is $\zeta_{n,LG}/\zeta_{n,HG}$ ($= 10\log(\zeta_{n,LG}/\zeta_{n,HG})$ dB). At $\omega_n \ll \omega$ and $\omega_n \gg \omega$, the relative gain converges to one ($= 0$ dB). Therefore, the relative gain at the n th stage monotonically decreases from the DC frequency and monotonically increases after ω_n . The VGA is designed to have a flat gain in the

Fig. 5 Chip micrograph of the proposed amplifier



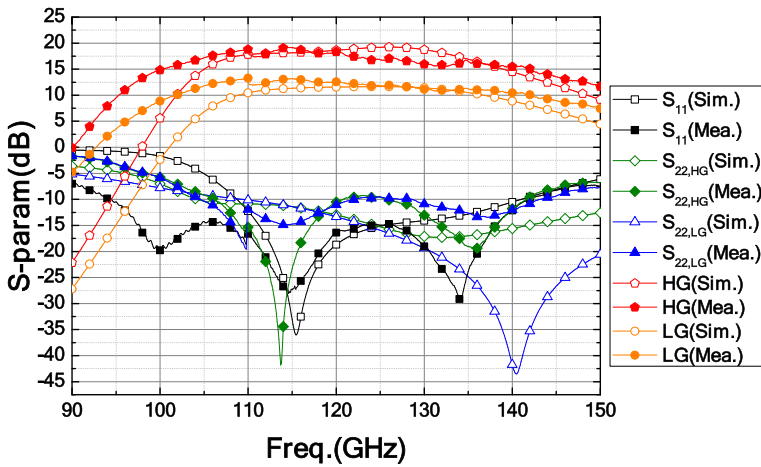


Fig. 6 S_{11} , S_{22} , and gain of the proposed amplifier

LG and HG modes by setting the gain-variation stage at low and high frequencies. From Eq. (4), when ω is substituted to $\omega_n + \Delta\omega_n$, the phase variation in the n th stage ($\Delta\theta_n$) is given as

$$\Delta\theta_n \sim \tan^{-1} \left(\frac{(-\omega_n \Delta\omega_n)}{\zeta_{n,LG}(\omega_n^2 + 2\omega_n \Delta\omega_n)} \right) - \tan^{-1} \left(\frac{(-\omega_n \Delta\omega_n)}{\zeta_{n,HG}(\omega_n^2 + 2\omega_n \Delta\omega_n)} \right) \quad (5)$$

Equation (5) shows that, if $\Delta\omega_n$ is negative, $\Delta\theta_n$ is positive. In contrast, if $\Delta\omega_n$ is positive, $\Delta\theta_n$ is negative. In the 7th and 8th stages, because the center frequency of 120 GHz is larger than the resonating frequency in the seventh stage, $\Delta\omega_7$ and $\Delta\omega_8$ are positive, and $\Delta\theta_7$ and $\Delta\theta_8$ are negative. On the other hand, $\Delta\theta_4$, $\Delta\theta_5$, and $\Delta\theta_6$ are positive. In this manner, the VGA is designed by applying the phase-compensated technique so that the phase variation approaches zero near the center frequency.

Fig. 7 Simulated and measured P1dB in high- and low-gain states of the proposed VGA

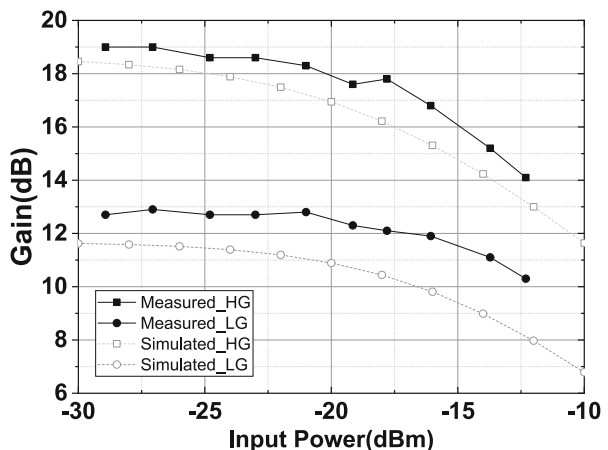


Fig. 8 Simulated and measured phase difference of the proposed VGA

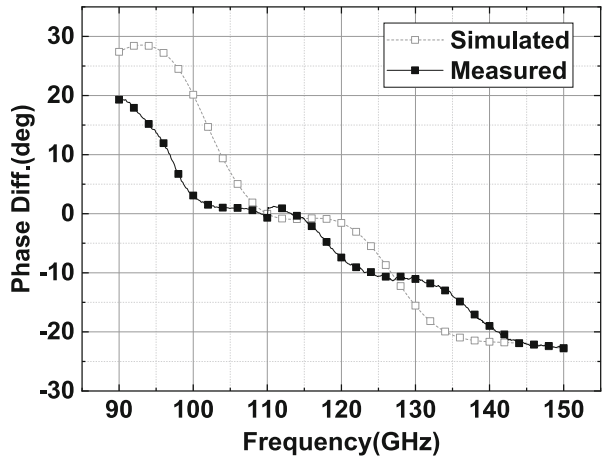


Figure 4 shows gain frequency response with continuous bias tuning. It is shown that gain is continuously controlled by tuning the control bias voltage. In this work, only two states ($V_{\text{ctrl}} = 1$ and $V_{\text{ctrl}} = 0$) are measured to be applied for polarization control unit.

3 Measurement Results

Figure 5 shows the fabricated 120-GHz VGA. The amplifier is fabricated using the 40-nm CMOS process. The addition of the PMOS switches does not affect the total chip area, and the total chip area is $450 \mu\text{m} \times 500 \mu\text{m}$. The total DC power consumption of the amplifier is 45 mW. Figure 6 shows the S_{11} , S_{22} , and gain of the amplifier. The measured S_{11} is less than -9 dB from 104.9 to 136.2 GHz, whereas the measured S_{22} is less than -9 dB from 93.3 to 141.4 GHz. Furthermore, the measured peak gains are 19.1 dB in the HG state and 13 dB in the LG state. The 3-dB gain bandwidths are 33.8 GHz in the HG state and 40.2 GHz in the LG state. The discontinuity at 110 GHz occurs because the S -parameter from 90 to 150 GHz is measured

Fig. 9 Simulated and measured group delay in the high- and low-gain states of the proposed VGA

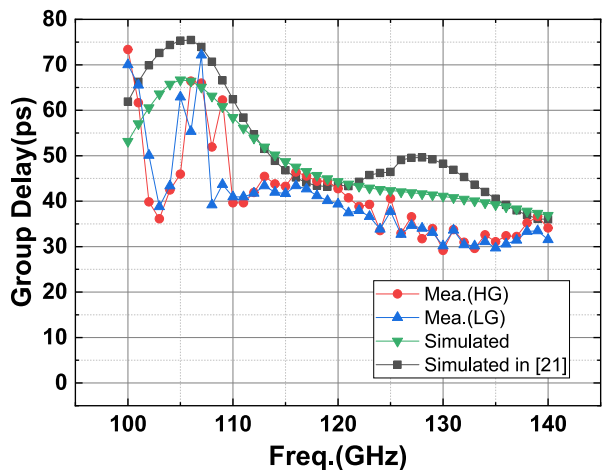
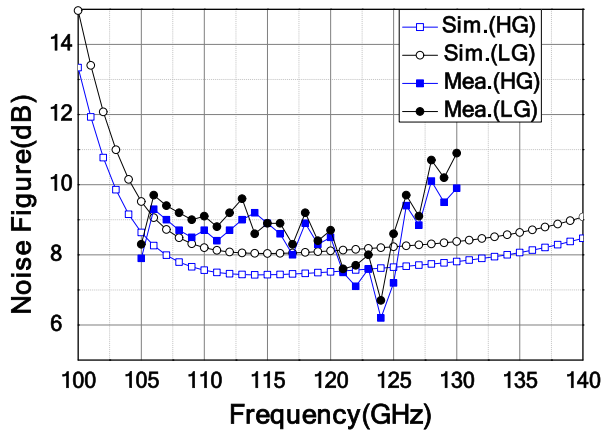


Fig. 10 Simulated and measured noise figure in the high- and low-gain states of the proposed VGA



by a W-band (from 90 to 110 GHz) and D-band (from 110 to 150 GHz) vector network analyzer (VNA). Figure 7 shows the simulated and measured P1dB for the HG and LG states of the VGA. For the HG and LG states, the OP1dB values are -2.7 and -2.6 dBm, respectively. Figure 8 shows the simulated and measured phase difference of the VGA. The phase variation of the amplifier is 15.5° within the 3-dB-gain bandwidth (102.9–136.7 GHz). If the VGA is applied to polarization control unit [9], the cross-polarization could be lower than at least -11.46 dB with 15.5° phase variation. Moreover, the measured phase variation is less than 2° in the 15.1-GHz frequency band that ranges from 100.9 to 115 GHz by implementing the phase-compensated technique. Figure 9 shows the simulated and measured group delay in the HG and LG states. The similar group delay characteristics are revealed compared to [21], and measured group delay is lower than 50 ps. Figure 10 shows the simulated and measured noise figures in the HG and LG states. The measured average noise figures are 8.5 and 8.9 dB in the HG and LG modes, respectively. Figure 11 shows the simulated IIP3 values of the HG and LG states. The simulated IIP3 values are -17.5 and dB -13.9 dB in the HG and LG modes, respectively. Table 3 lists the performance of the CMOS VGAs in the millimeter-wave frequencies. The CS amplifier with a PMOS switch exhibits the

Fig. 11 Simulated IIP3 in the high- and low-gain states of the proposed VGA. The IIP3 is simulated for 5-GHz offset

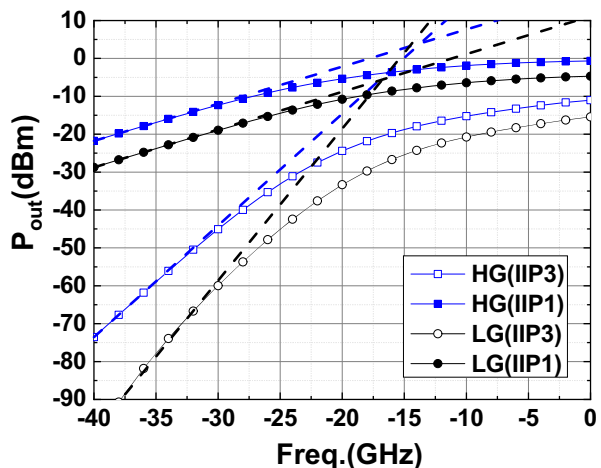


Table 3 Reported CMOS VGAs for the millimeter-wave frequencies

Ref.	Tech	f_c (GHz)	Gain (dB)	3-dB BW (GHz)	Pdc (mW)	OP1dB (dBm)	IP3 (dBm)	Phase Var. (°)	NF (dB)	Group delay (ps)	Area (mm ²)
[14]*	90 nm	73.5	14 dB (HG)/-26dB (LG)	5	22	N/A	N/A	N/A	N/A	N/A	0.726
[15]*	90 nm	78.1	23 (HG)/4.6 (LG)	18.8	55	0.2	N/A	N/A	5.3	N/A	0.5727
[16]*	90 nm	59	22 (HG)/-18 (LG)	10	26	0	-19 (HG)/3 (LG)	N/A	4.8 (HG)/18 (LG)	N/A	0.63
[17]	130 nm	61.5	13 (HG)/5 (LG)	7	N/A	N/A	N/A	5°	6.8	N/A	0.45
This work	40 nm	121.9	19.1 (HG)/13 (LG)	33.8 (HG) 40.2 (LG)	45 (HG/LG)	-2.7(HG) -2.62(LG)	-13.9(HG)/-17.5(LG)	15.5***/20***	8.5 (HG)/8.9 (LG)	<50ps	0.225

*Continuous gain tuning

**For 3-dB bandwidth (102.9–136.7 GHz)

***For 15.1-GHz bandwidth (100.9–115 GHz)

widest bandwidth than the other reported VGAs owing to the application of the CS topology. The presented VGA is advantageous for system integration because it uses a relatively small area compared with the number of stages.

4 Conclusion

A wideband 120-GHz phase-compensated VGA with a PMOS switch is presented. The measured gain and 3-dB bandwidth of the VGA are 19.1 dB and 33.8 GHz, respectively, while consuming DC power of 45 mW in the HG state. The OP1dB is -2.7 dBm, and the phase variation between the HG and LG states are 15.5° and 2° in the 3-dB gain bandwidth and 15.1-GHz frequency band, respectively.

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