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MEMS Slow-Wave CPW Phase Shifter for mm-Wave Applications

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Abstract
MEMS-based phase shifters show the best performance in terms of figure of merit, but their footprints are usually large and it is difficult to achieve several bits. This paper demonstrates a miniaturized phase shifter based on slow-wave CPW and MEMS that occupy 0.47 mm^2. A total phase shift of 152° was obtained with a maximum insertion loss of 3 dB, resulting in a figure of merit of 50°/dB at 60 GHz. The 3-bit device showed an insertion loss variation of 1.3 dB and return loss better than 13 dB. The pull-in and pull-out voltages were measured to be 17 V and 10 V, respectively. The presented device is well suited for mm-wave phased array applications. Thanks to the proposed concept, more bits could be easily achieved and much higher frequencies could be addressed.

Keywords Millimeter wave integrated circuits · Passive circuits · Phase shifters · RF-MEMS

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1 Introduction

Several consumer applications such as 5 G, wireless personal area networks, wireless high-definition video distribution, point-to-point links, automotive radars, and wireless sensor networks require improved capabilities of wireless signal transmission, including extremely high data rate, increased security, reduced electromagnetic interference, extreme miniaturization, and low power consumption. Due to the congested aspect of the low microwave frequency bands, and to achieve better resolution, these applications are moving to a significantly higher region of the frequency spectrum, at the mm-wave range.

To achieve longer communication range with mobile terminals or sensors, many mm-wave developments require phased arrays with beam-steering/forming capabilities. When dealing with low-power consumption and high-performance systems, for instance applications needing mobility, these phased arrays must be based on the development of passive phase shifters, which constitutes a major challenge.

Several technologies have been used to develop passive phase shifters at mm-waves, including CMOS/BiCMOS, ferroelectric, namely BST, liquid crystal, and MEMS. A brief state-of-the-art shows that most of the phase shifters demonstrated so far either exhibit unacceptable insertion loss or occupy large area. However, a careful comparison of phase shifters realized in all these technologies is not simple, since one has to take into account not only the size and the electrical performance, but also the cost, the reliability, and, especially for MEMS, the packaging challenge. The classical figure of merit (FoM) to compare phase shifter performance is defined by the ratio of the maximum phase shift over the maximum insertion loss. In this paper, a second figure of merit (FoM_2) is defined giving an idea of the trade-off between electrical performance and size. In order to maintain FoM_2 constant for phase shifters of different lengths realized in a given technology, the absolute variation of the electrical length ($\Delta\phi$) multiplies the classic figure of merit. Therefore, FoM_2 is defined as the $\Delta\phi \times$ FOM/area and is expressed in $(\text{degree})^2/(\text{dB/cm}^2)$.

In general, MEMS-based phase shifters show the best electrical performance, but their footprint is quite large. The 2-bit phase shifter presented in [1] is based on a switched line topology implemented on quartz substrate using SP4T MEMS switches. This device shows a high FoM of 90°/dB, but its footprint is large (4 mm^2), leading to a small FoM_2 of 60. Moreover, due to the topology of this phase shifter, a higher resolution would lead to a more complex MEMS switch and a considerable increase in area. Loaded line topology leads to the realization of phase shifters with higher resolution, as demonstrated by the 4-bit MEMS-based phase shifter presented in [2]. The high-performance MEMS switches and the quartz substrate used in this device also lead to a high FoM of 93°/dB; however, the occupied area is equal to 11.85 mm^2, also leading to a small FoM_2 of 25 that can be prohibitive for many applications needing large phased arrays. This large area can be explained by the use of a classical topology, where large MEMS are loading a CPW, resulting in both long and wide devices.

Contrary to MEMS phase shifters, their CMOS/BiCMOS counterparts offer much smaller footprint, but their electrical performance is poor, since the MOS-based varactors and switches used as tuning elements exhibit quality factors limited to about 10 to 15 at mm-waves [3]. In [4], a reflection-type phase shifter (RTPS) was realized in a 90-nm CMOS technology. Its area is only 0.075 mm^2, but the FoM is limited to 11°/dB, due to the poor quality factor of the MOS varactors, as mentioned above. However, the reduced area yields to a high FoM_2 of 128. More recently, a wideband (56–64 GHz) RTPS realized in 65-nm CMOS technology, still using MOS varactors, showed a slightly better FoM, equal to 13°/dB [5]. The wideband was

obtained thanks to the use of a coupled-line coupler instead of a hybrid coupler that is commonly used. The footprint is only 0.034 mm^2, leading to a very high FoM_2 of 345.

Loaded slow-wave transmission lines were used in a 32-nm SOI CMOS technology in [6], achieving a FoM of 24.6°/dB and an area of 0.073 mm^2 (FoM_2 = 591). In [7], a RTPS developed in 0.13-μm SiGe BiCMOS technology used slow-wave coupled lines for the hybrid-coupler and presents a FoM of 25.2°/dB and an area of 0.33 mm^2 (FoM_2 = 119). In both cases, the FoM_2 is high and the slow-wave transmission lines showed some improvement of the FoM, but the insertion loss above 6 dB is still too high.

A RTPS with MEMS using CMOS technology Back-End-Of-Line was presented in [8] avoiding the use of MOS varactors to reach a higher FoM of 45°/dB. Only three phase states were possible in the phase shifter. It uses a small-footprint coupler; however, the large comb-like MEMS varactors result in a large surface (1.04 mm^2) when compared to the MOS varactor-based phase shifters. The result is a moderate FoM_2 of 62. Apart the cost issue due to the device size along with the phase states issue, the latter example clearly illustrates the trade-off between size and electrical performance.

Phase shifters based on either barium strontium titanate (BST) or liquid crystal (LC) were also reported in the literature. In general, BST-based devices show good electrical performance at RF frequencies. For instance, a high FoM of 85°/dB was obtained at 30 GHz in [9]. However, the BST loss tangent increase with frequency dramatically limits the phase shifter's electrical performance at mm-waves. At 60 GHz, a much lower FoM of 23°/dB with a footprint of 1.2 mm^2 was reported in [10], leading to a limited FoM_2 of 32.

LC-based phase shifters show high FoM at higher frequencies, since LC loss tangent decreases with frequency [11]. A FoM of 42°/dB at 76 GHz was reported in [12]. However, due to the moderate variation of the dielectric constant of the LC, the area of LC phase shifters is usually large. In [12], the area of the loaded line phase shifter is 0.65 mm^2, leading to a FoM_2 of 59. The switching time is also quite slow, i.e., few ms, thus limiting the application field. To solve these issues, in [13], a slow-wave CPW (S-CPW) was combined with MEMS and LC to take advantage of their high FoM, while reducing the size and response time of the phase shifter. A FoM of 52°/dB at 45 GHz with a 0.38 mm^2 footprint was obtained, thus resulting in a high FoM_2 of 369. However, despite the good performance of this phase shifter, the encapsulation of LC and MEMS could be complicated and increase costs.

The MEMS phase shifter concept presented in [14] proposes a topology where the MEMS are part of an S-CPW [15]. The benefit of using S-CPW for the implementation of phase shifters is twofold: the performance is not dependent on substrate conductivity as shown in [16]; hence, silicon technologies can be used, and the inherent slow-wave effect leads to compact devices and high-quality factor. The MEMS S-CPW approach leads to more compact devices compared to a periodically loaded line approach [2], and still presents high electrical performance. This concept was also demonstrated in [17] using CMOS 0.35-μm technology. The fabricated 2-bit MEMS phase shifter resulted in a 36°/dB FoM and an area of 0.58 mm^2, thus leading to a FoM_2 of 16.

A similar concept was used in [6], in which FET switches were used to control the equivalent distributed capacitances and inductances, changing the phase velocity, while maintaining the characteristic impedance unchanged.

This paper presents a MEMS S-CPW phase shifter using the basic concept proposed in [14, 17–19]. The phase shifter is based on an S-CPW with movable floating ribbons and can be considered as a multi-section MEMS tuned transmission line. Even if the concept was proposed in [14] and [17–19], many improvements were carried out in the present paper,

leading to a more mature and practical device. A multi-state phase shifter was achieved, thanks to the use of several DC commands, leading to a 3-bits phase shifter. A dedicated MEMS technology [20] was used, which allowed a higher degree of freedom in the design, as compared to the CMOS technology used in [17]. Also, the design was done thanks to the use of the analytical model presented in [21], which dramatically decreases the simulation time, allowing a much faster optimization of the whole structure with several DC commands. Thanks to this optimization, the MEMS S-CPW phase shifter was properly designed, leading to a higher FoM along with a larger FoM_2.

Moreover, the design methodology is carefully described in the present paper, which was not the case in [14, 17], since much simpler designs had been carried out. In Sect. 2, the phase shifter principle and fabrication process are presented. Next, the phase shifter design is detailed in Sect. 3. Results are presented in Sect. 4. Finally, the paper is concluded in Sect. 5.

2 MEMS S-CPW Principle and Technology

2.1 Principle

The principle of the MEMS S-CPW phase shifter is illustrated in Fig. 1. As explained in [14, 17], Au floating ribbons are actuated above a CPW, thus forming a tunable S-CPW with tunable propagation characteristics. In general, electrostatically actuated microstructures, such as the shielding ribbons, can be displaced continuously from rest up to two-thirds of the spacing between them and the CPW strips (h in Fig. 1, in this case) by controlling the applied DC voltage. It is well known that this is not an adequate approach because the position of the shielding ribbons would be highly sensitive to the fabrication process variations, leading to unpredictable behavior with major reliability issues.

The voltage required for the shielding ribbons to move the final one-third of the spacing is known as the pull-in voltage, at which it will collapse onto the CPW strips. The pull-in voltage might change due to process variation, but the position of the shielding ribbons will be predictable. For this reason, in the proposed MEMS S-CPW phase shifter, the shielding ribbons were actuated digitally between rest and pull-in, not continuously. In [12], this principle was used to achieve a 1-bit device. In this paper, besides the fact that a more mature MEMS technology illustrated in Fig. 1 was used, the principle demonstrated in [12] was

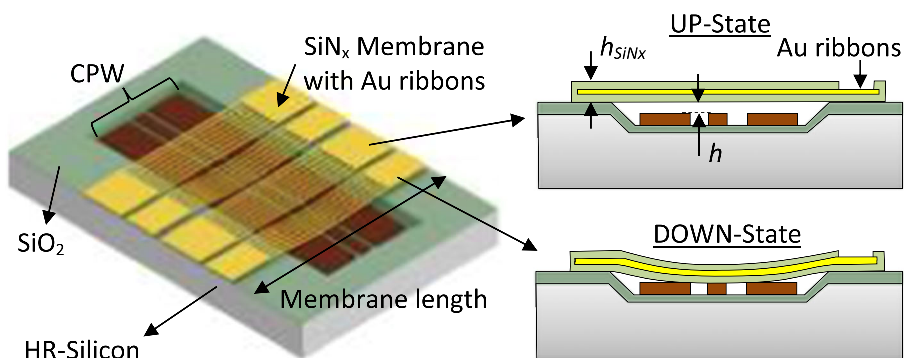

Fig. 1 RF MEMS technology used for the MEMS S-CPW phase shifter

extended to achieve a multi-state phase shifter, the design of the new MEMS S-CPW phase shifter being described in Sect. 3.

In the technology used in this paper, the floating ribbons of the S-CPW (placed orthogonally to the direction of propagation) were placed above the CPW strips. They are normally placed below the CPW strips in CMOS/BiCMOS technologies because these are fabricated on the uppermost metallic layer, which is normally the thickest one. Whatever their relative position is, the shielding ribbons capacitively load the CPW, while the magnetic field is practically unperturbed. This leads to a slow-wave effect, which is particularly interesting for the development of phase shifters because it reduces their size and increases their FoM. In this sense, it is comparable to the traditional distributed MEMS transmission line (DMTL) phase shifters, where a tunable element (RF MEMS switch) periodically loads a transmission line. The great advantage of the proposed approach is the distributed aspect of the MEMS. It is no longer a transmission line loaded with elementary cells for tuning, as it is a DMTL illustrated in Fig. 2, but rather a fully distributed-MEMS transmission line with tuning of the electrical length by simply modifying the height between the CPW strips and the floating ribbons. Therefore, in the case of the present paper, the S-CPW itself is a MEMS.

In S-CPWs, the electric field is confined between the shielding ribbons and the CPW strips, and their distance essentially controls the capacitance per unit length (C). By releasing the shielding ribbons, as suggested in [14], it is possible to move them with the application of a DC voltage between the CPW strips and themselves. The developed electrostatic force pushes the shielding ribbons closer to the CPW strips, reducing the phase velocity and increasing the phase shift, becoming a MEMS S-CPW phase shifter.

2.2 Technology

The proposed MEMS phase shifter was fabricated using a dedicated RF MEMS process (from CEA-LETI, France) to overcome the MEMS release issues encountered in [17]. Figure 1 shows an illustration of the technology used for the device fabrication.

The gold CPW strips are formed at the bottom of a cavity and separated from the high resistivity silicon substrate by a silicon dioxide (SiO_2) layer. The gold shielding ribbons are sandwiched between two silicon nitride (SiN_x) layers that form a stress-compensated suspended membrane. Even though high resistivity silicon was used, it is not required to

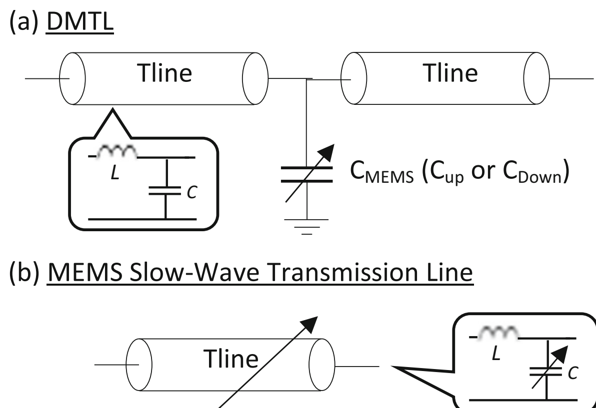

Fig. 2 **a** Elementary cell of the classic DMTL phase shifter and **b** the proposed MEMS slow wave transmission line

reduce losses, since the electric field is confined between the CPW strips and the shielding ribbons, as indicated in [16]. Table 1 gives the dimensions used in the design of the MEMS phase shifter, as well as the fabricated ones. *W*, *Wg*, and *S* are the width of the CPW signal and ground strips, and CPW gap, respectively. *SS* and *SL* are the shielding ribbons gap and width, respectively. The other dimensions are the thicknesses defined in Fig. 1.

3 MEMS S-CPW Phase Shifter Design

3.1 Mechanical Design

The mechanical design of the SiN_x membranes with the shielding layer ribbons was based on the reliable mechanical design of the CEA-Leti RF MEMS switch [20].

The length of all the membranes, L_{mem}, was fixed at 320 μm and the membranes' thickness (h_{SiNx}) at 1 μm to allow a reasonably large spring constant to avoid stiction after pull-in. Because the width of each membrane depends on the electrical design, the spring constant varies for each other, as it will be explained below. In the final design, membranes with widths varying from 15 to 30 μm were analyzed, which results in a spring constant, *k*, varying from 40 to 80 N/m, considering the approximation of an evenly distributed load along the membrane and a tensile stress of 150 MPa. This intrinsic stress contributes to increase the spring constant as described in [20].

The CPW ground strips are also used as DC electrodes to actuate the membrane. For this reason, it is desired to design wide ground strips placed as close as possible to the center of the membrane, to reduce the pull-in voltage. Thus, it requires a small CPW width, *D*, given by equation (1).

$$D = W + 2S. \quad (1)$$

Here, there is a compromise between the pull-in voltage and *Q*-factor of the S-CPW. In general, larger *D* yields higher S-CPW *Q*-factors. $D = 41$ μm was chosen, which results, as shown below, in a *Q*-factor of 20. The pull-in voltage, V_p, was calculated by analytical formulas, at first, using a simplified approach considering an evenly distributed load along the membrane, resulting in 25 V. The electro-mechanical simulations presented in this paper were performed in ANSYS Multiphysics using the fabricated dimensions of the structure to predict a more realistic behavior of the MEMS.

Table 1 Designed and fabricated dimensions

	Designed (μm)	Fabricated (μm)
W	5	4
W_g	54.5	53.5
S	18	19
SS	2	2.15
SL	1	0.85
h	1.2	1.2
h_{SiNx}	1	1.1
Ribbons thickness	0.2	0.24
CPW Strips thickness	1	1.1
SiO_2 thickness	2	2.3

3.2 Electrical Design

The S-CPW was designed following the electrical model presented in [21]. This is very important for the optimization of the MEMS phase shifter, since it allows a fast calculation and analysis of the characteristic impedance, dielectric constant, and *Q*-factor of the S-CPW as a function of its geometry (CPW strips and gap widths). The phase shift in a MEMS-tunable S-CPW, $\Delta\theta$ in radians, can be defined as shown in equation (2).

$$\Delta\theta(\mathrm{rad}) = \Delta\beta \times l = \frac{\omega}{C_0} \times \left(\sqrt{\varepsilon_{\mathrm{reffmax}}} - \sqrt{\varepsilon_{\mathrm{reffmin}}}\right) \times l, \tag{2}$$

with $\varepsilon_{\mathrm{reffmax}}$ and $\varepsilon_{\mathrm{reffmin}}$ the maximum and minimum effective dielectric constants in the DOWN and UP states, respectively, ω the angular frequency, l the phase shifter physical length, and c_0 the speed of light in vacuum. $\Delta\beta = \beta_{\max} - \beta_{\min}$ is the differential S-CPW propagation constant between DOWN ($\beta_{\max}$) and UP ($\beta_{\min}$) states illustrated in Fig. 1. The DOWN state corresponds to the state when all the ribbons on the shielding layer are actuated, collapsed onto the CPW strips. At this state, the S-CPW has a higher capacitance and the propagation constant is greater. At the UP state, the ribbons are at rest and the propagation constant is smaller.

The design results from a trade-off between the insertion loss relative to the *Q*-factor of the S-CPW, called IL_{Q}, and that coming from the S-CPW mismatch, called IL_{Γ}. The maximum insertion loss IL_{Qmax} and $IL_{\Gamma\ \max}$ can be used to derive, as shown in equation (3), two different figures of merit, FoM_{Q} and FoM_{Γ}, that will be used to explain the design trade-off. The total figure of merit, $FoM_{\mathrm{Q}+\Gamma}$, considers both insertion loss sources.

$$FoM_{\mathrm{Q}} = \frac{\Delta\theta}{IL_{\mathrm{Qmax}}(\mathrm{dB})} \text{ and } FoM_{\Gamma} = \frac{\Delta\theta}{IL_{\Gamma\ \max}(\mathrm{dB})}$$
$$FoM_{\mathrm{Q}+\Gamma} = \frac{\Delta\theta}{IL_{\mathrm{Qmax}}(\mathrm{dB}) + IL_{\Gamma\ \max}(\mathrm{dB})} \tag{3}$$

Regarding FoM_{Q}, $IL_{\mathrm{Q\ max}}$ can be defined from the S-CPW *Q*-factor:

$$Q = \frac{1}{2}\frac{\beta_{\max}}{\alpha_{\max}(\mathrm{Np/m})} = \frac{1}{2}\frac{\beta_{\max} \times l}{\alpha_{\max}(\mathrm{Np}/m) \times l} = \frac{\frac{\omega}{C_0}\sqrt{\varepsilon_{\mathrm{reffmax}}}}{2\, IL_{\mathrm{Q\ max}}(\mathrm{Np})} \times l \tag{4}$$

leading to

$$IL_{\mathrm{Q\ max}}(\mathrm{dB}) = 4.34 \times \frac{\frac{\omega}{C_0}\sqrt{\varepsilon_{\mathrm{reffmax}}}}{Q} \times l, \tag{5}$$

where $\alpha_{\max}(\mathrm{Np}/m)$ is the attenuation constant in Nepers per unit length for the DOWN state and l the physical length of the S-CPW. From equations (2), (3), and (5), the FoM_{Q} converted to °/dB can be derived as

$$FoM_{\mathrm{Q}}(^\circ/\mathrm{dB}) = 13.2 \times Q \times \left(1 - \sqrt{\frac{\varepsilon_{\mathrm{reffmin}}}{\varepsilon_{\mathrm{reffmax}}}}\right) \tag{6}$$

From equation (6), it can be seen that the FoM_Q increases when the ratio between $\varepsilon_{\mathrm{reffmax}}$ and $\varepsilon_{\mathrm{reffmin}}$ increases. The best case would be when this ratio is negligible compared to unity, then the FoM_Q is simply given by $13.2 \times Q$. Moreover, the physical length l, derived from equation (2) and given in equation (7), decreases if $\varepsilon_{\mathrm{reffmin}}$ decreases with $\varepsilon_{\mathrm{reffmax}}$ considered as constant, which is necessarily the case, as shown later in this paper.

$$l = \frac{\Delta\theta}{\frac{\omega}{C_0} \times \left(\sqrt{\varepsilon_{\mathrm{reffmax}}} - \sqrt{\varepsilon_{\mathrm{reffmin}}}\right)} \tag{7}$$

Hence, it can be concluded from this simple analysis that the difference between $\varepsilon_{\mathrm{reffmax}}$ and $\varepsilon_{\mathrm{reffmin}}$ must be maximized to (i) increase the FoM_Q and (ii) decrease the physical length.

However, increasing the ratio between $\varepsilon_{\mathrm{reffmax}}$ and $\varepsilon_{\mathrm{reffmin}}$ leads to the increase of the minimum and maximum characteristic impedance of the tunable S-CPW for DOWN and UP states, called $Z_{\min}$ and $Z_{\max}$, respectively. Therefore, the mismatch is accentuated, increasing the return loss, which is assessed by the second proposed FoM_Γ. The characteristic impedance of DOWN and UP states can be considered inversely proportional to the dielectric constant, as shown in equation (8).

$$Z_{\min} \propto \frac{1}{\sqrt{\varepsilon_{\mathrm{reffmax}}}} \text{ and } Z_{\max} \propto \frac{1}{\sqrt{\varepsilon_{\mathrm{reffmin}}}} \tag{8}$$

The input/output reflection coefficient can be defined for the DOWN and UP states, respectively, as equation (9):

$$\Gamma_{\mathrm{DOWN}} = \frac{Z_0 - Z_{\max}}{Z_0 + Z_{\max}} \text{ and } \Gamma_{\mathrm{UP}} = \frac{Z_0 - Z_{\min}}{Z_0 + Z_{\min}} \tag{9}$$

where Z_0 is the characteristic impedance required for the system. To optimize the device by minimizing the maximum return loss, it is necessary to get Γ_{DOWN} equal to $-\Gamma_{\mathrm{UP}}$; thus, the characteristic impedances are related as

$$Z_0 = \sqrt{Z_{\max} Z_{\min}} \tag{10}$$

Using equations (8) and (10) leads to

$$Z_0 \propto \frac{1}{\left(\varepsilon_{\mathrm{reffmax}} \times \varepsilon_{\mathrm{reffmin}}\right)^{1/4}} \tag{11}$$

In UP or DOWN states, the phase shifter can be considered as a mismatched transmission line (not matched to Z_0). The insertion loss due to this mismatch, IL_Γ, is higher where the return loss, RL, is maximum, when the electrical length of the S-CPW resonates in an odd multiple of 90°. They are given by equations (12) and (13), respectively.

$$RL = \Gamma = \frac{Z_{max} - Z_{min}}{Z_{max} + Z_{min}} \tag{12}$$

$$IL_{\Gamma} = \sqrt{1 - \Gamma^2} = \sqrt{1 - \left(\frac{1 - \sqrt{\frac{\varepsilon_{reffmax}}{\varepsilon_{reffmin}}}}{1 + \sqrt{\frac{\varepsilon_{reffmax}}{\varepsilon_{reffmin}}}} \right)^2} \tag{13}$$

The plot of IL_{Γ} is given in Fig. 3. It clearly shows that the insertion loss increases with the increase of ratio between $\varepsilon_{reffmax}$ and $\varepsilon_{reffmin}$.

In conclusion, in one hand, the increase of the ratio $\varepsilon_{reffmax}/\varepsilon_{reffmin}$ leads to an increase of the FoM_Q, but in the other hand, it leads to an increase of the mismatch of the tunable S-CPW for the UP and DOWN states, reducing the FoM_{Γ}. There is an optimum choice of the ratio $\varepsilon_{reffmax}/\varepsilon_{reffmin}$, leading to a phase shifter with minimum insertion loss considering all phase states. This optimum choice is highlighted by plotting the total $FoM_{Q+\Gamma}$ for an $\varepsilon_{reffmin}$= 7, shown in Fig. 4. However, since the $FoM_{Q+mismatch}$ curve is relatively flat near its maximum value, higher ratios could be chosen to reduce the phase shifter length without much reduction of this FoM.

In Fig. 4, it can be seen that FoM_Q increases continuously with $\varepsilon_{reffmax}/\varepsilon_{reffmin}$. However, when the mismatch of the S-CPW is considered, the $FoM_{Q+\Gamma}$ reaches a maximum for a given $\varepsilon_{reffmax}/\varepsilon_{reffmin}$, and then slowly decreases. Simulations ANSYS HFSS of the tunable S-CPW using the proposed technology showed a Q-factor of around 20, as already mentioned. Hence, to start the design, the curve with $Q = 20$ was considered, in which the optimum $\varepsilon_{reffmax}/\varepsilon_{reffmin}$ that leads to the highest $FoM_{Q+\Gamma}$ (110°/dB) is equal to 5.14. The maximum return loss for the UP and DOWN states, calculated from equation (12), is equal to 8.3 dB.

Figure 5 illustrates the design flow for the MEMS S-CPW phase shifter.

The first design step of the tunable S-CPW is the choice of the CPW dimensions, i.e., strip width W, gap S, and air gap height h. The choice of these dimensions must respect the conditions given in equations (10) and (11). Figure 6 gives the S-CPW characteristic impedance and dielectric constant as function of W for $D = 41$ µm (defined in Sect. 3.1) and different air gap heights h, from 0 up to 1.4 µm, all curves from the analytical model. $\varepsilon_{reffmin}$ corresponds to $h = 0$ µm (DOWN state). Note that the membrane thickness h_{siNx} was fixed to 1 µm (Table 1) for technological constraints, and the floating ribbons were placed in the middle of the membrane. Hence, the total height for the DOWN state is 0.5 µm of SiN_x, whereas the total height for the UP state is the sum of air gap height h and 0.5 µm of SiN_x.

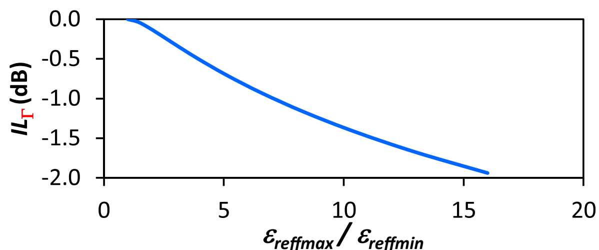

Fig. 3 Influence of $\varepsilon_{reffmax}/\varepsilon_{reffmin}$ in the insertion loss IL_{Γ}

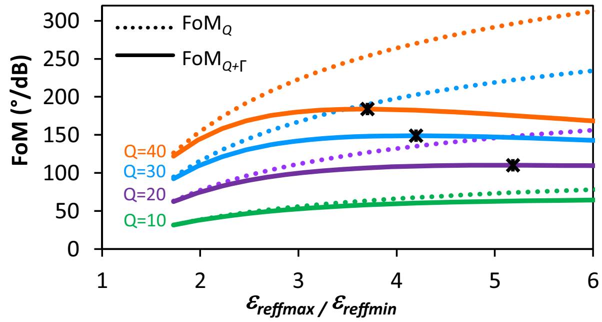

Fig. 4 Comparison between FoM_Q (dotted lines) and $FoM_{Q+\Gamma}$ (solid lines) as a function of $\varepsilon_{\mathrm{reffmax}}/\varepsilon_{\mathrm{reffmin}}$ for four different S-CPW Q-factors (10, 20, 30, and 40). The ∗ points indicate the maximum value of the curve

In order to achieve an average characteristic impedance close to 50 Ω, the combination of Z_{min} and Z_{max} must respect equation (10). The choice of $Z_{\mathrm{min}} = 33\ \Omega$ and $Z_{\mathrm{max}} = 75\ \Omega$ was done, according to the characteristic impedance that could be achieved by the technology. From the graph in Fig. 6, the choice of $Z_{\mathrm{min}} = 33\ \Omega$ for the DOWN state ($h = 0$ μm) gives $\varepsilon_{\mathrm{reffmax}} = 36$ and $W = 5$ μm, which results from (1) in $S = 18$ μm. For the UP state, considering Z_{max} and W, an $h = 1.2$ μm should be chosen, which gives a $\varepsilon_{\mathrm{reffmin}} = 7$.

From these results, the physical length of the tunable S-CPW can be calculated using equation (7). For $\Delta\theta = 315°$ (i.e., $360° - 360°/8$ corresponding to 3 bits), a length $l = 1.3$ mm is found using this procedure. The characteristics of the designed tunable S-CPW are summarized in Table 2 along with their Q calculated with the electrical model.

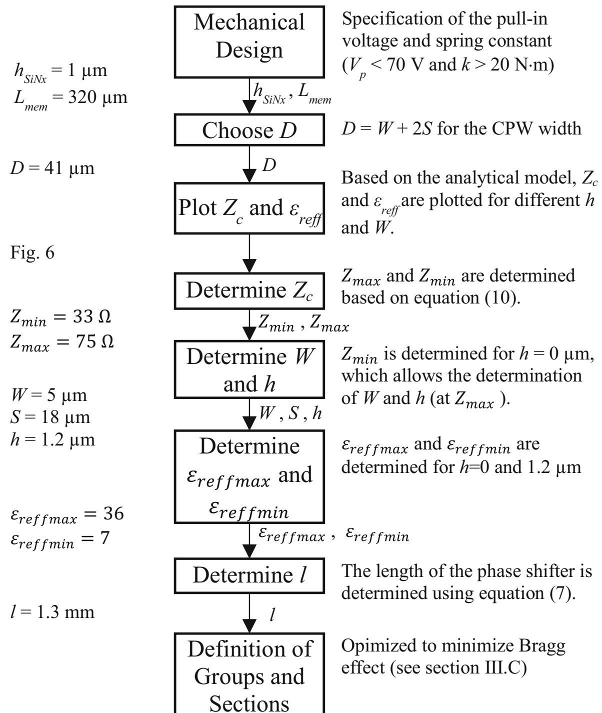

Fig. 5 Design flow of the MEMS S-CPW phase shifter

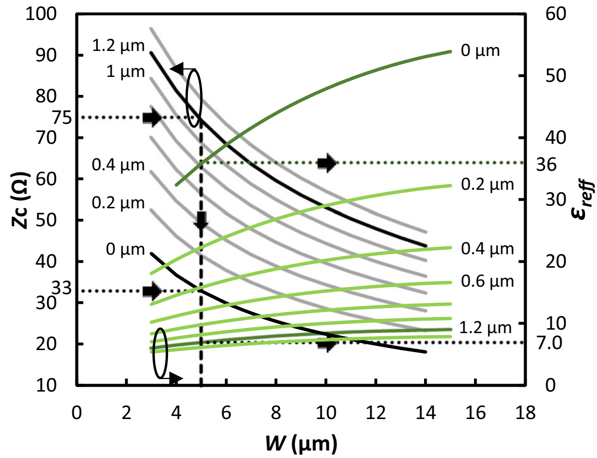

Fig. 6 Characteristic impedance and effective dielectric constant in function of CPW strip width W and air gap height h ranging from 0 to 1.4 μm. $W_g = 54.5$ μm. $D = W + 2S = 41$ μm

3.3 Phase Shifter Design

The characteristics of the S-CPW for the UP and DOWN states listed in Table 2 were used in Keysight's ADS™ to design the phase shifter.

To obtain higher resolution as compared to [12, 15], the shielding ribbons were divided in groups that can be actuated independently. Ideally, to obtain n bits of resolution, the shielding ribbons would have to be divided in n groups. However, the phase shift is not linear with respect to the length of each group, because of the characteristic impedance steps between actuated and unactuated sections, leading to standing waves formation, and hence not linear phase variation. Therefore, in this design, even if 128 phase states were obtained with the use of seven groups, it would correspond to a 3-bit phase shifter if one wants to achieve the precise phase states given by the number of bits. Many phase states occur between the designed 3-bit phase states; however, some of them are redundant.

The Bragg effect must also be considered when designing the phase shifter, since a periodic-like high-low characteristic impedance structure may appear for certain states. To minimize the Bragg effect, the groups were subdivided in eight intercalated sections, as exemplified in Fig. 7, each section composed by all groups. After that, the length of each of the seven groups illustrated in Fig. 7 was defined to obtain 3 bits of resolution with a maximum phase shift of 315°. The length and number of ribbons for each group is given in Table 3. Each group provides an incremental phase shift of 45° and they were designed to be activated in combination with the previous groups, e.g., to obtain a 270° phase shift, groups 1 through 6 should be activated. Due to the nonlinearity of the phase shift as a function of length and the resolution yielded by the individual ribbons, groups 6 and 7 are of the same length.

Table 2 Characteristics of the designed transmission line segment in the up and down states at 60 GHz

	S-CPW-UP	S-CPW-DOWN
Charac. Imp.	$Z_{max} = 75\ \Omega$	$Z_{min} = 33\ \Omega$
Diel. Const.	7	36
Q	20	18

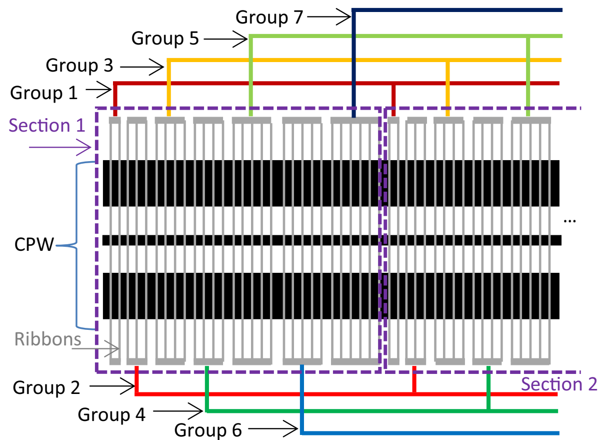

Fig. 7 Illustration of the actuation groups of the MEMS phase shifter

4 Experimental Results

Figure 8 shows an optical microscope image of the fabricated 3-bit phase shifter. The actual phase shifter is 1.375 mm long and 340 μm wide, thus leading to a surface equal to 0.47 mm^2, not considering the DC and RF pads.

Figure 9 shows a scanning electron microscope (SEM) image of some groups of the fabricated phase shifter. It is possible to identify the sections of each group. Color traces indicate how the sections were interconnected. In detail, the height between the membrane surrounding the floating ribbons and the CPW central strip of width W is shown. This SEM image revealed an air gap height h equal to 1.2 μm as designed and h_{SiNx} equal to 1.1 μm instead of 1 μm.

By applying a DC voltage to the shielding ribbons and connecting the DC ground to the RF ground, pull-in and pull-out voltages of 17 V and 10 V were measured, respectively. The voltage was swept from − 40 to + 40 V to measure the capacitance versus voltage $C(V)$ curve presented in Fig. 10. A small shift in the pull-in/pull-out was observed as the voltage was cycled several times. This indicates that the dielectric is charging, a well-known failure mechanism for capacitive MEMS switches.

The $C(V)$ curve in Fig. 10 also shows that there is a slight increase of capacitance after pull-in, suggesting that the membrane contacts the CPW in an uneven manner, i.e., the membrane does not contact the entire width of the ground strips and, as the voltage increases, the area of

Table 3 Length and number of ribbons for each group of the designed phase shifter

	Length (μm)	Number of ribbons	Phase shift (°)
Group 1	16	5	45
Group 2	19	6	90
Group 3	22	7	135
Group 4	25	8	180
Group 5	28	9	225
Group 6	31	10	270
Group 7	31	10	315

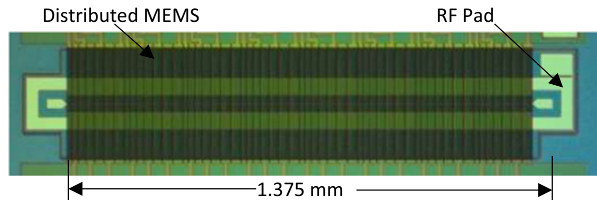

Fig. 8 Optical image of the MEMS phase shifter

contact increases. This behavior was observed thanks to electro-mechanical simulations carried out with ANSYS Multiphysics.

The electromechanical simulation was performed in ANSYS Structural using a transient analysis. Since the air gap height between the CPW electrode and the SiN_x membrane is 1.2 μm, and the bottom SiN_x layer is 0.55 μm thick, the distance between electrodes is 1.75 μm. Pull-in should occur when the floating ribbons are displaced approximately one-third of the gap or 0.58 μm. Figure 11 shows the deformation profile of the membrane for different simulated voltages after the structure reached an equilibrium. In the simulation, the pull-in voltage was 21 V. Results in Fig. 11 agree quite well with measurements presented in Fig. 10.

Figure 12 shows the measurement results for the phase shifter, from DC to 67 GHz. Measurements were carried out on an Anritsu Panorama ME7808C vector network analyzer (VNA) under vacuum. In Fig. 12a, it is possible to see that a linear phase shift is obtained with evenly spaced states. A maximum phase shift of 152° is achieved at 60 GHz, instead of the designed 315°. The extracted UP state characteristic impedance Z_{max} was approximately 75 Ω as designed, although the DOWN state characteristic impedance Z_{min} was approximately 50 Ω, instead of 33 Ω. The extracted $\varepsilon_{reffmin}$ was 8, close to the theoretical 7 and $\varepsilon_{reffmax}$ was 19, instead of 36. The reason for these differences in phase, Z_{min}, and $\varepsilon_{reffmax}$ can be associated with the actual distance between the shielding ribbons and the CPW strips in the fabricated phase shifter. In order to fit the measurement results, $h = 0.2$ μm (instead of zero) was considered in the DOWN state of the electrical model of the tunable S-CPW, along with the fabricated dimensions listed in Table 1. The whole phase shifter was simulated with Keysight ADS™, based on the characteristics of the S-CPW obtained from the electrical model, as done in the design phase. The results are also presented in Fig. 12a for the two extreme positions, i.e., "None Actuated" and "All Actuated". The agreement between retro-simulation and measurement results is very good for the phase shift (Fig. 12a) and return loss (Fig. 12b).

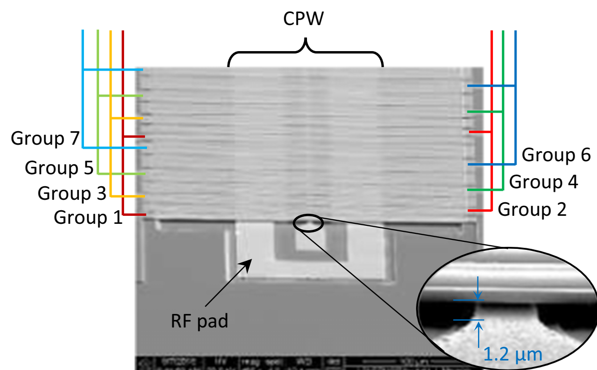

Fig. 9 Scanning electron microscope image of the MEMS phase shifter

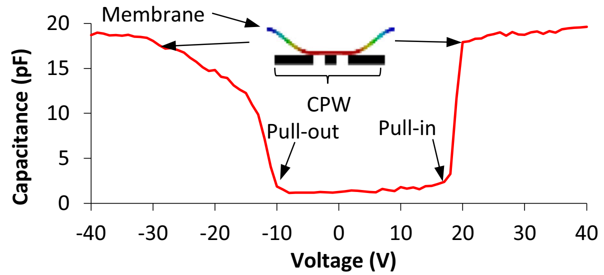

Fig. 10 Measurement of the pull-in and pull-out voltages of the MEMS phase shifter

This validates the hypothesis of an air gap with equivalent height of 0.2 μm between the SiN_x membrane and the CPW strips in the actuated case (DOWN state), which also change its characteristic impedance from 33 Ω (designed) to 50 Ω (measured) and the much lower $\varepsilon_{\mathrm{reffmax}}$. Therefore, the average characteristic impedance Z_{avg} is equal 61 Ω and, for this reason, the measured S-parameters were normalized to 61 Ω. A maximum insertion loss of 3 dB was obtained at 60 GHz, with a maximum insertion loss variation of 1.3 dB. The return loss is better than 13 dB for all phase states.

By using the measured values in equations (2) to (13), the calculated results are very close to measurement, including a calculated maximum return loss of 13.4 dB, corroborating the presented theory. And finally, the minimum Q-factor of the tunable S-CPW, corresponding to the DOWN state, can also be retrieved from the measured insertion loss, leading to $Q = 12$. For the UP state, the extracted Q-factor is equal to 13.5. These values were used to remake the calculations of the insertion loss at 60 GHz presented in Fig. 12c, showing that the calculated values for the UP and DOWN states agree very well with measurements.

Figure 13 presents the FoM for three different devices on the same wafer, showing small variation. A FoM of approximately 50°/dB at 60 GHz was obtained for the average of the three devices.

Table 4 presents a comparison between the presented MEMS phase shifter and the state-of-the-art for MEMS-based phase shifters at mm-waves. The FoM of the presented phase shifter is middle range, but the surface area is the smallest reported so far. If both FoM and area are taken into account (FoM_2), the device presented in this paper shows, to the best of our knowledge, the best compromise for MEMS-based phase shifters.

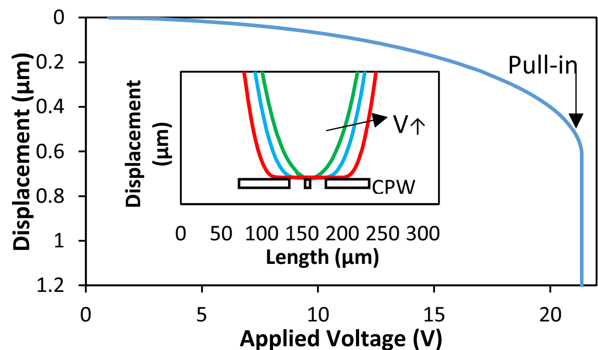

Fig. 11 Electromechanical simulation of the pull-in voltage and structure deformation after pull-in (insert)

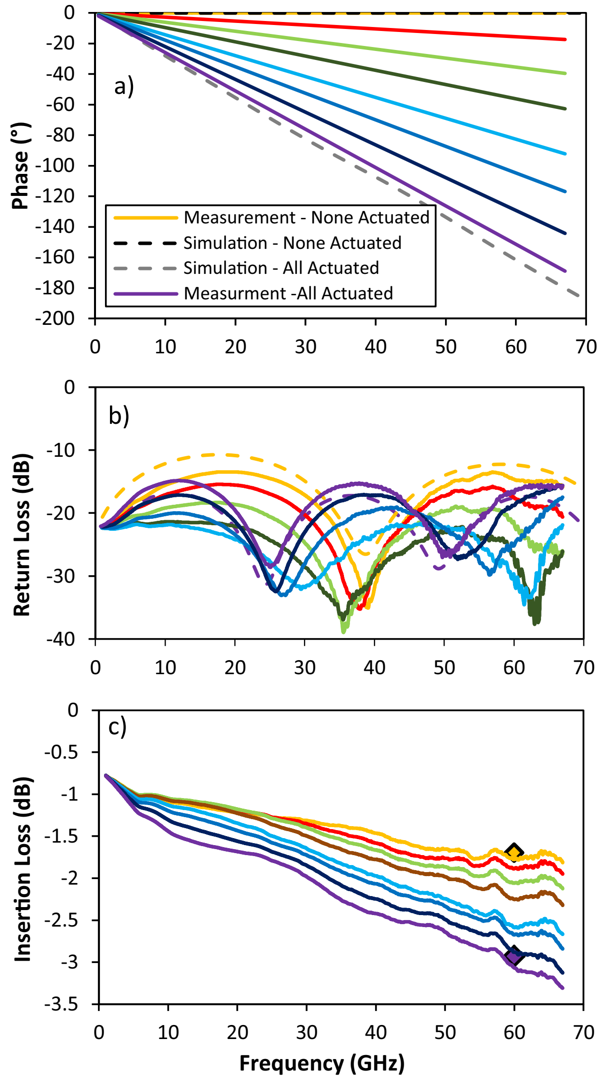

Fig. 12 Measured (solid lines) and simulated (dashed lines) phase shift (**a**), return loss (**b**), and insertion loss (**c**) of the MEMS phase shifter

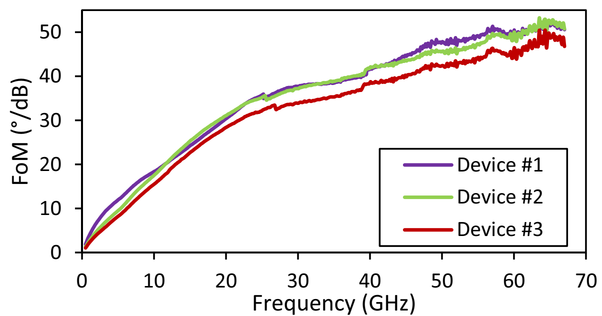

Fig. 13 Measured and simulated figure of merit (FoM) for three different devices on the same wafer

Table 4 State-of-the-art of passive phase shifters based on MEMS

Reference	[1]	[2]	[8]	[22]	[17]	This work
Technology	Quartz	Quartz	CMOS 0.18 μm	Glass	CMOS 0.35 μm	HR Si
Frequency (GHz)	60	65	65	78	60	60
Topology	Switched line	Loaded line	RTPS	Loaded line	Distributed-MEMS S-CPW	Distributed-MEMS S-CPW
Phase shift	270°	338°	144°	316°	25	152°
Resolution	2 bits	4 bits	1.5 bits	3 bits	2 bits	3 bits
Max. insertion loss (dB)	3	2.8	4	3.1	0.7	2.9
Change of Insert. loss (dB)	0.8	0.8	2.5	1.2	0.1	0.85
Area (mm^2)	4	11.85	1.04	9.67	0.58	0.47
FoM (°/dB)	90	93	45	102	36	50
FoM_2 ($\Delta\phi \times$ FOM/-area)	60	25	62	33	16	164

5 Conclusion

This paper demonstrated a miniaturized MEMS phase shifter based on a tunable slow-wave CPW. A total phase shift of 152° was obtained with a maximum insertion loss of 3 dB, resulting in a FoM of 50°/dB at 60 GHz. The miniaturized phase shifter occupies only 0.47 mm^2, resulting in $FoM_2 = 164$, which is the best reported in the literature for MEMS-based phase shifters, to the best of our knowledge. The device also showed an insertion loss variation of 1.3 dB and return loss better than 13 dB.

The pull-in and pull-out voltages were measured to be 17 V and 10 V, respectively. While the pull-in voltage can be considered small in comparison to other RF MEMS circuits, it limits the distance between the ground strips (D) of the S-CPW, which also limits the Q-factor. By increasing D, it is possible to improve Q, and thus, the FoM. The Q-factor can also be further increased by increasing the thickness of the gold layer used for the CPW strips fabrication. A dielectricless version of the device based on mechanical stoppers could be developed to eliminate this charging effect. This technique was already demonstrated in [23] for RF MEMS switches from the CEA-LETI and could be easily implemented in the case of the phase shifter proposed in this paper. However, this technique was not implemented yet due to the elevated fabrication cost of test runs.

To go further, the phase shift can still be increased without increasing the length of the device by reducing the thickness of the SiN_x film between the floating ribbons and the CPW strips. And finally, an operating frequency of the order of 120 GHz could very simply be envisaged by limiting the length of the segments to 100 μm in order to be located far enough from the Bragg frequency.

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