



## A 220- to 299-GHz CMOS Terahertz Detector

Zhao-yang Liu<sup>1,2,3,4</sup> · Feng Qi<sup>1,2,3,4</sup> · Ye-long Wang<sup>1,2,3,4</sup> · Peng-xiang Liu<sup>1,2,3,4</sup> · Wei-fan Li<sup>1,2,3,4</sup>

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### Abstract

This paper proposes a terahertz (THz) detector in a 180-nm standard CMOS process. The detector consists of a square loop antenna and an NMOS transistor. The antenna has two feed ports. One is connected to the source of the transistor and the other is grounded to provide the source a dc ground. To improve the power transfer efficiency between the antenna and the transistor, impedance matching between them is needed. It is concluded that in order to increase the voltage responsivity of the detector, impedance matching should be achieved by changing the impedance of the antenna rather than by changing the impedance of the transistor. The parasitic capacitance and inductance of the gate power supply line will affect the antenna-transistor impedance matching. An open microstrip transmission line connected to the gate is designed to eliminate this influence. Measurement results show that the detector can detect THz radiation in the frequency range of 220 to 299 GHz. At 244 GHz, the detector achieves a best voltage responsivity of 2497 V/W and a noise equivalent power (NEP) of 357 pW/Hz<sup>1/2</sup>.

**Keywords** CMOS · Terahertz detector · Terahertz imaging · Square loop antenna

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✉ Feng Qi  
qifeng@sia.cn

- <sup>1</sup> Shenyang Institute of Automation, Chinese Academy of Sciences, Shenyang, 110016, China
- <sup>2</sup> Institutes for Robotics and Intelligent Manufacturing, Chinese Academy of Sciences, Shenyang, 110016, China
- <sup>3</sup> Key Laboratory of Opto-Electronic Information Processing, Chinese Academy of Sciences, Shenyang, 110016, China
- <sup>4</sup> The Key Lab of Image Understanding and Computer Vision, Liaoning Province, Shenyang, 110016, China

## 1 Introduction

Terahertz (THz) spectrum, ranging from 100 GHz to 10 THz, has a lot of potential applications, such as security check [1], radar [2], communication [3], material analysis [4], and cancer detection [5]. With the development of THz technology, the demand for small, high-speed, and high-sensitivity detectors for THz radiation operating at room temperature becomes more pressing. Thermal detectors like Golay cells [6], bolometers [7], and pyroelectric detectors [8] are sensitive. However, they have a relatively slow temporal response. In the past decade, the study of THz detectors based on field effect transistors (FETs) has gained significant attention due to their advantages of high sensitivity, high response speed, and compactness. The interest in the applications of FETs for THz detection started at the beginning of 1990s with the pioneering theoretical work of Dyakonov and Shur who demonstrated that a FET can detect THz radiation higher than its cutoff frequency [9, 10]. First detector realizations have been demonstrated in GaAs high electron mobility transistor (HEMT) technologies in [11]. InAlAs/InGaAs/InP HEMT with an asymmetric dual-grating-gate has demonstrated responsivity of 2.2 kV/W at 1 THz [12, 13]. Furthermore, in 2017, H. Qin et al. reported direct detection of incoherent THz emission from hot blackbodies by using antenna-coupled AlGaIn/GaN HEMT detectors cooled at 77 K [14]. Although HEMT-based detectors exhibit high sensitivity, it is difficult to integrate such a detector and signal processing circuits on a single chip. Owing to the advantages of low cost, high yield, and easy integration, CMOS technology is emerging as an alternative to other technologies. In recent years, development of CMOS FET-based detectors has been remarkably progressing [15–26]. The first sub-THz silicon FET detector was demonstrated in 2004 by Knap et al. [15]. The first focal plane FET detectors array was reported for imaging at 650 GHz in 2009 [16]. In 2012, a 1-k-pixel THz video camera chip was reported [19]. However, it adopts a two-NMOS configuration of a loop antenna feeding two NMOS transistors. Only half of the power received by the antenna is transferred to each transistor in the two-NMOS configuration. As a result, its output is 50% less than that of the single-NMOS detector. In 2017, a fully integrated 860-GHz CMOS THz sensor with readout circuit was reported [22], which integrates a grounded patch antenna to receive the THz waves. In 2019, a  $32 \times 32$ -pixel 0.94-THz imager with pixel-parallel 12b VCO-based ADC in 180-nm CMOS was reported, which also integrates a patch antenna [25]. However, the height between the metal layers of CMOS process is low, which will result in a low antenna radiation efficiency when the metal layers are used to fabricate a patch antenna below 300 GHz. Moreover, the large area of the patch antenna also makes it unsuitable for CMOS THz detectors below 300 GHz.

This paper presents a CMOS THz detector in a 180-nm CMOS process. The detector integrates a square loop antenna feeding a single-NMOS transistor. Compared with the circle loop antenna reported in [19], the square loop antenna is easier to be implemented in the CMOS process. Moreover, the square loop antenna is more suitable for THz detectors below 300 GHz than the patch antenna. To improve the power transfer efficiency between the antenna and the transistor, impedance matching between them is needed. There are two ways to achieve impedance matching: changing the impedance of the antenna and changing the impedance of the transistor.

After analyzing, we conclude that the way to increase the voltage responsivity ( $R_v$ ) of the detector is to change the impedance of the antenna rather than the impedance of the transistor. In the single-NMOS configuration, the gate-source bias supply lines will influence the transistors' impedance and result in impedance mismatching. To overcome this problem, an open microstrip transmission line connected to the gate of the transistor is designed. Measurement results show that the detector can detect THz radiation in the frequency range of 220 to 299 GHz. At 244 GHz, the detector achieves a best  $R_v$  of 2497 V/W and a noise equivalent power (NEP) of 357 pW/Hz<sup>1/2</sup>. Using the detector, a clear raster-scanning transmission image is obtained. This paper is organized as follows. Section 2 reviews the theoretical analysis of the THz transistor. Section 3 presents the detailed design of the proposed THz detector. Section 4 presents the measurement results. Section 5 concludes this paper.

## 2 Theory

Detection of THz radiation by plasmonic nonlinearities in a two-dimensional (2D) electron channel of the FET was originally proposed by Dyakonov and Shur in the 1990s [9, 10]. When a THz radiation,  $V_a \cos \omega t$ , is coupled to the gate and source of a FET, as shown in Fig. 1, a photoresponse appears in the form of dc voltage between the source and drain which is proportional to the THz power. The dc voltage  $V_{out}$  can be written as:

$$V_{out} = -V_a^2 / [4(V_G - V_{TH})] \quad (1)$$

where  $V_a$  is the amplitude of the THz radiation,  $V_G$  is the gate bias, and  $V_{TH}$  is the threshold voltage of the FET. However, the theory does not give a design guideline on how to maximize detector responsivity by optimizing the FET physical dimensions. The relationship between  $V_a$  and the THz power that the FET accepts is:

$$V_a^2 = 2P \cdot \frac{|Z_m|^2}{\text{Re}(Z_m)} \quad (2)$$

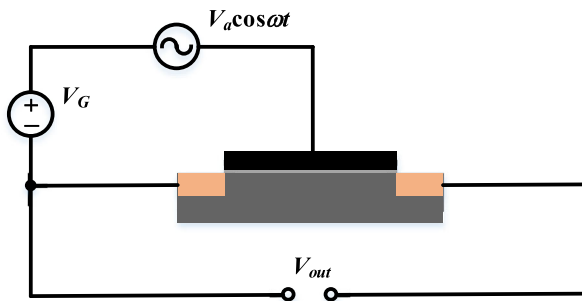


Fig. 1 Schematic of a FET as a THz detector

where  $P$  is the THz power that the FET accepts and  $Z_m$  is the source input impedance of the FET at the corresponding THz frequency [22]. Therefore, Eq. 1 can be rewritten as:

$$V_{out} = -\frac{P}{2(V_G - V_{TH})} \cdot \frac{|Z_m|^2}{\text{Re}(Z_m)} \quad (3)$$

Equation 3 indicates higher  $|Z_m|^2/\text{Re}(Z_m)$  results in a higher  $|V_{out}|$ . [22] has simulated the relationship between  $Z_m$  and the transistor dimensions. The simulation results show that  $|Z_m|^2/\text{Re}(Z_m)$  increases as the length and width of the FET decrease. Therefore, it concludes that the FET with the minimum physical dimension can produce a maximum responsivity. Hence, the NMOS transistor in the present design has the minimum size of  $0.18 \mu\text{m}$  in length and  $0.24 \mu\text{m}$  in width.

### 3 Detector Design

The circuit schematic of the proposed THz detector is shown in Fig. 2. It consists of an integrated on-chip square loop antenna and a source-feeding NMOS transistor with a nonbiased channel. The antenna has two feed ports. One is connected to the source of the transistor and the other is grounded to provide the source a dc ground. THz waves are received by the antenna and then coupled to the NMOS transistor, which has the minimum size of  $0.18 \mu\text{m}$  in length and  $0.24 \mu\text{m}$  in width. The gate of the transistor is biased to a constant potential  $V_G$  and its drain is open. The output signal  $V_{out}$  is extracted from the drain. An open microstrip transmission line,  $TL$ , is designed to eliminate the influence of the gate bias supply line on the transistor's impedance. All required low-frequency routing into the transistor is realized

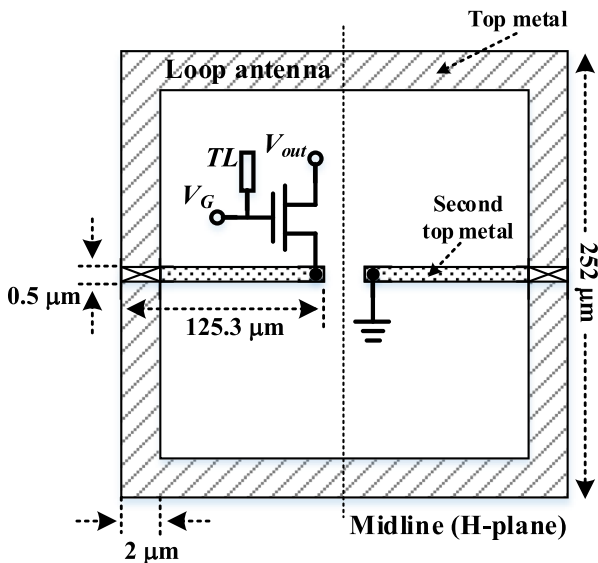


Fig. 2 Architecture of the proposed THz detector

along the antenna midline (H-plane) in order to reduce the impact on the antenna performance.

The proposed THz detector has the following advantages. First, the detector uses a single-NMOS configuration. Compared with the two-NMOS detector configuration reported in [16, 17, 19, 24], the single-NMOS configuration offers an improved voltage responsivity. In the two-NMOS configuration, only half of the power received by the antenna is transferred to each transistor. As a result, its output is 50% less than that of the single-NMOS detector. Second, it integrates a square loop antenna, which is compatible with CMOS process design rules. Compared with the circle loop antenna reported in [19, 24], the square loop antenna is easier to be implemented in the CMOS process. Moreover, the square loop antenna is more suitable for THz detectors below 300 GHz than patch antenna [16, 21–23] for the patch antenna would occupy a very large area below 300 GHz. Third, one feed port of the antenna is connected to the source of the transistor and the other is grounded to provide the source a dc ground. Compared with [16, 17, 19], in which an additional bias line connected to the antenna is needed to provide the NMOS gate-source bias, the proposed structure does not require such an additional bias line, thus mitigating the system-level complexity for future array implementations. Fourth, an open microstrip transmission line is designed to improve the detector performance by eliminating the influence of the gate supply line. Finally, an NMOS transistor with a minimum size is used as the rectifying element. The analyses presented in Section 2 demonstrate that a transistor with a minimum size can produce a maximum output signal.

### 3.1 NMOS transistor

The length and width of the NMOS transistor are  $0.18 \mu\text{m}$  and  $0.24 \mu\text{m}$ , respectively. We used the Synopsys TCAD simulator to simulate the source input impedance of the transistor under different frequencies. The simulation result is shown in Fig. 3. To achieve the maximum power transfer from the antenna to the NMOS transistor, the

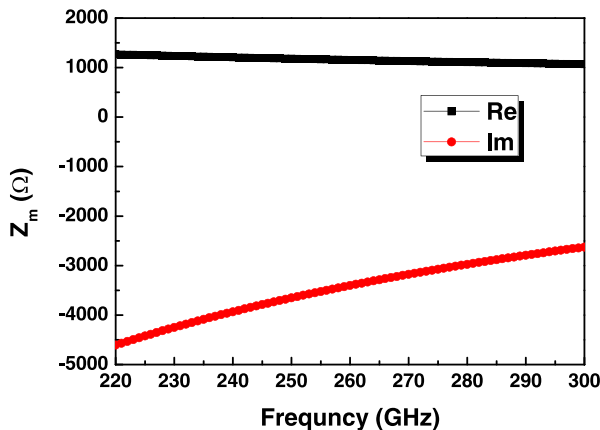


Fig. 3 Simulated source input impedance of the transistor under different frequencies

source input impedance of the transistor should be the conjugation to the antenna's impedance.

### 3.2 Square Loop Antenna

The square loop antenna is implemented using the top metal layer in the CMOS process and designed to provide broadband operation. The side length and the line width of the antenna are  $252 \mu\text{m}$  and  $2 \mu\text{m}$ , respectively, as shown in Fig. 2. The antenna has two feed lines. One is connected to the transistor and the other is grounded to provide the source a dc ground. Restricted by the minimum size of  $2 \mu\text{m}$  of the top metal layer, it is difficult to achieve a good impedance matching between the antenna and the transistor if the feed lines are implemented using the top metal layer. Hence, the feed lines are made of the second top metal layer. The length and width of each feed line are  $125.3 \mu\text{m}$  and  $0.5 \mu\text{m}$ , respectively.

The 3D electromagnetic solver package HFSS was used to simulate the antenna performance. Simulated results predict an antenna efficiency of 58–71% with a 1.85–4.5 dBi directivity across the 220–299-GHz band for back-side illumination through a  $180\text{-}\mu\text{m}$ -thick bulk silicon substrate. The simulated impedance of the antenna is plotted in Fig. 4.

The matching coefficient  $M_c$ , defined as the ratio of the power accepted by the NMOS transistor to the incident power from the antenna, can be expressed as follows:

$$\begin{aligned} M_c &= \frac{P}{P_{inc}} \\ &= \frac{\text{Re}(Z_m)}{|Z_m + Z_{ANT}|^2} / \frac{1}{4\text{Re}(Z_{ANT})} \\ &= 4\text{Re}(Z_{ANT})\text{Re}(Z_m) / |Z_m + Z_{ANT}|^2 \end{aligned} \quad (4)$$

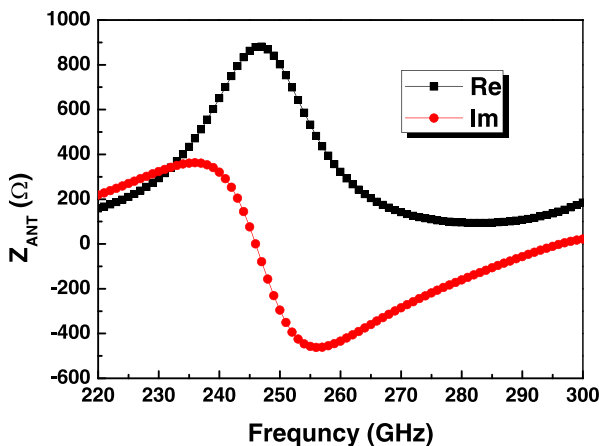


Fig. 4 Simulated impedance of the antenna under different frequencies

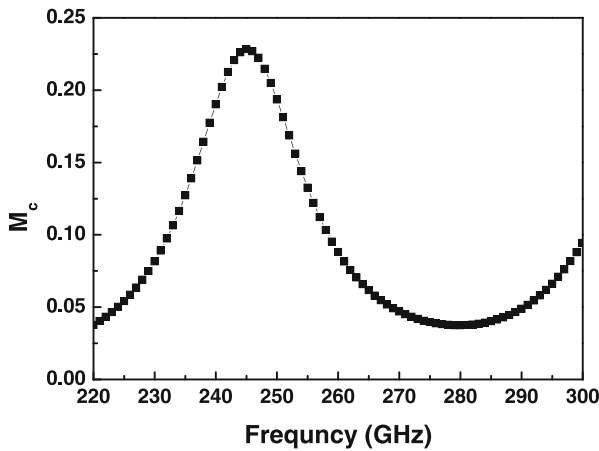


Fig. 5 Calculated  $M_c$  as a function of frequency

where  $P$  is the THz power accepted by the NMOS transistor,  $P_{inc}$  is the incident THz power from the antenna, and  $Z_{ANT}$  is the antenna’s impedance. Figure 5 shows the calculated  $M_c$  as a function of frequency. Equation 3 can be rewritten as:

$$\begin{aligned}
 V_{out} &= -\frac{M_c P_{inc}}{2(V_G - V_{TH})} \cdot \frac{|Z_m|^2}{\text{Re}(Z_m)} \\
 &= -\frac{M_c \eta J_{inc} A_{eff}}{2(V_G - V_{TH})} \cdot \frac{|Z_m|^2}{\text{Re}(Z_m)}
 \end{aligned}
 \tag{5}$$

where  $\eta$  is the radiation efficiency of the antenna,  $J_{inc}$  is the power density incident to the antenna, and  $A_{eff}$  is the effective area of the antenna.  $A_{eff}$  can be calculated as follows:

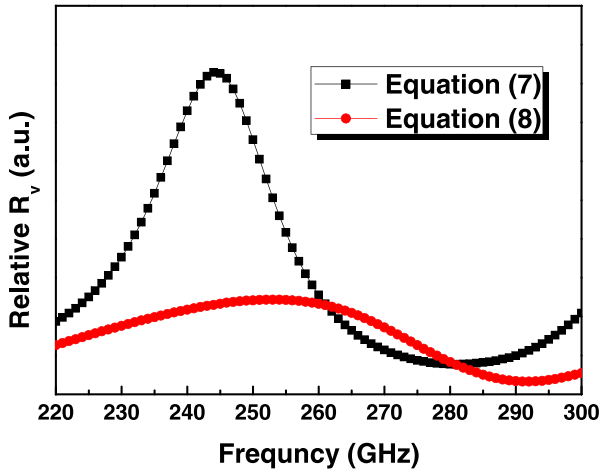
$$A_{eff} = D\lambda^2/4\pi
 \tag{6}$$

where  $D$  is the directivity of the antenna and  $\lambda$  is the electromagnetic wave length in free space. The performance of a THz detector is typically expressed by means of  $R_v$  and NEP [27].  $R_v$  is defined as the ratio between the detector output voltage and the power incident to antenna, that is:

$$R_v = -\frac{V_{out}}{J_{inc} A_{eff}} \propto M_c \eta \cdot \frac{|Z_m|^2}{\text{Re}(Z_m)}
 \tag{7}$$

According to the simulation results and Eq. 7, the relative  $R_v$  under different frequencies is calculated and plotted in Fig. 6.

As shown in Fig. 5, the maximum value of  $M_c$  is 0.23, which indicates that the THz power transfer between the antenna and NMOS transistor is not good. However, it is difficult to find a good matching network design to increase the impedance of the antenna without serious attenuation of its radiation efficiency. If we change the impedance of transistor to increase the  $M_c$  value, the value of  $\frac{|Z_m|^2}{\text{Re}(Z_m)}$  would decrease. Next, we discuss an ideal condition. We assume that the perfect impedance matching

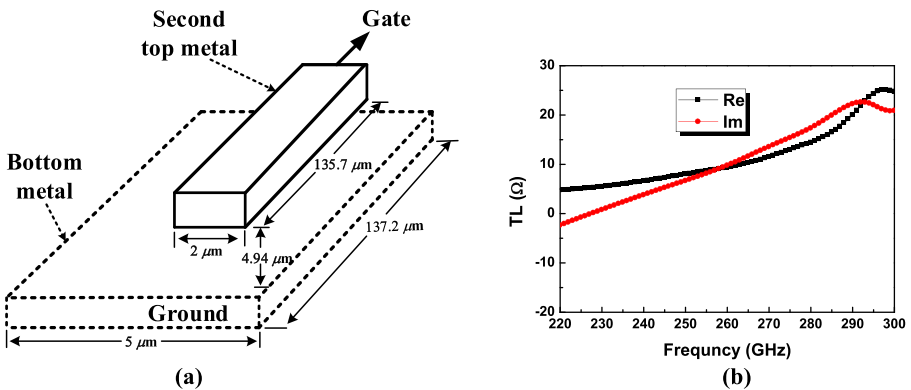


**Fig. 6** Calculated relative  $R_v$  of the detector based on the simulation results. The black and red lines are calculated based on Eqs. 7 and 8, respectively

is achieved at all frequencies by changing the impedance of the transistor, which means  $\text{Re}(Z_m) = \text{Re}(Z_{ANT})$  and  $\text{Im}(Z_m) = -\text{Im}(Z_{ANT})$ . So,  $M_c = 1$  and:

$$R_v \propto \eta \cdot \frac{|Z_{ANT}|^2}{\text{Re}(Z_{ANT})} \tag{8}$$

The relative  $R_v$  in this condition is also plotted in Fig. 6. As shown, although perfect impedance matching is achieved, the  $R_v$  is not optimized due to the low value of  $\frac{|Z_{ANT}|^2}{\text{Re}(Z_{ANT})}$ . Therefore, we conclude that the way to increase the  $R_v$  is to change the impedance of the antenna rather than the impedance of the transistor.



**Fig. 7** a Structure of the TL and b simulated impedance of the TL as a function of frequency



### 3.3 Open Microstrip Transmission Line

Since the gate of the transistor should be connected to a constant potential, it is typically biased directly by an off-chip voltage supply through the bonding wire, pad, and on-chip metal line. The parasitic capacitance and inductance of these components will influence the transistor's source input impedance. The  $TL$  (Fig. 2) is an open microstrip transmission line used to improve the detector performance by reducing the influence of the gate connections [22]. One end of it is connected to the transistor gate, and the other is floating, as shown in Fig. 7a. It is implemented in the second top metal layer, using the bottom metal layer as the ground plane. Its length and width are  $135.7 \mu\text{m}$  and  $2 \mu\text{m}$ , respectively. Figure 7 b shows its simulated impedance. Both the real and imaginary parts are less than  $30 \Omega$  in the frequency range of 220 to 299 GHz. Since the  $TL$  and the gate bias supply line are connected in parallel, the low impedance  $TL$  will reduce the influence on the transistor's impedance.

## 4 Measurement Results

The detectors are fabricated in a 180-nm CMOS process. Figure 8 shows its die photo. The proposed detector is displayed in the middle, which is characterized using the lock-in technique. The chip is mounted on a printed circuit board (PCB). Since the chip receives THz waves from the back, we made a circular hole in the middle of the PCB to place the chip and bonded it with a polyethylene, as shown in Fig. 9a. Figure 9 b illustrates the measurement setup. Continuous-wave THz signal is radiated by a THz vector network analyzer (VNA). The frequency of the radiated THz signal is tunable. In the test, the test frequency ranges from 220 to 299 GHz. Linearly polarized THz signal is radiated through a 25-dBi diagonal horn. A mechanical chopper with a frequency of 114 Hz modulates the THz signal. A 20-dB low noise amplifier (LNA) is connected directly at the output of the detector and a lock-in amplifier is

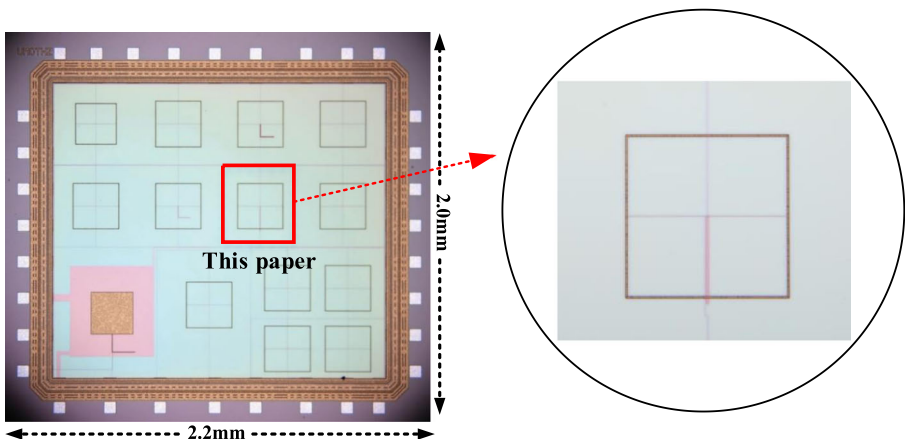
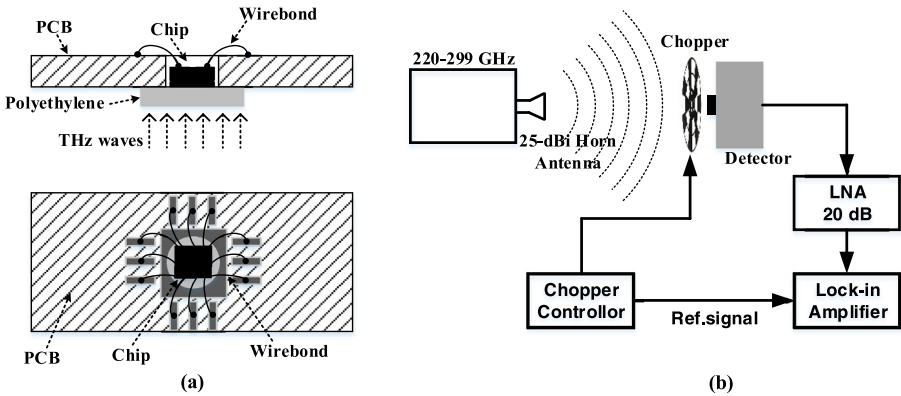


Fig. 8 Die photo of the THz detector

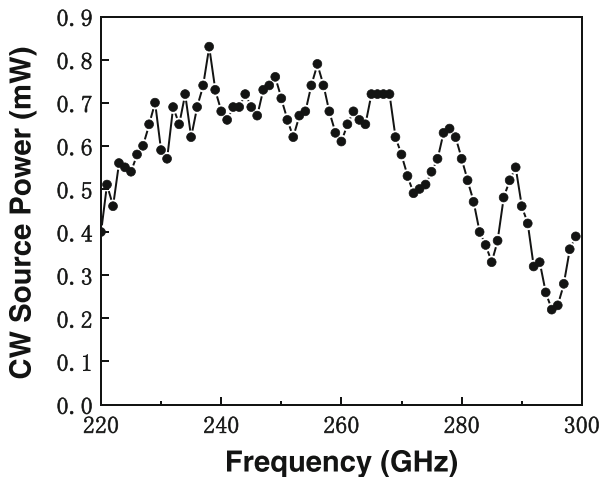


**Fig. 9** **a** Cross section and top views of the PCB for testing and **b** measurement setup used to characterize the detector

used to recover the output signal. The radiated THz power at different frequencies is measured with a power meter and plotted in Fig. 10.

The measurement results show that the detector has the best output at 244 GHz. The measured  $R_v$  and NEP of the detector as a function of the gate bias voltage at 244 GHz are shown in Fig. 11. The peak non-amplified  $R_v$  is 2497 V/W and the minimum NEP at 114-Hz modulation frequency is 357 pW/Hz<sup>1/2</sup> for a gate bias of 0.33 V and 0.52 V, respectively. The NEP changes slowly in the gate voltage range of 0.3–0.6 V.

The maximum  $R_v$  versus frequency is plotted in Fig. 12. From 220 to 299 GHz, the  $R_v$  is between 117 and 2497 V/W. In the frequency range of 241 to 260 GHz, the  $R_v$  is higher than 1500 V/W. The simulated relative  $R_v$  based on Eq. 7 is also plotted in Fig. 12. The two curves are similar in shape but there is a difference of



**Fig. 10** Continuous-wave radiation power measured with a power meter

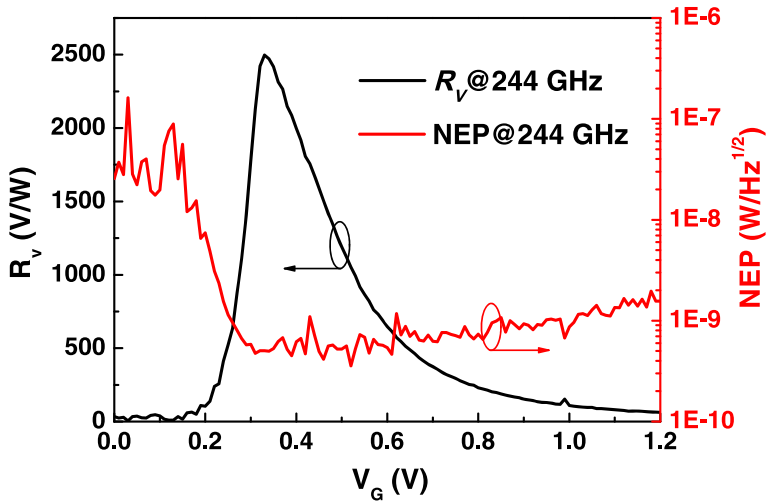


Fig. 11 Measured  $R_v$  and NEP at 244 GHz as functions of the gate bias voltage

approximately 7 GHz in frequency. The reason for this deviation may be that in the simulation of the antenna, the dielectric constant is set according to the value given by foundry, while in fact the dielectric constant varies with the frequency. In other words, the dielectric dispersion is not considered in the simulation, which leads to the difference between simulation and measurement.

We realize a THz imaging system using the detector, as shown in Fig. 13a. A mechanical chopper with a frequency of 114 Hz modulates the radiation of a VNA

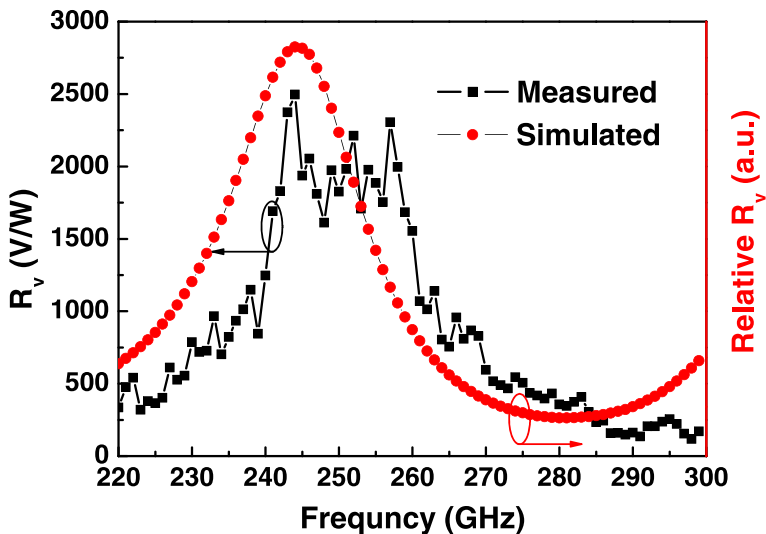
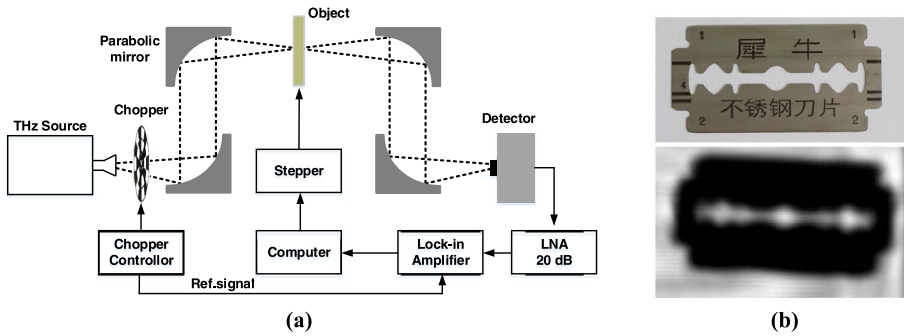


Fig. 12 Measured  $R_v$  and simulated relative  $R_v$  at varying source frequencies



**Fig. 13** **a** Block diagram of the THz imaging system and **b** image captured at 244 GHz of a knife in a paper envelope

with a radiation frequency of 244 GHz, and at the same time, generates a TTL signal as the reference signal for a lock-in amplifier. The THz radiation is collimated and focused on an object by two parabolic mirrors. The object is fixed on a two-dimensional stepper to realize the scanning image. The transmitted THz radiation is collimated and focused on the detector by two other parabolic mirrors. The output signal of the detector is amplified by a 20-dB LNA and the lock-in amplifier is used to capture the amplified signal. Figure 13 b shows a raster-scanning image of a knife in a paper envelope. The scanned area was  $3 \times 5 \text{ cm}^2$ , divided into  $150 \times 250$  pixels. The image clearly reveals the shape of the hidden knife. A performance comparison between this work and other published THz detectors is shown in Table 1.

**Table 1** Performance comparison of CMOS terahertz detectors

Technology	Freq. (THz)	Max $R_v$ (V/W)	Min NEP ( $\text{pW}/\text{Hz}^{1/2}$ )	Ref.
180 nm CMOS	0.24	2.5k	357	This work
65 nm CMOS	0.86	<sup>1,2</sup> 140k	<sup>1,2</sup> 100	[19]
65 nm CMOS	1.027	800	66	[17]
65 nm CMOS	3.0	526	73	[23]
130 nm CMOS(SBD)	0.28	250	33	[27]
130 nm CMOS	0.3	5k	10	[18]
130 nm CMOS	0.27	<sup>3</sup> 300k	<sup>3</sup> 18.7	[20]
180 nm CMOS	0.86	3.3k	106	[22]
180 nm CMOS	0.29	701	261	[24]
250 nm CMOS	0.65	<sup>4</sup> 80k	<sup>4</sup> 300	[16]

<sup>1</sup>With an integrated amplifier with a 50-dB open-loop gain and a 5-dB VGA gain

<sup>2</sup>With an integrated Si lens

<sup>3</sup>With an integrated amplifier with a 58-dB closed-loop gain

<sup>4</sup>With an integrated amplifier with a 43-dB open-loop gain

## 5 Conclusions

This paper proposes and implements a novel THz detector in a 180-nm standard CMOS process. The detector integrates a square loop antenna feeding a single-NMOS transistor with a nonbiased channel. One port of the antenna is grounded so that it does not require an additional bias line to provide a dc path for the NMOS transistor. An open microstrip transmission line,  $TL$ , is designed to improve the detector performance. Measurement results show that the detector can detect THz radiation in the frequency range of 220 to 299 GHz. At 244 GHz, the detector has the best output. The maximum  $R_v$  and minimum NEP are 2497 V/W and 357 pW/Hz<sup>1/2</sup>, respectively. Using the detector, a clear raster-scanning transmission image has been obtained. The results indicate that the proposed detector can be further used in a multi-pixel array for THz imaging.

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