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A K-Band Low-Power Phase Shifter Based on Injection Locked Oscillator in 0.13 μm CMOS Technology

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Abstract In this paper, the design challenges of the injection-locked oscillator (ILO)-based phase shifter are reviewed and analyzed. The key design considerations such as the operating frequency, locking range, and linearity of the phase shifters are analysed in detail. It is possible to optimize the phase shifter in certain parameters such as ultra-low power while meeting the requirements of a certain system. As a design example, a K-band phase shifter is implemented using a commercial 0.13 μm CMOS technology, where a conventional LC tank based topology is implemented but optimised with a good balance among power consumption, working range, sensitivity, and silicon area, etc. Measurement results show that the proposed phase shift is able to work at 22–23.4 GHz with a range of 180° while consuming 3.14 mW from a 1.2 V supply voltage.

Keywords Phase shift · CMOS · K-band · Injection locked oscillator · Voltage-controlled oscillator

1 Introduction

The continuously increasing demands for higher data rate have increased attentions to phased arrays for nowadays communication systems. At the expense of hardware complexity, a higher signal-to-noise ratio is achievable in such a system where a high-performance phase shifter is a key building block to combine multi-phase signals

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effectively [21, 25, 31]. As for circuit implementation, with the rapid progress of silicon based radio-frequency integrated circuits (RFICs), it is possible to implement a fully-integrated phase-array system with low power consumption by taking the advantage of the highest level of integration using the CMOS technology [21, 25, 31]. Phase shifters with different topologies such as passive reciprocal networks type using transmission lines [21, 25, 31] , lumped elements networks [2, 17], vector modulated type [3, 29, 30], and other topologies [18, 24], have been extensively reported. And recently, many work implemented in advanced CMOS technology, with lower power or high-frequency operations has been reported in [1, 15, 27]. Unfortunately, a phase shifter with high frequency, accurate phase control, small silicon area, low power consumption, low loss variation within the entire working frequency range, etc., remains a great challenge. The design strategy of a phase shifter should be determined based on different applications. For example, an active vector modulator phase shifter exhibits high gain at the cost of high DC power and complexity with additional digital control circuits. By contrast, passive phase shifters usually exhibit better linearity without DC power consuming but with a certain insert loss which requires additional link budget in a communication system. In addition, the passive components in the passive phase shifter, such as transmission lines occupy a considerably large silicon area, making it less attractive in CMOS fully-integrated system. The tuning mechanism of the phase shift is another key consideration, vector summer can only provide certain phase shifts with several-bit of resolution, e.g., a 4-bit 360° phase shifter in 22.5° steps, using digital switches [27] (e.g., 22.5° for 3-bit operation, using digital switches). The alternative solution, a continuously varying phase shifter is able to work at a limited range only. It is therefore not possible to conclude an uniform solution to a communication system. But considering the rapid progress of millimetre wave range phase array mobile system with a high level of integration, it is of a great interest if the phase shifter can be implemented with acceptable phase accuracy, small silicon area and low power consumption. In this paper, a K-band phase shifter is presented to meet these requirements. The theoretical analysis of the phase shift in a LC tank based oscillator is presented, followed by the optimisation of the performance matrix as well as the silicon verification of the prototype in a commercial 0.13 μm CMOS technology.

2 Design Consideration

In a K-band fully-integrated mobile communication system, the silicon area and power consumption become the major design considerations once the accuracy of the phase shifter is secured. The passive design is less attractive due to large silicon areas occupied by the passive devices [21]. The large power consumption and limited resolutions in a vector summer based phase shifter are the major drawbacks. As a design example, a K-band vector-sum phase shifter with a resolution of 22.5° requires a total power consumption of 25.2 mW as reported in [23]. Phase shifts based on injection locked voltage controlled oscillators have been reported as a good candidate to solve these issues [11, 26]. They has been widely used in designing quadrature (fix phase of 90°) oscillator [9, 10, 14] or phase shifters [1, 4, 11, 26, 27]. Unfortunately,

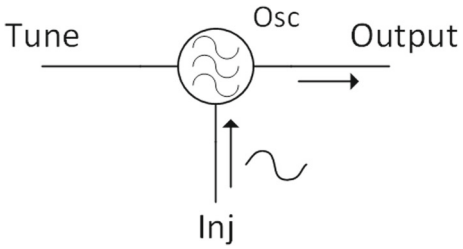


Fig. 1 An oscillator can be injected by a source and output a same frequency wave in a very special circumstance

the oscillator is sensitive to process, voltage, and temperature (PVT) variations. The total linear phase tuning range is thus very limited and unstable. It is therefore of a great importance to perform a detailed analysis of this topology and to perform optimizations accordingly.

2.1 Physical Model of the Injection Locked Oscillator

A simplified scheme of injection locked oscillator (ILO) can be modeled as an oscillator locked to an external signal source, as shown in Fig. 1.

The circuit works as a free running oscillator without an input signal. But the oscillator will tracks the input frequency at a certain frequency range close to its self-resonant frequency, which is called injection locking. For an oscillator with the free running frequency of ω_0, which is locked in with an input signal I_{inj} (at the frequency of ω_{inj}), as shown in Fig. 2, the working condition can be derived as follows.

As illustrated in Fig. 3,

$$\mathbf{I}_{\text{out}} = \mathbf{I}_{\text{inj}} + \mathbf{I}_{\text{osc}} \tag{1}$$

It is assumed that the angle between $\mathbf{I}_{\text{inj}}$ and $\mathbf{I}_{\text{osc}}$ is θ and the angle between $\mathbf{I}_{\text{out}}$ and $\mathbf{I}_{\text{osc}}$ is φ, the relationship between θ and φ can be written as.

$$\frac{I_{\text{out}}}{\sin\theta} = \frac{I_{\text{inj}}}{\sin\varphi} \tag{2}$$

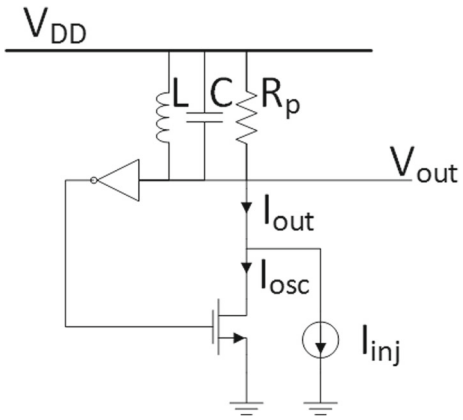


Fig. 2 An oscillator injected by I_{inj} having an output current of I_{out}

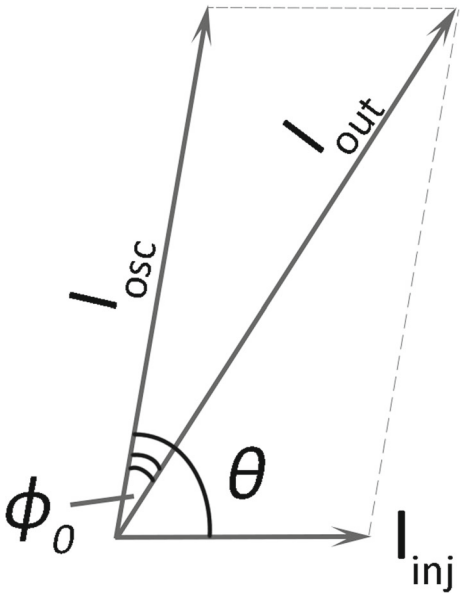


Fig. 3 The sum of the vectors of $\mathbf{I}_{inj}$ and $\mathbf{I}_{osc}$ is $\mathbf{I}_{out}$ [22]

$$\sin\varphi = \frac{I_{inj}}{I_{out}}\sin\theta \tag{3}$$

According to Eq. 1,

$$\sin\varphi = \frac{I_{inj}\sin\theta}{\sqrt{I_{out}^2 + I_{osc}^2 + 2\cos\theta I_{out} I_{osc}}} \tag{4}$$

When $I_{inj} \ll I_{osc}$, then

$$\sin\varphi = \frac{I_{inj}}{I_{osc}}\sin\theta \tag{5}$$

Considering $Z(\omega)$ represents the impedance of the resonance circuit, then

$$Z(\omega) = j\left(\omega L - \frac{1}{\omega C}\right) + R_L \tag{6a}$$

$$= j(\omega^2 - \omega_0^2)\frac{L}{\omega} + R_L \tag{6b}$$

Where R_L is the loss of the tank and $\omega_0 = \frac{1}{\sqrt{LC}}$ is the resonant frequency of the tank.

Since ω is close to ω_0, so

$$\omega^2 - \omega_0^2 \approx 2\omega(\omega - \omega_0) \tag{7}$$

Equations 7 and 6 gives

$$Z(\omega) \approx 2j(\omega - \omega_0)L + R_L \tag{8}$$

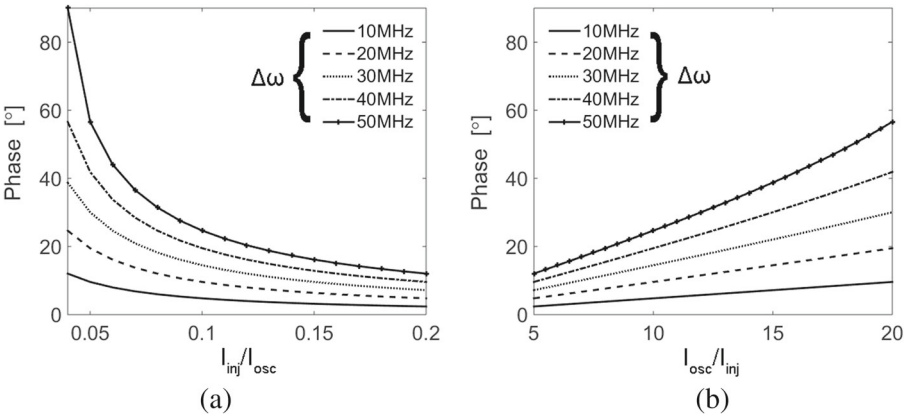


Fig. 4 Phase shift created by oscillator injected by a stable oscillation source when $Q_{\text{ext}} = 10$, $f = 24$ GHz with different $\Delta\omega$

The phase shift φ of the tank is given as:

$$\varphi \approx \arctan\left(\frac{2(\omega - \omega_0)L}{R_{\text{L}}}\right) \tag{9}$$

Considering $Q_{\text{ext}} = \frac{L\omega_0}{R_{\text{L}}}$ to be the external quality factor, Eq. 9 can be re-written as

$$\tan\varphi \approx \frac{2(\omega - \omega_0)Q_{\text{ext}}}{\omega_0} \tag{10}$$

When $I_{\text{inj}} \ll I_{\text{osc}}$, φ is small enough to make $\sin\varphi \approx \tan\varphi$,

$$\sin\theta \approx \frac{2(\omega - \omega_0)Q_{\text{ext}}}{\omega_0} \cdot \frac{I_{\text{osc}}}{I_{\text{inj}}} \tag{11}$$

The phase shift between injected signal and output, $\theta - \varphi \approx \theta$ (at the extreme case that φ is so small that can be ignored), can now be approximated as

$$\theta \approx \arcsin\left(\frac{2(\omega - \omega_0)Q_{\text{ext}}}{\omega_0} \cdot \frac{I_{\text{osc}}}{I_{\text{inj}}}\right) \tag{12}$$

Supposing the injection source is a stable oscillation source, function of θ is relevant to ω_0, Q_{ext} and I_{osc}.

$$\theta \approx F_{\text{ps}}(\omega_0, Q_{\text{ext}}, I_{\text{osc}}) \tag{13}$$

The phase shift depends on at least three design parameters. It is possible to change ω_0, Q_{ext}, or I_{osc} to obtain the phase shift as suggested in Eq. 13. Given a constant Q_{ext} and ω_0, e.g., $Q_{\text{ext}} = 10$ and $f = 24$ GHz, the phase shift vs. I_{osc} can be illustrated in Fig. 4. Moreover, Fig. 5 suggests that phase shift is strongly linear over $I_{\text{osc}}/I_{\text{inj}}$ if $\Delta\omega = \omega - \omega_0$, the frequency shift, is small enough, which suggests that to adjust the phase shift by controlling I_{osc} is a high linearity way.

Unfortunately, the range of phase shift is quite limited in this solution, as illustrated in Fig. 4. Likewise, the changing of Q_{ext}(while I_{osc} and ω_0 is locked) exhibits

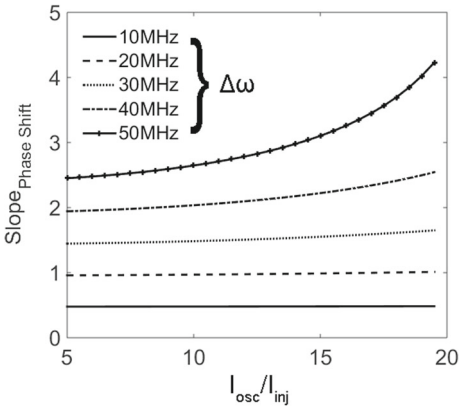


Fig. 5 The slopes of the phase shift curves with different $\Delta\omega$

similar characteristic. Tuning ω_0 to change the phase induces the largest phase shift range, because

$$\Delta\omega \approx \frac{\omega_0}{2Q_{\text{ext}}} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \sin\theta \tag{14}$$

$\Delta\omega$ reaches maximum value

$$\Delta\omega_{\max} = \frac{\omega_0}{2Q_{\text{ext}}} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \tag{15}$$

when $\sin\theta = 1$, or maximum absolute value

$$\Delta\omega_{\text{-max}} = -\frac{\omega_0}{2Q_{\text{ext}}} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \tag{16}$$

when $\sin\theta = -1$. $[\omega + \Delta\omega_{\text{-max}}, \omega + \Delta\omega_{\max}]$ is the locking range. If ω_0 is able to reach both lower and upper bound, 180° phase shift can be achieved theoretically.

2.2 Voltage-Controlled Oscillator

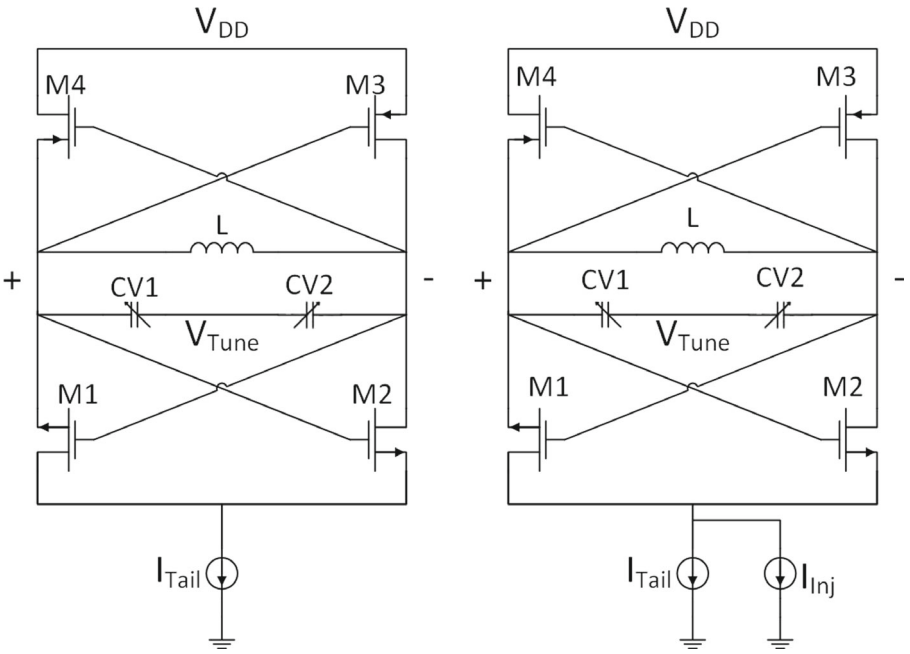
2.2.1 General Design Considerations

Supposing the oscillator of the ILO mentioned above is designed as a voltage controlled oscillator(VCO), it is possible to obtain variable phase shifts by changing the free running frequency of the VCO, ω_0. Both ring oscillators [1, 7, 13, 28] and LC oscillators [9, 11, 19, 26, 27] can be possibly implemented as a phase shifter. Considering the working range of tens of GHz, only the LC tank based VCO as shown in Fig. 6a is analyzed in this work.

The working frequency of this ILO (Fig. 6b), ω_0 is given as Eq. 17

$$\omega_0 = \omega \cdot \left(\frac{1}{2Q_{\text{ext}}} \cdot \frac{I_{\text{inj}}}{I_{\text{osc}}} \cdot \sin\theta + 1\right)^{-1} \tag{17}$$

The major challenge in the frequency tuning of the VCO is the optimization of the varactor, which has been widely used to change the effective load capacitance in the LC tank. The strong desire of wide tuning range of capacitance is actually limited by



(a) A typical LC-VCO. (b) An injection locked LC-VCO.

Fig. 6 Schematic diagram of LC-VCOs

the minimal required quality factor. The sizing of the varactor is thus one of the key trade-offs. As illustrated in Eq. 14 and [16], a tank with low quality factor, Q_{ext}, is preferred if a larger locking range is desired. However, it is risky to design a low Q_{ext} tank which results in a larger power consumption and poor phase noise performance.

2.2.2 Optimisation of the LC Tank

The key issue in this design will be the optimisation of the LC tank. The operating frequency and quality factor of the oscillator can be determined as follows.

Considering the tank as a parallel LC circuit, the relationship between the inductor, the capacitor and the quality factor of the tank, Q_{tank}, can be addressed as (18)

$$Q_{\text{tank}} = \frac{1}{\frac{1}{Q_{\text{L}}} + \frac{1}{Q_{\text{C}}}} \tag{18}$$

where

$$Q_{\text{L}} = \frac{\omega_0 L}{R_{\text{L}}} \tag{19}$$

$$Q_{\text{C}} = \frac{1}{\omega_0 C R_{\text{C}}} \tag{20}$$

At a relatively low frequency, the Q_{L} is the dominator of the Q_{tank}. But at K-Band, the quality factor of both the inductor and capacitor are important. To achieve a high

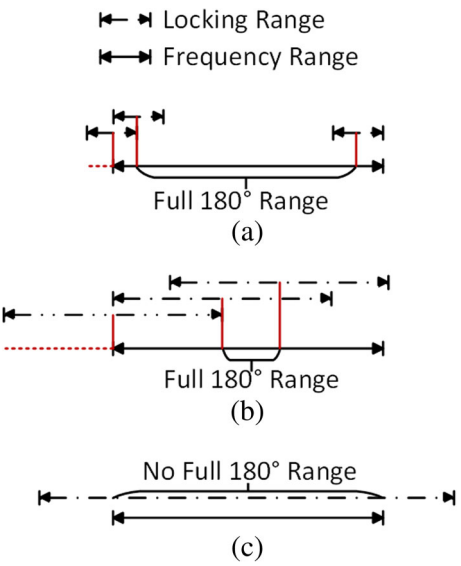


Fig. 7 Three kinds of locking and frequency ranges ratios

resonant frequency, the L_{tank} and the C_{tank} of the tank circuit should be determined as:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{21}$$

Where $L \approx L_{\text{tank}}$ and $C \approx \frac{1}{\frac{1}{C_{\text{tank}}}+\frac{1}{C_{\text{para.total}}}}$ ($C_{\text{para.total}}$ refers to the total parasitic capacitance).

As mentioned in Eq. 14, low Q_{tank} results in a larger locking range at the expenses of large device ($C_{\text{para.total}}$) and total power consumption.

According to Eqs. 14, 15 and 16, if the minimum VCO working frequency is larger than the lower bound(or the maximum working frequency is smaller than the upper bound), the $\Delta\omega$ is too small for the $\sin\theta$ to reach -1 (or 1), thus shrinking the phase shift range. Which also means that, to achieve full 180° phase shift, the locking range needs to be located within the VCO frequency tuning range. In this work, the term "full 180° range" refers to "the frequency range of the input which can be shifted 180° by the phase shifter" to address this issue. Figure 7a shows how the full 180° range almost covers the entire frequency range. If the locking range is much larger and not ignorable, full 180° range will shrink, as shown in Fig. 7b. Assuming a wide locking range which is even larger than the frequency range as shown in Fig. 7c, the phase shift generated by this ILO can never achieve 180°. Meanwhile, it can be concluded that small locking range are more sensitive to tuning voltage (a small deviation on tuning voltage), which suggest that the large locking range topology exhibits a higher precision.

By taking the advantage of the unique characteristic of varactor capacitance curve, fine tuning of phase shift is now possible. Figure 8 shows the C-V curve of the varactor used in this work, which has a lower slope at around -0.4 V and higher slope at around 0 V. If the injection is just located at the frequency when varactor is biased

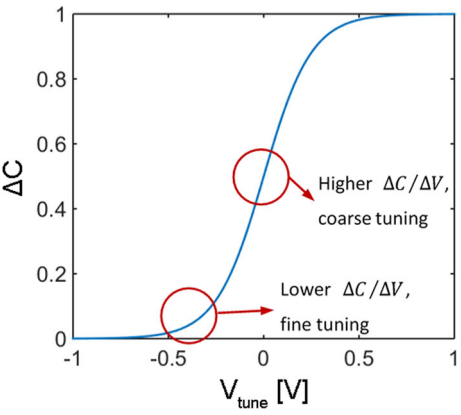


Fig. 8 A typical normalized varactor capacitance curve

at -0.4 V, the $\Delta C/\Delta V$ is small so that the phase changes smoothly. When V_{tune} is 0 V, phase tuning around this biasing condition is the best way to perform a coarse tuning. It should be noticed that the coarse tuning area exhibits better linearity than the fine tuning area [27], which suggests that the low $\Delta C/\Delta V$ area may also affect the linearity or precision.

High-quality factor means higher power efficiency, but it narrows the locking range down and the phase shifts are more sensitive to control voltage(harmful to the precision of phase shift). Besides, to maintain a high-quality factor at a given frequency, lumped elements of the circuit should be balanced and properly sized as suggested in Eq. 21. For example, if MIM capacitors (MIMs) are sized to be smaller (both capacitance and size) to increase the quality factor, the inductors need to be larger (usually both inductance and size). If quality factor is lowered to increase the precision, the power consumption is increased when using larger transistors. The increased parasitic capacitance that grows with power consumption will also narrow the frequency range down. Although a narrow frequency range results in a better precision, the frequency shift generated by model mismatch and small working bandwidth are additional issues.

3 Circuit Design

A guideline is therefore summarized to design the ILO based phase shifter with a good balance among these design considerations.

Step 1. Design a VCO circuit, which covers the desired working range. The quality factor of the LC tank can be determined subject to different applications. For example, to have a smaller silicon area, a small inductor without significant Q decrease is usually preferred.

Step 2. Determine the locking range. One of the three kinds of schemes, which are shown in Fig. 7, can be selected to set a goal in future quality factor optimisation. Larger locking range needs lower Q in small signal condition while smaller one needs higher.

Step 3. Tank optimization. Since the locking range has been determined, the tank should be adjusted to achieve the target quality factor. The sizing of both inductors and capacitors are possible solutions in tuning the tank quality factor. Higher quality factor usually means smaller inductors or MIMs but it may cause frequency up-shift. The width and length of each finger of MOS varactors can be reduced to have higher quality factor at the cost of narrow scaling range [6, 32]. Considering the large silicon area contributed by the inductor, a smaller inductor is always preferred, hence the change of inductors should be at the lowest priority.

Step 4. Circuit optimization. The negative resistance path consumes most of the power and brings large amount of parasitic capacitance. Back to step 3 once the path changes and repeat this procedure until a satisfied result is achieved. Offsets of frequency can be set to re-locate the locking range at the desired frequency range in low $\Delta C/\Delta V$ area at the cost of lower linearity, as shown in Fig. 7.

As a design example, an injection locked oscillator phase shifter(core of the circuit) is designed under this guideline. The K-band phase shifter is implemented in a commercial 0.13 µm RF CMOS technology. The schematic is based on the conventional topology shown in Fig. 6b. The input signal is injected at the tail transistor of the oscillator. Buffers are used to isolate the oscillator from output port, or power will be drained from the oscillation cycle and the circuit can hardly oscillate. Low power and small silicon area are the key considerations in this design. The LC tank is designed to have a mid-frequency range to solve frequency drift problems and with 180° frequency coverage. A high-quality factor is designed to achieve a low power operation.

3.1 Optimization

The inductor and capacitor should be properly sized to reach the target frequency at K-band. For example, 0.9 nH L_{tank} need about 1.9 pF C_{tank} to achieve around 24 GHz. Since the C_{tank} can be adjust in future without much area consideration and it is desirable to have a certain margin of potential parasitics, a smaller capacitor is used in this design.

Equation 14 suggests that both lowering the Q_{ext} and increasing the I_{inj} are helpful to enlarge the locking range. However, both solutions increase the I_{osc} and thus increasing power consumption [5, 12, 20]. The first and second schemes in Fig. 7 are preferred in this design. These schemes exhibit a slightly lower precision but a

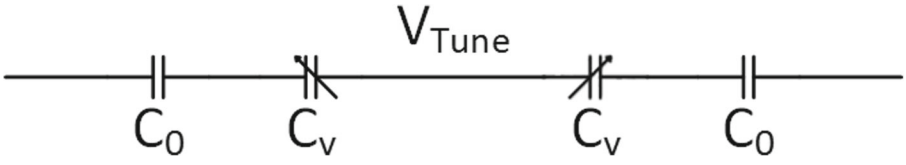


Fig. 9 Varactors are zero biased by blocking DC voltage from negative-resistance path

lower power (high Q) and full 180° phase shift are achieved compared with the third scheme in Fig. 7.

Further optimization can be performed as well. The varactors of the tank are shown in Fig. 9, where C_0 are used to keep varactors in zero voltage biasing. Since a mid-frequency range is chosen to improve the precision, small L varactors can be used to lower the scale ability. Ratios of C_0 and varactors also have related with the scale ability and quality factor, as illustrated in Fig. 10.

Supposing the capacitor circuit of the tank has a fix maximum capacitance, the capacitance of C_0 should be decreased when the fingers of MOS varactors increase (W and L remained) and vice versa. This will affect the scaling ratio and Q_C of the capacitor circuit. It can be seen in Fig. 10 that ratios goes down as fingers grow while Q_C has a maximum value at about 22 fingers. Since neither maximum Q nor maximum frequency range is the goal of optimisation, the number of fingers can be determined within [10, 22].

Usually, the negative-resistance path consumes most of the power of the phase shifter. Reducing the biasing current of the path is an essential way to lower the power consumption. That means the width or the number of fingers of the transistors should be kept as small as possible. However, changing the size of the transistor will have a side-effect, changing the parasitic capacitance. The C_{tank} has to be increased to maintain desired phase shifts within the same frequency range, since the parasitic capacitance has been lowered unconsciously. Besides, considering the efficiency of signal injection and redundancy of process variations, the path still need further adjustments.

Based on this design strategy, the parameters of instances of the tank can be determined as Table 1.

For simplicity, the input network is not perfectly matched to a perfect 50 Ohm match to save silicon area. In case there is a need of inject efficiency, the matching work can be added [8].

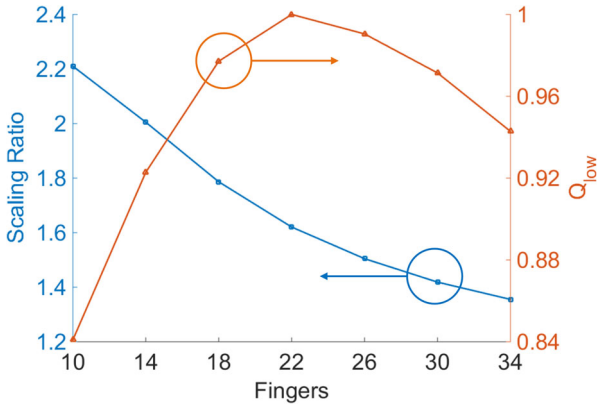


Fig. 10 Scaling ratio (*left*) and normalized Q_C of the capacitor circuit (*right*). The circuit has a fix maximum capacitance and C_0 vary along with fingers of varactors

Table 1 Instances of the tank

Varactors	Length = 300 nm, Width = 3.3 µm, Number of fingers = 11, Capacitance = from 37 to 126 fF
C_0	Length = 25 µm, Width = 20 µm, Capacitance = 490 fF
Inductor	Radius = 45 µm, Turn = 1, Inductance = 140 nH

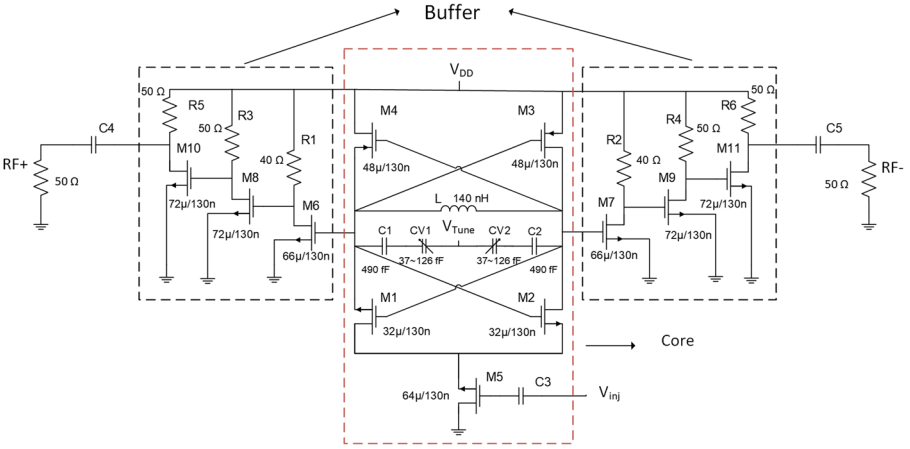


Fig. 11 Complete schematic of the proposed circuit

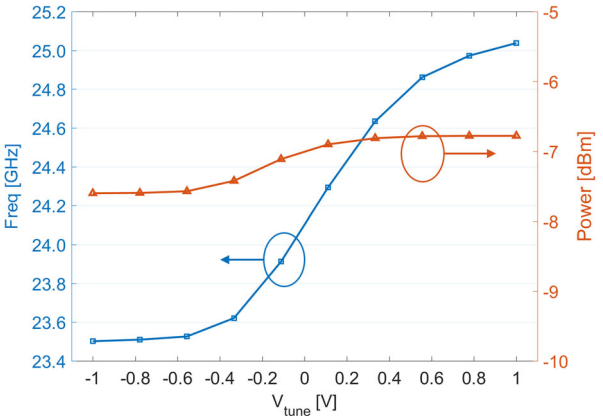


Fig. 12 Frequency and output power of output signal when V_{tune} from −1 V to 1 V

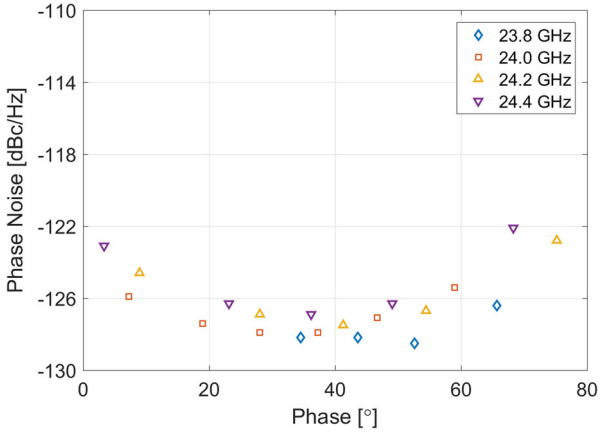


Fig. 13 Simulated phase noise at various frequency at 100 kHz offset

4 Simulation and Experiment Results

In this paper, the complete schematic of the proposed circuit is shown in Fig. 11. The V_{inj} is the injection port(also the input port) while the RF+ and RF− is both connected to the 50-Ohm port. V_{tune} is used to change the VCO working frequency. Buffers are added to isolate the core from output port. Under proper DC condition, the input of the circuit is connected to an input frequency source, the output will locked in to the input and generate tunable output with certain phase shifts. The proposed circuit is simulated using Cadence Spectre RF with EM extraction of critical interconnections.

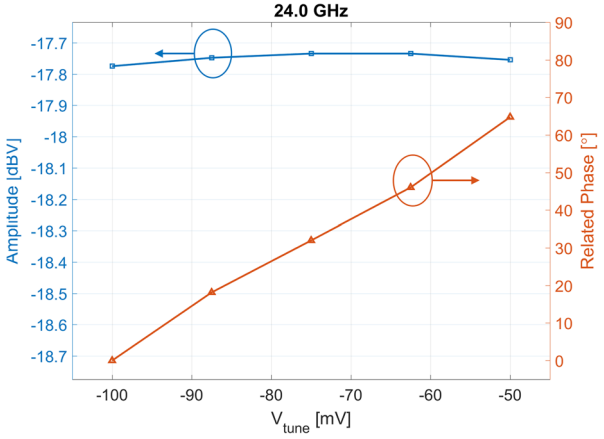


Fig. 14 Related phase and amplitude vs. V_{tune}

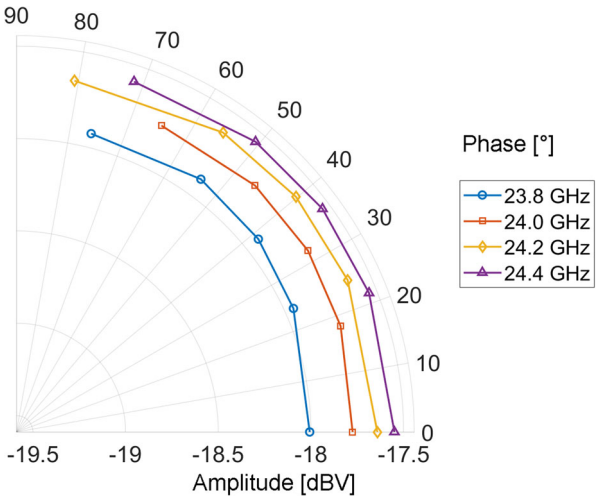


Fig. 15 Polar plot of output amplitude vs. phase at various frequency

The circuit is first simulated as a VCO. It can be seen in Fig. 12 that the frequency increase along with the V_{tune} and has a tuning range of about 1.5 GHz, from 23.5 to 25.0 GHz in periodic steady state (PSS) analysis.

To verify the stability of the phase tuning, post-layout transient simulations at different operating frequencies and tuning voltages are performed as well. In these simulations, the amplitude of the injected signal is set to be 550 mV. Figures 13 and 14 implies that with the increase of V_{tune}, phase increases as well, which verifies the theoretical analysis above. The increase rate of the phase is about 1.3°/mV. In this case, voltage steps around 8.65 mV can make 11.25° shifts. A polar plot, Fig. 15,

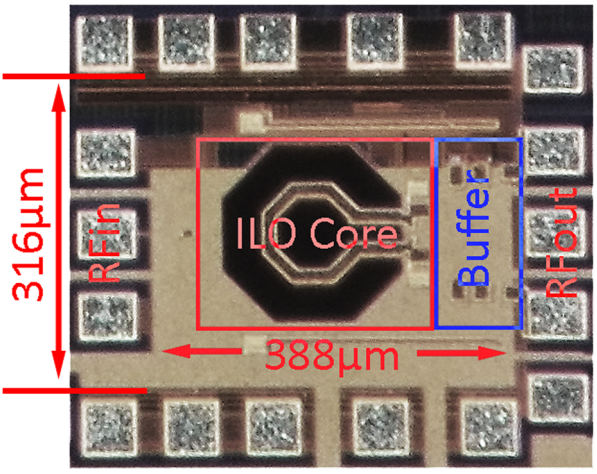
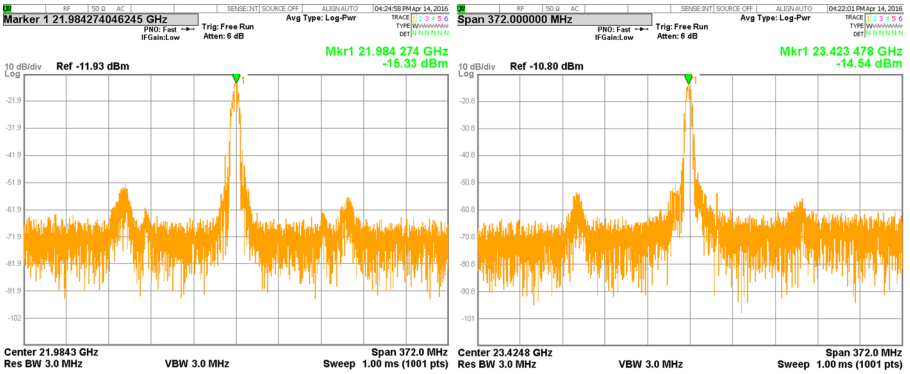


Fig. 16 Die photo of the phase shifter



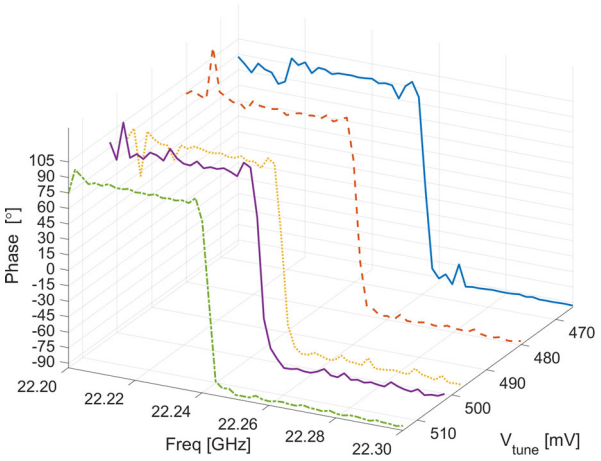
(a) Frequency when $V_{\text{tune}} = -1.2\text{V}$. (b) Frequency when $V_{\text{tune}} = 1.2\text{V}$.

Fig. 17 Frequency range of the VCO

also shows that the output amplitude variation is smaller than 0.5 dBV from 23.8 to 24.4 GHz. As shown in Fig. 13, the phase noise variation is smaller than 8 dB from 23.8 to 24.4 GHz at 100 kHz offset.

The circuit is fabricated using Grace Semiconductor Manufacturing Corporation(GSMC) 0.13 µm RF CMOS technology. Die photo of the circuit is shown in Fig. 16, which occupies an silicon area of about 540 µm × 620 µm (including I/O pads) or about 316 µm × 388 µm (excluding I/O pads). The on-wafer measurement is carried out using an Agilent MXA Signal Analyzer N9020A with a Cascade Probe Station. RF probes are attached to the GSGSG (output) pads on die. All measurement with a DC power consumption of ILO core of about 3.14 mW with a DC Voltage of 1.2 V. A spectrum measurement is performed at the very first stage. Figure 17 shows the ILO has a frequency range of 22 ∼ 23.4 GHz.

Fig. 18 Normalized data of phase shift vs. Freq at different V_{tune}



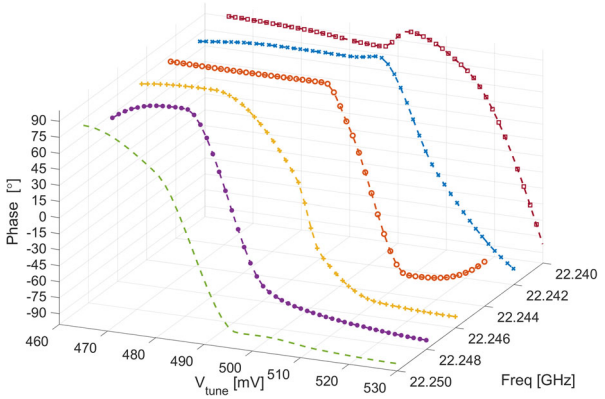


Fig. 19 Normalized data of phase shift vs. V_{tune} at different frequency

Compared Fig. 17 with Fig. 14, it is clear that the operating frequency and tuning range of the oscillator reduce considerably. This is due to insufficient EM extraction of interconnections and inaccurate device model at tens of GHz. The working frequency in measurement is about 22 to 23.4 GHz with a range of 1.4 GHz.

The S-parameter measurement is on an R&S ZVA67 network analyzer (VNA) with same Probe Station. RF probes calibrated through the on-wafer 12-term TOSM calibration are attached to the GSG(input) and GSGSG(output) pads on die. The measured S-parameters are shown in Figs. 18 and 19.

As can be seen in Fig. 19, with the increase of V_{tune}, phase shift drops and the range of it is about 180°, almost reach the theoretically maximum range. Compared

Table 2 Phase shifters using ILO method

	Tseng [26]	Grubinger [11]	Wu [27]	This paper
Working frequency	13 ∼ 15 GHz	14.6 ∼ 15.7 GHz (Input)/ about 30 GHz (Output)	42.75 ∼ 49.5 GHz	22 ∼ 23.4 GHz
V_{dd}	N/A	1.9 V	1 V	1.2 V
Phase shift range	179° (best)	280° (after doubler at 30 GHz)	Larger than 180°	about 180° (best)
Method	Continuous tuning	Continuous tuning with doubler	Discrete	Continuous tuning
Technology	0.18 µm CMOS	BiCMOS	65 nm CMOS	0.13 µm CMOS
Area	0.45 × 0.55 mm^2	N/A	N/A for single path	0.32 × 0.39 mm^2 (w/o pads)
Power	14 mW (ILO Core)	N/A	55 mW (Core), 35 mW (Auto tuning)	3.14 mW (ILO Core)

with the simulation results, the locking range is smaller and the increase rate of the phase is even larger, about 4°/mV. In this case, to be used as a phase shifter, the V_{tune} should be precisely controlled to achieve desired phase shift, e.g., a high 10-bit DAC to provide 1 mV steps. Table 2 summarizes the proposed work with literatures, which suggests the successful implementation of a low power phase shifter with a small silicon area.

5 Conclusion

An ILO-based phase shifters in K-band with continuous phase tuning is proposed. Several key design considerations have been analyzed to reach a design strategy of a low cost and low power operation at K-band. The proposed phase shifter is implemented using a 0.13 µm CMOS technology. Measurement results show that the proposed design is able to provide about 180 degree phase shift continuously while consuming 3.14 mW from a 1.2 V supply voltage.

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