J Infrared Milli Terahz Waves (2016) 37:737–752
DOI 10.1007/s10762-016-0265-x

CMOS-Compatible Room-Temperature Rectifier Toward Terahertz Radiation Detection

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Received: 13 May 2015 / Accepted: 10 March 2016 /
Published online: 22 March 2016
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Abstract In this paper, we present a new rectifying device, compatible with the technology of CMOS image sensors, suitable for implementing a direct-conversion detector operating at room temperature for operation at up to terahertz frequencies. The rectifying device can be obtained by introducing some simple modifications of the charge-storage well in conventional CMOS integrated circuits, making the proposed solution easy to integrate with the existing imaging systems. The rectifying device is combined with the different elements of the detector, composed of a 3D high-performance antenna and a charge-storage well. In particular, its position just below the edge of the 3D antenna takes maximum advantage of the high electric field concentrated by the antenna itself. In addition, the proposed structure ensures the integrity of the charge-storage well of the detector. In the structure, it is not necessary to use very scaled and costly technological nodes, since the CMOS transistor only provides the necessary integrated readout electronics. On-wafer measurements of RF characteristics of the designed junction are reported and discussed. The overall performances of the entire detector in terms of noise equivalent power (NEP) are evaluated by combining low-frequency measurements of the rectifier with numerical simulations of the 3D antenna and the semiconductor structure at 1 THz, allowing prediction of the achievable NEP.

Keywords Image detector · Terahertz · Rectifying antenna (rectenna) · Direct terahertz detection · Zero-bias detector · Room-temperature detector

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1 Introduction

Terahertz imaging and spectroscopy applications have great potential in time-domain spectroscopy [1], communications [2], security control [3], and biomedical imaging [4]. For this reason, in the past decades, great interest by the research community has been drawn toward this region of the electromagnetic spectrum, driving constant progress in the development of microwave and optical terahertz devices for the improvement of detectors in terms of noise equivalent power (NEP).

Currently, one of the main interests of terahertz technology is the development of low-cost, fast, highly sensitive, compact, and room-temperature detectors. For terahertz imaging applications, the integration in arrays in standard CMOS technology is important in order to take advantage of the capabilities of the integrated electronics. Attempts to reach a CMOS terahertz integrated imager reported in the literature followed two main approaches. The first one implies the use of a bolometer as the sensitive element and involves micro-electromechanical systems (MEMS) technology combined with CMOS in order to realize a thermally insulated suspended resistance. The bolometer is designed to transduce the electromagnetic energy in thermal form, resulting in a change in the temperature of the detector exposed to the radiation [5–7]. Proper thermal insulation (in particular from the antenna arms) may represent a relevant limit of this approach, together with a large noise component due to the polarization required by the reading process of the resistance value. A second approach adopts the use of the rectenna, with the integrated antennas [8–10] focusing the energy of the impinging electromagnetic field into a localized spot (active region) where the rectifying element is placed. In most cases reported in the literature, the rectifying element was realized by connecting the antenna arms to the MOS transistor drain and gate, i.e., in a nonlinear diode configuration. The connection between the antenna and the MOS structure is not trivial, and a relevant portion of the electric field concentrated in the spot is likely to spread out of the MOS channel. In particular, the transistor parasitic capacitances greatly reduce the rectifier efficiency. This forces the use of highly scaled technological nodes to make this solution suitable for terahertz-range applications.

This paper presents a new approach resulting from the direct integration of the antenna with a rectifying device obtained by modification of commercial CMOS Image Sensors (CMOS ISs) [11].

Nowadays, CMOS ISs mostly use a pinned photodiode as the photosensitive element of the pixel, that is, a p–n–p structure that collects photogenerated electrons and constitutes the charge-storage well (SW) dedicated to the charge integration during the exposure time [12]. We demonstrate that a modification of a limited region of the surface of the SW, placed in contact with the metal constituting the antenna, results in an efficient rectifying device, with no need to rely on deep submicron technology. The antenna coupled to the rectifying device (so-called rectenna) exposed to the electromagnetic radiation gives rise to charge injection into the SW, charge which is collected in the SW during the integration time. The rectifying device is designed to ensure the confinement of the accumulated charge within the SW, avoiding leakage currents toward the antenna pad and thus allowing operation in the time integration regime. In the readout cycle, the integrated charge is transferred to a “floating diffusion” capacitance, FD, inducing a voltage difference to be read by the integrated circuitry. Commonly, a transistor in source–follower configuration senses voltage variations at FD. The sensitivity of the complete system is strongly dependent on the capability of the rectenna to focus the electric field onto the rectifying element. In order to quantify this capability, the

electric field enhancement factor, FE, defined as the ratio between the magnitude of the resulting electric field on the rectifying device and the magnitude of the incoming electric field, is used.

Planar antennas, such as dipoles, bowties, spirals, and log-periodic antennas [13], were widely used in previous works.

In this paper, we propose to adopt the technological approach described in [14] that makes it possible to integrate a three-dimensional antenna directly on the surface of the chip, by means of MEMS technology, and ensures a very low parasitic capacitance because of the distance between the antenna spires and the silicon wafer.

This work is organized as follows. In Section 2, the overall structure of the proposed detector and each of its parts are presented along with a discussion of the operating principle of the detection system; further, the numerical analysis of both electromagnetic and solid-state elements of the system is reported. In Section 3, a test structure for on-wafer characterization of the proposed rectifying device is introduced and the resulting experimental data are presented and discussed. Combining the theoretical results and experimental data reported in the paper, we finally validate the rectifier model and determine an effective evaluation of the expected detector NEP at 1 THz. The conclusions follow in Section 4.

2 Detector Structure and Principle of Operation

The proposed detector architecture can be realized on the backend of the silicon wafer hosting a CMOS IS. As shown in Fig. 1, the detector consists of the combination of a 3D antenna, underneath which a nanometric metallic whisker is positioned, of a rectifying device created at the edge of the nanometric metallic whisker, and of a semiconductor charge-storage well underneath the rectifier. Each functional part is described in the following subsections.

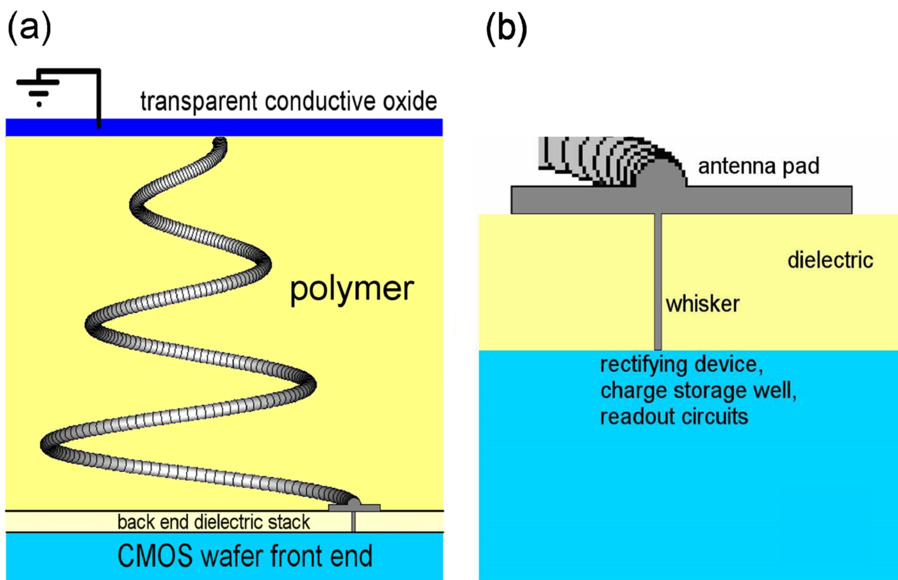


Fig. 1 **a** The geometry of the conical tapered helix antenna. **b** Details of the antenna pad and the metallic whisker facing the storage well

2.1 Three-Dimensional Antenna for Terahertz Range

An antenna suitable for terahertz frequencies has dimensions compatible with chip dimensions. We proposed a 3D version which can be fabricated by means of MEMS technology, compatible with CMOS technology, based on controlled metal layer release [14]. In particular, the proposed antenna is a conical tapered helix in monopole configuration. The antenna is realized on the top of the backend inter-metal dielectric (IMD) stack of a silicon CMOS wafer containing the IS readout electronics and the rectifying device and is connected to the latter by means of the bonding pad and a thin metallic whisker crossing the IMD layer, as shown in Fig. 1b. An ultimate functionality of the nano-whisker is the enhancement of the focusing of the impinging terahertz field into the small region where the rectification occurs, allowing the sensitivity of the system to be greatly increased, as will be evaluated in the following. To confer a mechanical support to the antenna, an electrically insulating polymer that is transparent to the terahertz radiation is spread onto the chip surface around the antenna. A layer of terahertz-transparent conductive oxide (TCO) must be placed above the polymer in contact with the antenna edge (see Fig. 1a), in order to ensure an external path for the extraction of collected electrons to ground. An accurate analytical model of FE in the tapered helix antenna derived in [15] makes it possible to calculate the antenna FE. Numerical electromagnetic simulations of the antenna were performed with the finite-difference time-domain method, with results reported in [15]. The adopted simulation setup reproduces the electromagnetic condition occurring in reception mode, that is, when the terahertz wave impinges on the structure. With this setup, a monochromatic plane wave at a frequency of 1 THz with right-hand circular polarization and unitary electric field amplitude $E_i = 1$ V/m reaches the antenna. The assumption of a metallic ground plane is justified by the fact that a standard metallization level available on the CMOS process backend can be used underneath the antenna to realize the metallic shield. A narrow window under the antenna finally allows the whisker to reach the semiconductor. In the simulations, the ground plane is separated from the whisker by a thin dielectric layer of thickness $T_D = 10$ nm with a dielectric constant of silicon $\varepsilon_{Si} = 11.9$.

The nano-whisker radius, R_W, and height, H_W, strongly affect FE. In Fig. 2, the results obtained for a three-turn tapered helix antenna with a wire diameter of 2 μm, planar turn spacing of 8 μm, external turn diameter of 100 μm, vertical pitch of 50 μm, and three values of

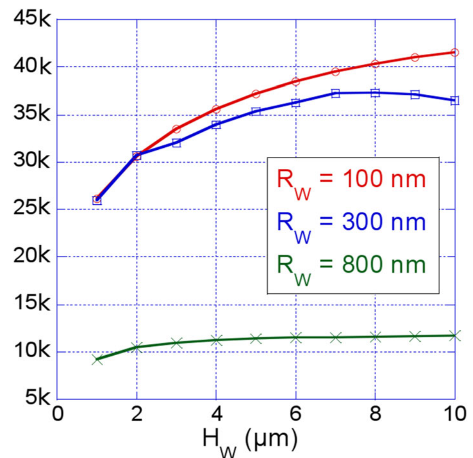


Fig. 2 Simulated electric field enhancement factor in a three-turn tapered helix rectenna for different values of whisker radius: $R_W = 100$ nm (*line with circles*), $R_W = 300$ nm (*line with squares*), and $R_W = 800$ nm (*line with crosses*)

the whisker radius, R_W, are reported [16]. All of the R_W values shown are realizable in standard CMOS technology. As expected, we found a relevant increase of FE with the reduction of R_W, obtaining values that dramatically exceed the FE values currently available in the literature; in fact, FE obtained by planar antennas widely used in integrated solutions is at least one order of magnitude lower. Saturation of the FE increase occurs for relatively large values of R_W (about 100 nm). This last dimension is compatible with the resolution of a standard CMOS photolithography process for via contacts, which ensures that it is not necessary to adopt deep submicrometric technologies for whisker fabrication.

Further increments of FE can be obtained by using higher H_W values. Numerical analysis shows that with a proper design of both the helical monopole and nano-whisker, values of FE as high as 40,000 can be reached.

2.2 Rectifying Device

The semiconductor structure implemented in the detector must be able to perform several operations: first, the rectification of the high-frequency radiation; second, the accumulation of the rectified charge into a storage capacitance; and third, allowing the charge readout. Overall, the structure must be realized by means of a technology compatible with CMOS IS.

In most cases reported in the literature [17, 18], the rectifying element was realized by connecting the antenna arms to the drain and gate of a MOS transistor in diode configuration, which produces the necessary nonlinearity. The connection between the antenna and the MOS structure is not trivial, and it has been verified that a relevant portion of the electric field concentrated in the spot by the antenna is likely to spread out of the MOS channel. A great improvement in the efficient use of a focused electric field can be achieved by a rectifying device created just at the base of the antenna nano-whisker. In this position, the device, with vertical extension of a few tenths of a nanometer, is directly crossed by the antenna electric field, with minimal dispersion.

In CMOS image detectors, the SW is constituted by an n^--type doped region surrounded by the p-type region of the substrate. In addition, a p^+-type implanted surface layer is commonly used to separate the SW from the defective semiconductor surface [19]. The depth and width of the SW are around 2 μm.

Choosing to create the rectifying device just along the surface of the SW improves the collection of the rectified charge but imposes the condition that its structure must maintain the continuity of the potential barrier of the SW itself.

In the proposed structure shown in Fig. 3, the edge of the metal whisker is in contact with the p^+-type implanted surface layer, forming a metal–semiconductor junction. The antenna edge thus becomes a part of the electronic device. The semiconductor of the SW completes the structure of the rectifier.

The work function of the metal must be such as to ensure a position of the Fermi level similar to those in highly *n*-doped silicon; for example, titanium (Ti) with a work function of 4.33 eV, a material compatible with CMOS technology, can be used as the terminal portion of the whisker. With the Ti work function, the contact gives rise to a rectifying junction with the "p^+-Si" layer; hereafter, this is referred to as the "first junction". The p^+-Si layer under the whisker must have a controlled thickness, typically a few tenths of a nanometer, which can be easily implemented by choosing the dose and energy of the ion implantation. The p^+-Si layer and the weakly doped region, n^--Si, of the SW form a "second junction". Due to its reduced thickness, the p^+-Si region becomes almost completely depleted of carriers, giving rise to a

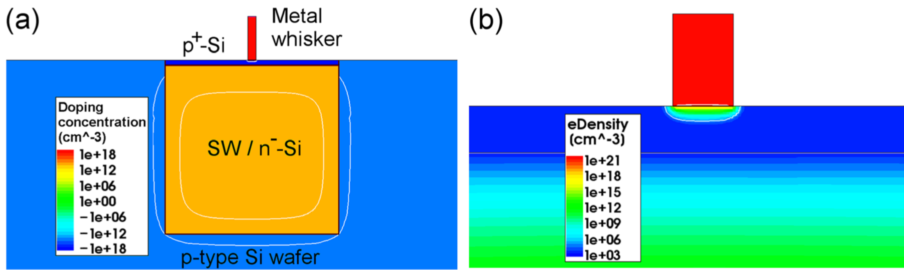


Fig. 3 **a** Schematic representation of the doping distribution of the proposed semiconductor device for the rectification and charge accumulation. Positive and negative values correspond to n-type and p-type doping, respectively. **b** Simulation of electron density, at zero-bias condition, in the region of the rectifying barrier

reduction of the barrier, to a value of 0.3–0.5 eV with respect to the silicon conduction band inside the SW. The doping concentration of the p^+-Si region can be modified in order to adjust this barrier height.

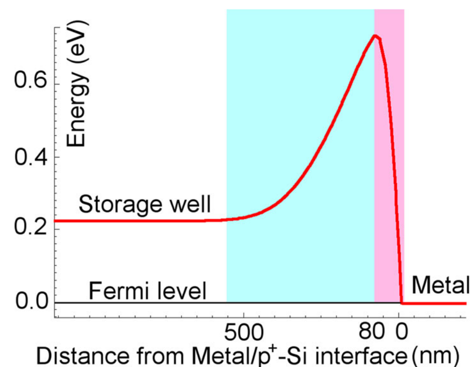
A sketch of a 1D cut of the lower energy level in the conduction band (along the vertical cut through the center of the device) is reported in Fig. 4 and shows the presence of two low opposite barriers. This double barrier maintains the continuity of the potential barrier around the SW under the antenna too.

Since the structure is supposed to be zero-biased to avoid bias noise, the rectifying barrier must be sufficiently low (0.3–0.5 eV) in order to produce an appreciable rectified current, even under the presumably very low voltage variations induced by the terahertz radiation. The reduced barrier height is sufficient to limit the charge leakage, since the large parasitic capacitance between the SW and the ground-connected p-type substrate ensures a very limited variation of the potential of the SW, once charged.

This structure also shows a rectifying behavior arising from the different extensions of the two depletion regions, the very short one of the first junction and the much more extended one of the second junction, as schematically indicated in Fig. 4 with light color areas: light pink color to indicate the depletion zone of the first junction and light blue color to indicate the depletion zone of the second junction.

The rectifying effect can be explained as follows: the electric field variations induced by the antenna and focused by the whisker on the device induce variations in the voltage drop through the depleted zones of the two barriers. The majority of the voltage drop occurs through the second depletion region, mainly extending into n^--Si of the SW and is much

Fig. 4 One-dimensional sketch of the conduction band energy through the junction (vertical cut in the center of the device) and depletion regions



wider than the short depletion region of the first junction. As a consequence, with a positive voltage applied to the metal, a reduction in the barrier of the second junction occurs, and electrons preliminarily stored in the SW can be extracted. On the contrary, with negative voltage, far fewer of the electrons present in the metal layer are injected into the SW, since the barrier of the first junction is reduced by a much smaller amount due to its shorter extension.

Numerical simulations of the semiconductor device were performed by means of Synopsys Sentaurus TCAD tools. The simulation engine makes it possible to perform 2.5D simulations, setting the area of the metal contact to 100 nm × 100 nm. As a reference, these contact dimensions are achievable by means of a 193 nm DUV photolithography process used for the test structure presented in the next section.

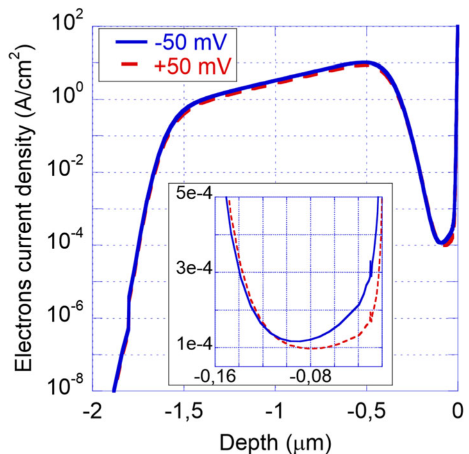
Figure 5 shows the 1D cut of the absolute value of electron current density through the device, across the rectifying junction and through the SW. The current is induced by two voltage ramps of +50 and −50 mV with a rise time of 1 ps. At the metal contact and within the SW, the current density is the same for both signs of excitation. Inside the barrier, the electron current is dramatically lower, substituted by displacement current.

The residual conduction current through the barrier is many orders of magnitude below the absolute current injected at the contact. This residual conduction current density presents a difference of about 50 % under the two excitation ramps with opposite signs. The difference in conduction current with forward and reverse voltages of the two ramps is highlighted in the inset of Fig. 5. The difference produces the rectification effect. The results depicted in Fig. 5 were obtained using a hydrodynamic model approximation in order to take into account the limited time of flight of electrons. Monte Carlo simulations [20] indicate that in the terahertz range, the ballistic propagation length is comparable with the barrier width. Nevertheless, a consistent similarity can be found with a simple drift diffusion model as pointed out in [21].

The value of the conduction current through the barrier is extremely dependent on the effective carrier depletion in the p^+-doped layer and thus on its thickness and doping concentration. For this reason, the electron extraction efficiency will be more precisely evaluated from measurements in the next section.

On the other hand, from the simulation, we may obtain an evaluation of the electric field that is the origin of the barrier depletion. This evaluation is reliable since it is only related to the dimensions of the dielectric structure. For example, in the simulation reported in Fig. 5, where

Fig. 5 Electron current density along a 1D cut by the center of the RF contact at the end of the positive (*solid line*) and negative (*dashed line*) voltage ramp. *Inset*: magnification of the electron current density in the double barrier



a p^+-Si layer of 30 nm was adopted, the absolute density of the current feed at the center of the contact is about 2000 A/cm^2. As stated before, this current becomes almost entirely displacement current within the barrier. We can thus calculate the intensity of the electric field of 1.26 kV/cm.

3 On-Wafer Measurements

3.1 Setup Description and Measurements

We developed a test structure to verify the rectification properties of the detector. The test structure, reported in Fig. 6, does not include the antenna and is designed for tests at frequencies well below the terahertz range in order to permit measurements with standard probes and the available instrumentation. The signal is applied by a radio frequency generator to emulate the excitation coming from the receiving antenna. The choice of this measurement setup may appear to limit the obtainable information to low frequencies; however, in the following, we will show that it is still possible to provide an evaluation of the expected results in the terahertz range by combining low-frequency measurements and numerical simulations.

The test structure was expressly realized with minor changes to a standard configuration of a CMOS photodetector using the Aptina/ON Semiconductor 0.15 μm technology node. The additional step consists in an extra p-type doping implantation below the whisker in order to trim the barrier height. Such an implantation can be performed through a properly designed window through which the metal used for the realization of contact, Ti, is also deposited. Further, metal deposition is performed to obtain a via between the pad metallization and the rectifying contact. Finally, at the top metallization level, three pads are realized with dimensions suitable to be contacted by RF microprobes. In particular, Cascade ACP40-GSG-150 microprobes were used during the measurements. The external ground pads are electrically connected to the doped substrate surrounding the SW by means of via holes and ohmic contacts.

Figure 7 shows the equivalent circuit of the measurement setup. The RF voltage generator is obtained from a vector network analyzer, VNA. An RF signal is applied by means of the pad and whisker to the metal layer of the junction. A Keithley 617 pico-ammeter, shown by the circled capital A, is connected to the floating diffusion contact, FD, of the transfer gate

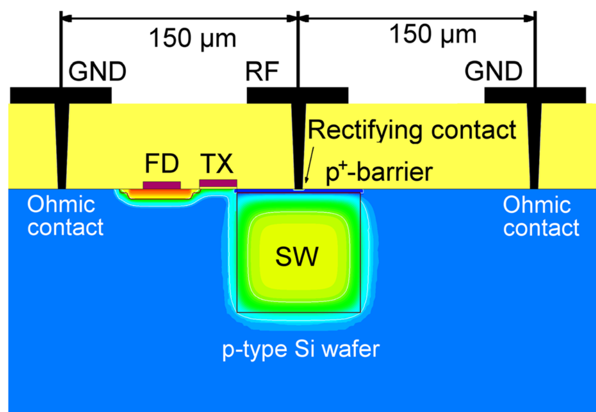


Fig. 6 The schematic description of the test structure. Dimensions of RF pads and SW are not to scale

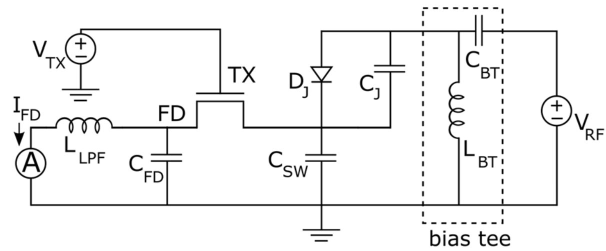


Fig. 7 Equivalent circuit of the measurement setup

transistor, TX. The pico-ammeter is decoupled by a low-pass filter, represented here by the series insertion of an inductance, L_{LPF}. Capacitances of FD and of SW are denoted as C_{FD} and C_{SW}, respectively. The rectifying device is modeled by a diode, D_J, and junction capacitance, C_J.

Activation of the TX permits the flow of the rectified current toward the pico-ammeter. A bias tee at the input of the VNA, formed by L_{BT} and C_{BT}, ensures the DC continuity toward ground and zeroes the bias voltage from the RF source side.

In the RF measurement setup, an Agilent E8363B VNA was first used to measure the input scattering parameter and then to apply the RF power to the test structure. The RF power was kept constant at each measurement and changed step by step during the test. Figure 8 reports the measured S_{11} parameter at the RF pad, obtained with an input power of −10 dBm, indicating sufficient matching to test the rectification capability at frequencies between 1 and 40 GHz. Given the power level of the RF generator, with an output impedance of 50 Ω and the frequency, the peak voltage applied to the device could be determined by the use of the measured values of S_{11}.

The structure was tested at 1 and 40 GHz. In the following, we will refer to such measurement frequencies as RF, in order to distinguish them from the terahertz-range operation frequency of the detector.

Figure 9 reports the rectified current measured by the pico-ammeter versus the RF power applied to the test pad. The TX gate voltage is equal to 4 V for both curves and ensures that TX is in the ON state.

A linear approximation of the curves in Fig. 9 in the non-saturated region can be used to evaluate the system sensitivity, calculating the power necessary to reach the noise level. We

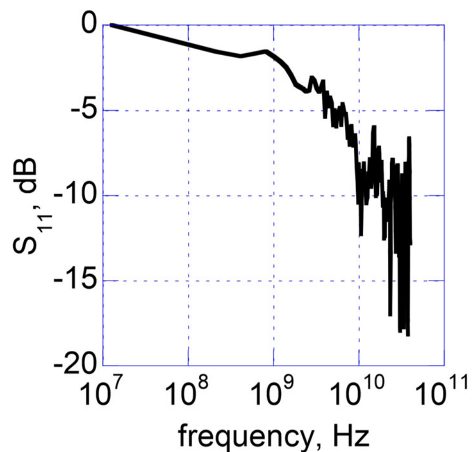


Fig. 8 Scattering parameter S_{11} measured on the RF test pad

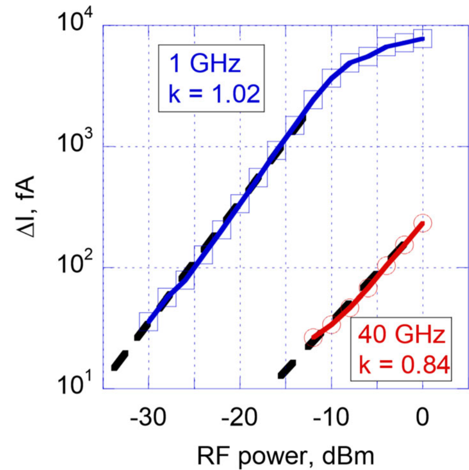


Fig. 9 Measurement of the current variations in the time integration regime at 1 GHz (*dashed line with squares*) and 40 GHz (*dashed line with circles*)

approximate as linear the relationship between the RF power expressed in decibel–milliwatts, P_{dBm}, and ten times the logarithm of the current, I_{dBA}, as given by

$$P_{\mathrm{dBm}} = P_{\mathrm{dBm},0} + k\left(I_{\mathrm{dBA}} - I_{\mathrm{dBA},0}\right), \tag{1}$$

where $P_{\mathrm{dBm},0}$, $I_{\mathrm{dBA},0}$, and the coefficient k can be calculated from geometrical regression of the measured data. This approach makes it possible to account for eventual nonlinearities in the rectification. From the measurement at 1 GHz, we obtained $k = 1.02$, while at 40 GHz, the coefficient resulted in $k = 0.84$.

We must point out that the rectifying device used in this structure was not optimized from the point of view of the noise due to injection of spurious electrons into the SW. The presence of a metal in contact with the silicon surface, beside the SW, introduces a large density of defects, which facilitate thermal generation of carriers and electrons crossing the barrier by hopping. In order to limit this negative effect, the final device should include a layer of SiOx, 70-Å thick, interposed between the metal and the semiconductor. This material passivates defects at the semiconductor interface, while allows penetration of electric field from the antenna, and permits the conduction of the rectified current by hopping through SiOx layer defects.

Since the SiOx structure was not yet included in the fabrication of this first device, in order to achieve a realistic evaluation of the noise expected, we measured the noise in a typical SW at 25 °C. In Fig. 10, we report, with red square marker, rms noise after the electronic reading and with blue diamond the dark current of the photodiode, versus the integration time. Both quantities are expressed in electrons delivered by the SW. rms noise reflects a constant contribution due to readout electronics, then increases with the square root of time. Charge due to the dark current increases linearly with time. Data lead to an approximated value of noise of 5 el/s.

With this value, we may calculate the noise equivalent power in the test setup, as the power necessary to create a rectified current equal to the noise current, obtaining −76.6 and −65.1 dBm, at 1 and 40 GHz, respectively. These values are extrapolated from measurements using (1). They could not be actually measured, due to the pico-ammeter setup limiting the detectable current to few fA.

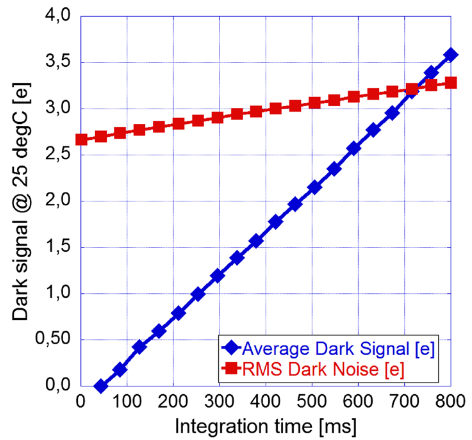


Fig. 10 Current noise measurements on a typical SW in CMOS IS. (*Red square marker*) rms noise after the electronic reading and (*blue diamonds*) the dark current of the photodiode. Reported versus the integration time. Both quantities are expressed in electrons delivered by the SW

3.2 NEP Evaluation

In order to extend the interpretation of measured results toward higher frequencies that are not covered by the actual measurements, we introduce two different equivalent circuits. The first one allows an evaluation of the behavior around the terahertz range and is obtained from TCAD hydrodynamic simulation in AC analysis mode. The simulations provide the frequency-dependent values of parallel capacitance and conductance, as seen from the metal contact, toward the rectifying junction and the SW, in the structure shown in Fig. 3a. The results of frequency analysis are reported in Fig. 11.

Both the equivalent capacitance and the equivalent conductance show strong frequency variations. Between 100 MHz and 1 THz, the results can be interpreted by a series equivalent circuit, with frequency-independent elements, namely C_S and R_S. This first equivalent circuit has a straightforward physical interpretation; it indeed can represent the presence of a resistance due to the weakly doped SW, in series, of the dielectric capacitance of the double barrier. The capacitance between the SW and the semiconductor substrate can be neglected, since it is much larger than C_S.

We notice that above 1 THz, the simulations in Fig. 11 predict a slowdown of the decrease of the parallel capacitance value and an increase of the conductance. We assume that this effect is due to the ballistic behavior of electrons through the double barrier [22, 23]. This effect, which eventually implies an improvement of the rectification capability, deserves an

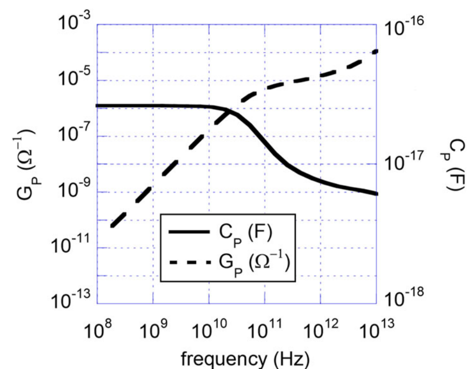


Fig. 11 Simulation of the frequency dependence of capacitance (*solid line*, *right y-axis*) and conductance (*dashed line*, *left y-axis*) equivalent circuit of rectifying structure and SW

autonomous investigation that is beyond the scope of this paper. As a conservative assumption, we will neglect the ballistic behavior in the following.

In the RF measurements performed at 1 and 40 GHz, we refer to a second, more general equivalent circuit, described in Fig. 12. The rectifying device represents only a part of this circuit. This second equivalent circuit is essential in order to evaluate the electric field really imposed on the rectifying junction during the measurements. In this circuit, C_{PAD} represents the capacitance of the test pad, and R_{p+} represents the series resistance toward the ground pads, due to the p^+-Si layer and to the p-type substrate. This part of the circuit is coherent with the S_{11} measurement reported in Fig. 8 showing a cutoff frequency of 1 GHz. The series equivalent circuit of the rectifying device is assumed to be connected in parallel to C_{PAD} due to the very short dimensions of the SW compared to the distance between the two RF pads and thus to the length of the resistive path toward the ground. From the simulation in Fig. 11, we determine $C_S = 2.7\text{E}{-17}$ F and $R_S = 50$ kΩ. The resulting cutoff frequency related to the time constant $\tau_S = C_S R_S$ is 120 GHz, and thus, it can be neglected in the evaluation of RF measurements.

From the model in Fig. 12, we infer that at low frequency, since the voltage drop across R_S can be assumed to be negligible, the voltage amplitude at the pad capacitance is equal to the voltage at the rectifying device, V_S. The voltage that must be applied to the double barrier in order to achieve a rectified current equal to the noise current can be calculated from the NEP in the test setup, obtained in the previous section. We obtain V_S values of 208 and 53 μV from measurements at 1 and 40 GHz, respectively.

We must now recall that the rectified current is induced by the periodic asymmetric deflection of the double barrier, and thus, it depends, in a constant manner, at both low frequencies of the measurements and at the terahertz frequencies, on the variations of the electric field inside the barrier itself. The equivalent circuit in Fig. 12 thus indicates that in order to achieve a given junction current, at any frequency, it is necessary to have the same voltage drop across C_S. Above the cutoff frequency of 120 GHz, due to the presence of R_S, it is the voltage drop across the entire rectifying device which must increase. On the contrary, below 120 GHz, the SW resistance can be neglected and the voltage drop across the rectifying junction is equal to the voltage drop at the C_{PAD}.

As a conclusion, with this approximation, the electric field variations necessary to equate the noise can be calculated at 1 or 40 GHz and can be extended up to the terahertz range using the expression:

$$E_S = \frac{C_S V_S}{A_S \varepsilon_0 \varepsilon_S}, \tag{2}$$

where A_S is the contact area in TCAD simulation. We obtain E_S, of 18 and 4.6 mV/cm from measurements at 1 and 40 GHz, respectively. This difference also affects the final determination of NEP at 1 THz. The difference basically relies on different values of k in Fig. 9. We believe this is a

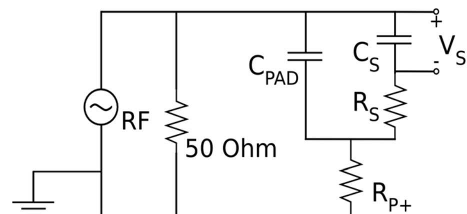


Fig. 12 The equivalent circuit of the test structure

characteristic behavior of the device related to its intrinsically 3D structure and certainly deserves further investigation. However, in this introductory paper, we provide a non-exhaustive description in order to derive a preliminary evaluation of the possible performances of the new device.

In the proposed terahertz detector, the electric field inside the barrier is imposed by the antenna. In this case the RF test pad is substituted by the antenna and the resistance of the p^+-doped layer is not present. In a numerical evaluation, the antenna can be taken into account through its equivalent circuit reported in Fig. 13, formed by the current generator, I_{ant}, in parallel to the admittance, Y_{ant}, and coupled with the equivalent circuit of the rectifying device, in this case reduced to C_{S} and R_{S}.

The equivalent circuit in Fig. 13 shows that the amount of the current delivered to the load by the antenna decreases as the admittance of the rectifying junction decreases at lower frequencies, as indicated by the simulation in Fig. 11. This effect gives rise to a reduction of the electric field variations in the junction. The value of FE of 40,000, calculated in [16], can be considered as ideal since in this calculation, only the series capacitance under the antenna was considered, while the series resistance R_{S} was ignored. In order to evaluate the relationship between the external radiation and the effective electric field variations applied to the junction, we must introduce an effective field enhancement factor, eFE. The eFE is calculated as the ideal FE multiplied by the ratio of current dividers between the antenna admittance, Y_{ant}, and the junction admittance, $Y=(R_{\mathrm{S}}+1/j\omega C_{\mathrm{S}})^{-1}$ and that between Y_{ant} and Y_0. The admittance Y_0 is evaluated from the structure adopted in the FE calculation, which modeled the device only as a dielectric gap, T_{D}, $Y_0=j\omega C_0=\varepsilon_0\varepsilon_{\mathrm{S}}A_0/T_{\mathrm{D}}$. The area A_0 is that of the whisker, with the base radius of 100 nm as used by simulations in [15]. Both current dividers must be normalized by the area of respective capacitances in order to express the electric field dependence. Due to the relatively low value of the junction admittance with respect to the antenna admittance, eFE can be approximated by the ratio between the dissipative equivalent junction admittance and its ideal value, leading to a simple single-pole low-pass behavior, as indicated in (3):

$$\mathrm{eFE}=\mathrm{FE}\left|\frac{\frac{1}{A_{\mathrm{S}}}\frac{Y}{Y_{\mathrm{ant}}+Y}}{\frac{1}{A_0}\frac{Y_0}{Y_{\mathrm{ant}}+Y_0}}\right|\simeq\mathrm{FE}\frac{A_0}{A_S}\left|\frac{Y}{Y_0}\right|=\mathrm{FE}\frac{A_0\,C_{\mathrm{S}}}{A_S\,C_0}\frac{1}{\sqrt{1+\omega^2{C_{\mathrm{S}}}^2{R_{\mathrm{S}}}^2}}. \tag{3}$$

We can obtain the external electric field impinging on the antenna, E_{ext}, dividing the electric field calculated inside the C_{S} capacitance by eFE. Substituting the expression of C_0, we obtain

$$E_{\mathrm{ext}}=\frac{V_{\mathrm{S}}C_{\mathrm{S}}}{A_{\mathrm{S}}\varepsilon_0\varepsilon_{\mathrm{S}}}\frac{1}{\mathrm{eFE}}=V_{\mathrm{S}}\frac{1}{T_{\mathrm{D}}}\frac{\sqrt{1+\omega^2{C_{\mathrm{S}}}^2{R_{\mathrm{S}}}^2}}{\mathrm{FE}}. \tag{4}$$

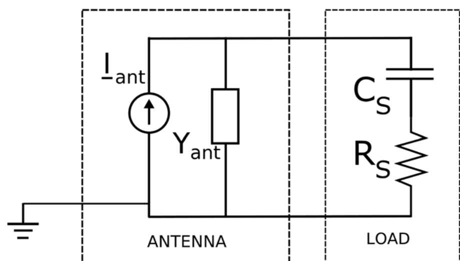


Fig. 13 The equivalent circuit of the antenna and of the detector

From (4), the power of the incoming radiation can be derived. Assuming a radius of 100 μm for the antenna and its geometrical area is equal to the effective radiation area, we finally calculate the NEP at 1 THz equal to 35 pW/Hz$^{1/2}$ and 0.6 pW/Hz$^{1/2}$ for $k = 1.02$ and $k = 0.84$, respectively. Being measured at a higher frequency, the NEP value of 0.6 pW/Hz$^{1/2}$ seem to be the most appropriate for an evaluation of the device behavior at 1 THz. We add a further consideration that at higher frequencies, a fast flux of carrier from the SW toward the barrier takes place, which actually reduces the barrier width leading to an increment of rectification efficiency. The reduction of the barrier width can also be inferred from the lower value of k that indicates a deformation of the barrier at higher power values. This effect is evident from simulations of the detector structure performed at the different frequencies and deserves further studies.

Comparison of these values with results presented in literature is reported in Table 1. All values derived from the literature are obtained from measurements at room temperature.

4 Conclusions

In this paper, a new CMOS-compatible direct-conversion terahertz radiation detector operating at room temperature is presented and experimentally evaluated. We demonstrate that a modification of a limited region of the surface of the CMOS IS pixel, placed in contact with the metallic antenna pad, provides an efficient rectifying device. The antenna and the rectifying device, that is, the rectenna structure, exposed to electromagnetic radiation give rise to charge injection into the storage well of the image detector that is collected during the integration time. In the readout cycle, the integrated charge is transferred to a capacitance and sensed by the integrated circuitry. Overall performances in terms of NEP were evaluated by on-wafer RF measurements. The study of the 3D antenna combined with the intimately integrated detector indicates that an increase of the sensitivity can be achieved compared with devices using 2D antenna patterns. The presented evaluation shows an extremely promising NEP value. The first evaluation of the proposed structure suggests that the final 1-THz NEP may be lower than what is currently reported as the minimum values in the literature. There is no need for scaling toward deep sub-micrometer technological nodes, since the rectifying device is essentially a vertical structure and the CMOS only provides the necessary integrated reading electronics.

Table 1 Comparison with literature results

Technology	Freq (THz)	Power cons. (μW/pixel)	Max RV (*V/W*)	Min MEP (pW/HZ$^{0.5}$)	Reference
This work	1			0.6–35	
65-nm bulk	0.86	2.5	115 K at 0.86 THz	12	[24]
			140 K at 0.86 THz	100	
	0.9		56.6 K at 0.9 THz	470	
65-nm SOI	0.65	–	1 K at 0.65 THz	54	[25]
65-nm bulk	1	–	800 K at 1 THz	66	[26]
0.13-μm bulk (SBD)	0.29	375	323 K at 0.28 THz	29	[27]
0.15-μm bulk	4.1	–	11 K at 4.1 THz	1330	[17]
0.25-μm bulk	0.6	5500	80 K at 0.6 THz	300	[18]

Acknowledgments The authors would like to thank Aptina for allowing the realization of the test structure in the state-of-the-art CMOS IS technology.

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