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Wafer-scale fabrication of penetrating neural microelectrode arrays

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Abstract The success achieved with implantable neural interfaces has motivated the development of novel architectures of electrode arrays and the improvement of device performance. The Utah electrode array (UEA) is one example of such a device. The unique architecture of the UEA enables single-unit recording with high spatial and temporal resolution. Although the UEA has been commercialized and been used extensively in neuroscience and clinical research, the current processes used to fabricate UEA's impose limitations in the tolerances of the electrode array geometry. Further, existing fabrication costs have led to the need to develop less costly but higher precision batch fabrication processes. This paper presents a wafer-scale fabrication method for the UEA that enables both lower costs and faster production. More importantly, the wafer-scale fabrication significantly improves the quality and tolerances of the electrode array and allow better controllability in the electrode geometry. A comparison between the geometrical and electrical characteristics of the wafer-scale and conventional array-scale processed UEA's is presented.

Keywords Utah electrode array (UEA) · Neural interface · MEMS · High aspect ratio · Wafer-scale fabrication · Microelectrodes

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1 Introduction

Advances in silicon micromachining, biomaterials, and system technologies have made feasible the progressive development of sophisticated devices to interface with the nervous system. Microelectrode arrays have been developed to stimulate and /or record from populations of neurons for a long period of time (Kipke et al. 2003; Anderson et al. 1989; Drake et al. 1988; Bai et al. 2000; Mojarradi et al. 2003; Robinson 1968; Musallam et al. 2007; Schanne et al. 1968; Gagne & Plamondon 1987; Chowdhury 1969; Fofonoff et al. 2004; Jones et al. 1992; Campbell et al. 1991). The UEA is one example of such a neural interface that can selectively communicate with large numbers of individual neurons (Jones et al. 1992; Campbell et al. 1991). Figure 1 shows schematic image of the UEA. The UEA consists of a ten by ten square grid of 1.5 mm long electrodes with 400 μm spacing. One hundred Pt/TiW/Pt bond pads are deposited on the back surface of these arrays, and one hundred 1.25 mil insulated gold wires are bonded to these pads and to a percutaneous connector for connection to external electronics. The tip of each electrode is metalized with iridium oxide to facilitate electronic to ionic transduction. The entire array, with the exception of the tip of each electrode, is insulated with a biocompatible Parylene-C.

In order to use an electrode array for stimulation and recording, uniformity and reproducibility of the electrode electrical and mechanical characteristics are of great importance. The geometrical architecture of the electrodes in the array defines their electrical and mechanical properties. This necessitates the need to develop a fabrication technology that is robust and that can produce uniformly shaped implantable microelectrodes with uniformly exposed tip sizes of the same order of magnitude as

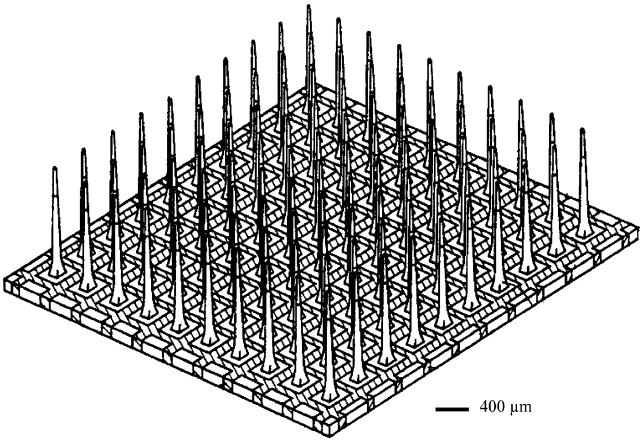


Fig. 1 Schematic image of the Utah electrode array

the neurons with which the electrode communicates (i.e., in the realm of micrometers).

Over the last two decades, microelectrodes have been produced as 2D and 3D arrays, mainly using silicon, glass, and metal microtechnologies (Kipke et al. 2003; Anderson et al. 1989; Drake et al. 1988; Bai et al. 2000; Mojarradi et al. 2003; Robinson 1968; Musallam et al. 2007; Schanne et al. 1968; Gagne & Plamondon 1987; Chowdhury 1969; Fofonoff et al. 2004; Jones et al. 1992; Campbell et al. 1991). Past attempts at manual assembling multiple sharpened metal (tungsten wire probes) and glass capillary probes into a linear array or a 2D matrix have been reported (Robinson 1968; Musallam et al. 2007; Schanne et al. 1968; Gagne & Plamondon 1987; Chowdhury 1969). However it is difficult to repeatedly control the geometry of such finished arrays. Furthermore the fabrication process to produce complex electrode arrays is labor intensive and is associated with low yields. Silicon based microelectrode arrays have previously been fabricated using surface micromachining (Michigan Electrode Array-MEA). The MEA is a 2D multichannel microelectrode array. Several of these 2D probes have been micro-assembled into 3D arrays (Kipke et al. 2003; Anderson et al. 1989; Drake et al. 1988; Bai et al. 2000). These probes are fabricated using fixed lithographic mask sets (typically a 5–10 mask process), which is also expensive and time consuming for small production volumes.

Conventionally, fabrication of the UEA's has been carried out on a single array basis. Many of the manufacturing processes were unrefined. Furthermore, the manufacturing technique is time consuming, and yields less consistency in results than desired. With the greater experimental usage of the UEA, and the eventual need for production level requirements, the existing array-scale fabrication technique provides inadequate quality, repeatability, and throughput. In order to mitigate the challenges of the current array fabrication technology, the hypothesis for this work was to develop wafer-level processes for the UEA fabrication, however owing to the high aspect ratio (15:1) and non planar surface formed by the tips of the electrodes, the development of wafer-scale fabrication of the UEA poses many engineering challenges. In this paper, we present a wafer-scale manufacturing technique for fabricating the UEA, we identify problems and limitations associated with the array-scale fabrication and then report on some manufacturing innovations that will mitigate these problems. Wafer-scale fabrication of the UEA has several advantages including a simplified manufacturing process, higher yield, lower production costs, and reduced fabrication time. More importantly, the novel processing techniques not only allow higher throughput but also lead to more consistent electrode shape, more uniform and controlled tip exposure and uniform impedance of the electrodes. It is envisioned that these technological advancements in the UEA fabrication would in turn lead to better understanding of observed variations in physiological results.

2 Methodology

Figure 2 present schematic view of the process flow for wafer-scale fabrication of the UEA. In this paper a 75 mm in diameter wafer was used which can result in production of 49, 10×10 (one hundred electrodes), arrays.

2.1 Back-side dicing

The starting material for the UEA is a 2000±25 μm thick (total thickness variation is ≤10 μm), 75 mm diameter *p*-type, c-Si (100) wafer with a resistivity of 0.01–0.05 Ω-cm, Fig. 2(a). In order to electrically isolate each electrode from its neighbors a Disco dicing saw, DAD 640, is used to make a 10×10 matrix of kerfs, Fig. 2 (b), on the polished side of the wafer. This step is called "back-side dicing." Later these kerfs will be filled with an insulating material. The dicing process involves making 11 cuts with a pitch of 0.4 mm. The silicon wafer is then rotated by 90^0, and additional sets of 11 cuts are made with the same pitch. The 11 orthogonal cuts in each direction make one UEA of 10×10 matrix and depending on the diameter of wafer large number of arrays can be accommodated in one wafer. A Semicon blade (part# FSN1600508) was used for the back-side dicing. All the cuts are 0.5 mm deep. Figure 3 shows a schematic view of a 75 mm wafer after back-side dicing to illustrate the pattern of dicing. The wafer is then ultrasonically cleaned in acetone, methanol, and then rinsed in DI water.

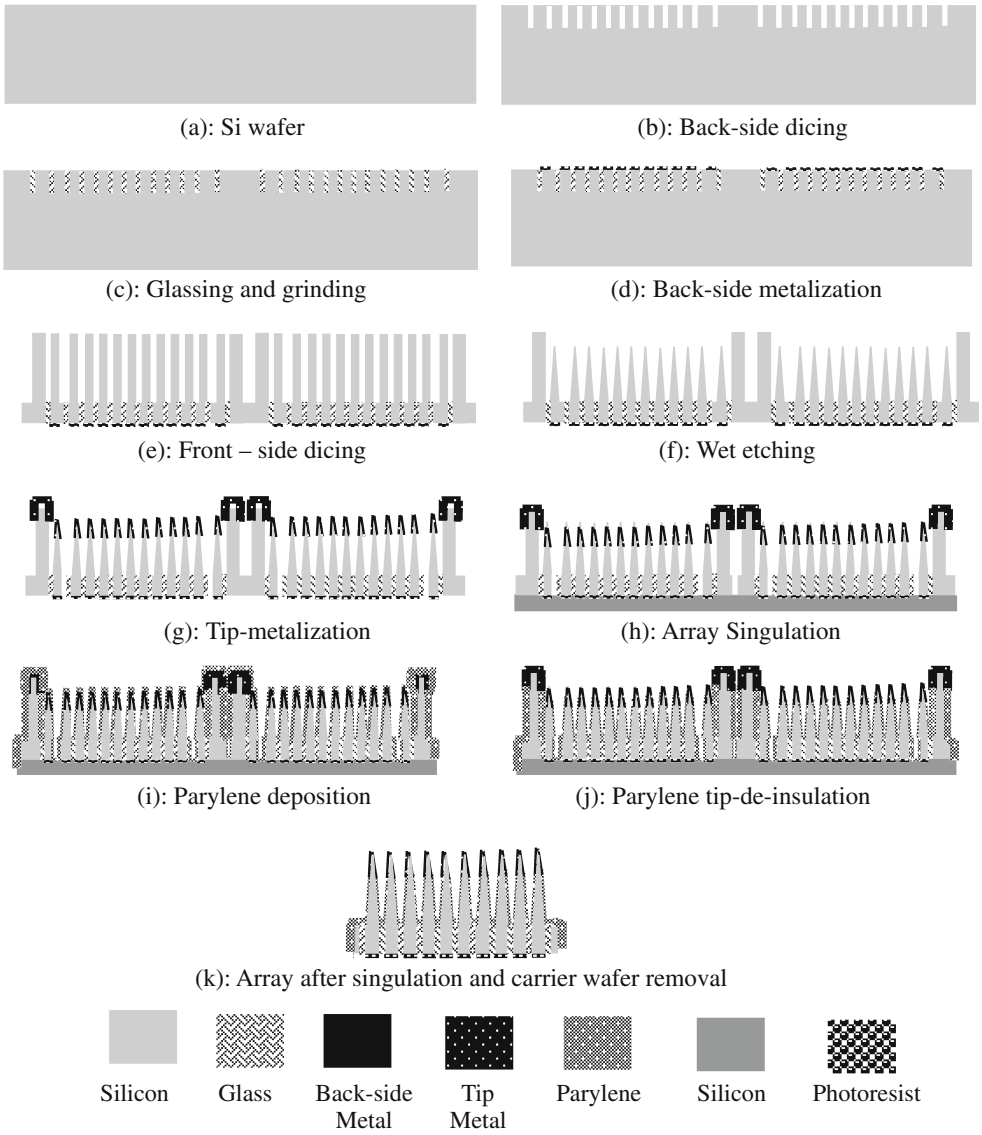


Fig. 2 Schematic view of the process flow for wafer-scale fabrication of UEA

2.2 Glassing

To fill the diced kerfs with an insulating material a Corning 7,070 glass frit (325 mesh) is used, Fig. 2(c). This glass has a coefficient of thermal expansion close to that of silicon, and exhibits high volume resistivity (Jones et al. 1992). The glass powder is mixed to a slurry in methanol (1.2:1 by wt.) and applied to the grooved surface of the wafer, where it flows into the kerfs. The wafer is then dried in a oven at 60°C for 15 min. The wafer is then placed into a covered ceramic boat and loaded into a dental vacuum furnace (Ney Centrion Company, model # GQA0208104). A mechanical pump is connected to evacuate the furnace chamber, and the glass coated wafer is held under vacuum for 10–15 min to degas. The process is repeated 3-4 times until 3–5 layers have been coated. After this the wafer is sintered at 1,150°C. This allows the glass to melt and completely fill the saw kerfs.

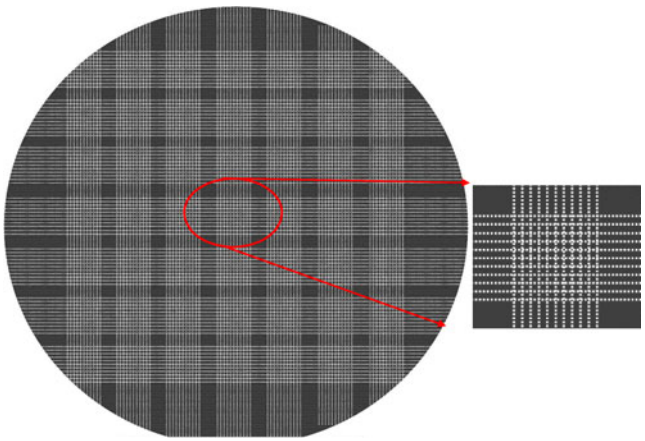


Fig. 3 Schematic top-view of 75 mm diameter wafer after back - side dicing

2.3 Grinding

The glassing procedure leaves an uneven layer of excess glass on top of the silicon wafer which is removed using a grinding process, Fig. 2(d). The grinding is achieved in three steps. In the first step the bulk glass is removed and the wafer is leveled in the dicing saw, using a resin bond, 0.6 mm thick blade. This step removes all the glass from the surface exposing the silicon surface with glass debris. In the second step, the wafer is lapped and polished using a customized stainless steel holder. The wafer is mounted on the holder using a semiconductor grade, wafer adhesive. The wafer is then manually lapped on 240, 320, and 600 grit size Silicon Carbide (SiC) paper for approximately 15 min for each grit. The SiC papers are mounted on a pottery wheel and wafer is manually lapped while the wheel is rotating. In the third and final step, the wafer is polished using a 9 μm and then 3 μm diamond suspensions on hard perforated cloth (Texmat AK8672) which is mounted on the pottery wheel. The wafer is finally polished in 1 um diamond suspension on medium nap polishing cloth (Microcloth AK 7222. This leaves a crosshatch pattern of insulating glass embedded on one side of the polished silicon wafer.

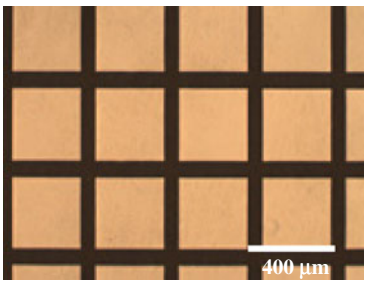
Figure 4(a) shows an optical image of back- side of the UEA after grinding process while Fig. 4(b) shows the rms roughness and total thickness variation (TTV) measured on the back-side (between the glass traces) across different wafers. The surface roughness measured in different wafers was less than 100 nm. The glass was found to be typically less than 1 μm below the silicon surface and the reason for the difference in height between glass and silicon was the different lapping polishing rate for silicon and glass. While the total thickness variation (TTV) was ≤69 nm for all wafers. The greatest advantage of this process is the simplicity and low cost to achieve mirror polished silicon surface.

2.4 Back-side metallization

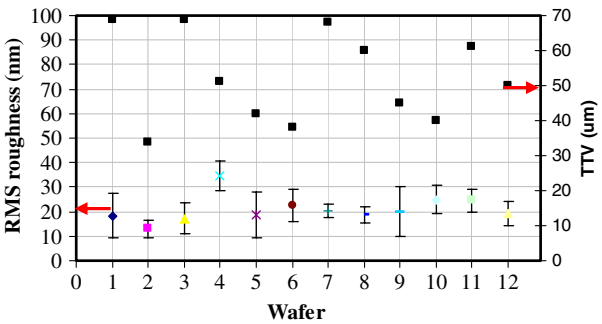
In order to have electrical connection to each electrode, metal bond pads are formed on the back side of each electrode and this step is called back-side metallization, Fig. 2(d). To have reliable interconnects, the bond-pad metal should make ohmic contacts and provide robust adhesion with the underlying silicon substrate. The stress of the metal stack should be minimum. Also the metallization scheme on the array should be suitable for wire bonding using specific type of wires and wedges. In order to make electrical contact to the individual electrode shanks in the array, a unique metal stack sequence, Pt/TiW/Pt, was DC sputter deposited (TM Vacuum SS-40C-IV multicathode sputtering system) onto the glassed side of the wafer, and a lift-off process is used to create a 300×300 μm square contact pad on the back side of each of the glass surrounded 'islands' of silicon. The thicknesses of each metal layer were 240/620/480 nm, respectively. The first Pt layer is selected for ohmic contact and silicide formation, the TiW is chosen as a diffusion barrier, and the second Pt layer is selected as bonding material for wire-bonding. Low film stress parameters were obtained by varying the sputtering power and pressure (Kim et al. 2008). The Ti layer was sputtered in argon ambient at a chamber pressure of 20 mTorr and at power of 90 W for 5 min. The first Pt and second Pt layer were deposited at a chamber pressure of 11 mTorr and at power of 90 W for 12 and 31 min, respectively. TiW was deposited at a chamber pressure of 11 mTorr and at power of 45 W for 52 min. Figure 5 shows a plot of resistance between two neighboring Pt/TiW/Pt bond pads in different wafers. The bond pads have good adhesion with the substrate and passed the scotch tape test.

2.5 Front-side dicing

To form the columns that will eventually form the needle shaped electrodes, a Disco dicing saw, DAD 640, is used to cut two orthogonal sets of deep kerfs into the non-glassed side of the wafer, called "front-side," Fig. 2(e). Each cut is made directly opposite of a glassed kerf, and the depth of the cut is set so that the blade just barely cuts into the glass. This leaves a number of tall (1.5 mm) square silicon columns, each separated from its neighbors by a layer of dielectrically insulating glass. A 10×10 matrix of rectan-



(a)



(b)

Fig. 4 (**a**) Optical image of back-side of the UEA after lapping and polishing. (**b**) Plot of rms roughness and TTV measured in different wafers

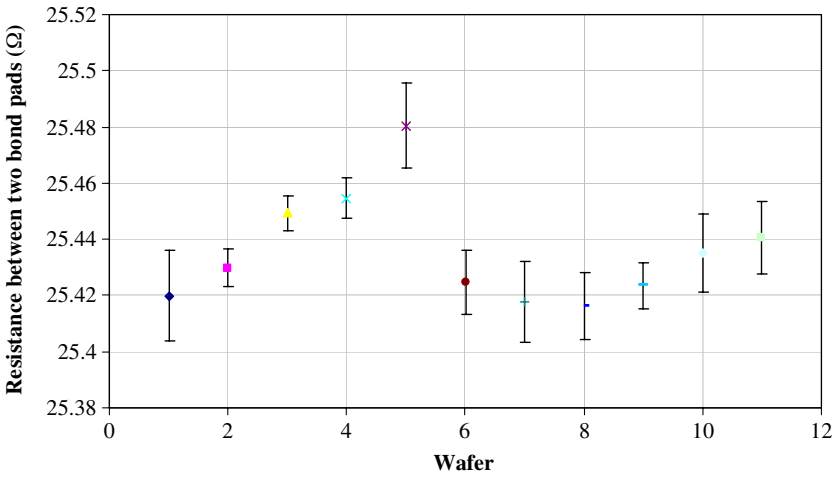


Fig. 5 Plot of contact resistance of Pt/TiW/Pt bond pads in different wafers. The 12 wafers measured had good uniformity in resistance

gular columns was created by making thirteen 0.5 mm deep orthogonal cuts, with an index of 0.4 mm, on the non polished side of the wafer. A Semicon nickel alloy diamond blade (part# FSN2400511) was used for dicing the columns. The 13 orthogonal cuts yielded 10×10 rows of electrodes plus one extra row of electrodes on all four sides of the array. Apart from the extra row of electrodes, sacrificial features called the *fins* and the *corner posts* were fabricated, as shown in Fig. 6. The extra row of electrodes, *fins* and the *corner posts* are designed to enhance uniformity in electrode geometry in the array during wet etching.

2.6 Wet etching

An important and early step in the array fabrication is the etching of electrodes to produce needle-shape electrodes with sharp tips. The square columns fabricated by dicing are subsequently transformed into rounded and pointed electrodes through a wet etching process (mixture of HF (49%)-HNO_3 (69%) in a ratio of 1:19) that rounds the column corners and sharpens the tip, Fig. 2(f). Etching of the UEA has two-steps consisting of (1) *dynamic* and (2) *static* etching (Campbell et al. 1991). Traditional etching processes are performed on a single array, and the etching conditions are not optimized. Furthermore the process is not only time and labor-intensive but also produces variable geometries of electrodes within an array. In order to achieve geometrical uniformity in electrodes, a wafer-scale etching method was developed and optimum etching conditions were investigated (Bhandari et al. 2010). A 100 mm diameter Teflon wafer holder was developed for wafer-scale wet etching of the 75 mm diameter diced wafers. Also a custom designed Teflon jig was built to continuously vent the gas evolved during *static* etching (Bhandari et al. 2010).

The wafer-scale etching method offers several advantages, like substantial reduction in the processing time, higher throughput and lower cost. It takes 30 min to etch a 75 mm diameter wafer containing 49 arrays, while to etch same of amount of arrays by old process it would take 25 h. More importantly, the method increases the geometrical uniformity from electrode to electrode within an array, and from array to array within a wafer. Figure 7(a) presents SEM image of wafer containing UEA after *dynamic* etching and Fig. 7(b) presents an SEM micrographs of UEA after static etching.

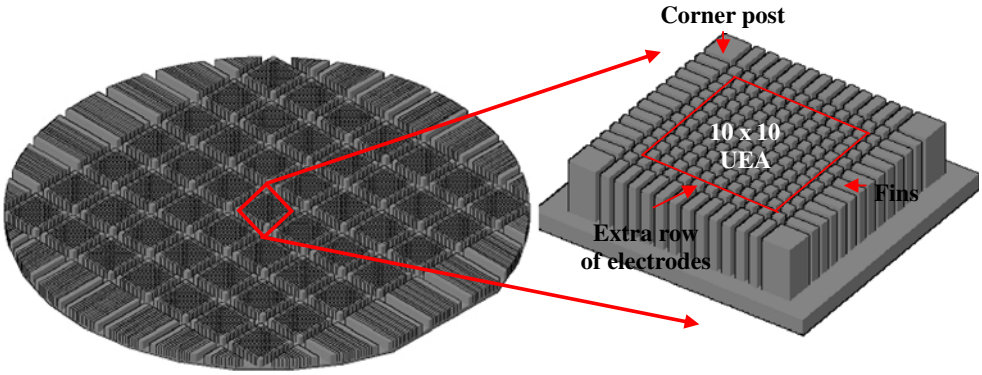


Fig. 6 Cartoon image of a 3-inch wafer illustrating the front-side dicing

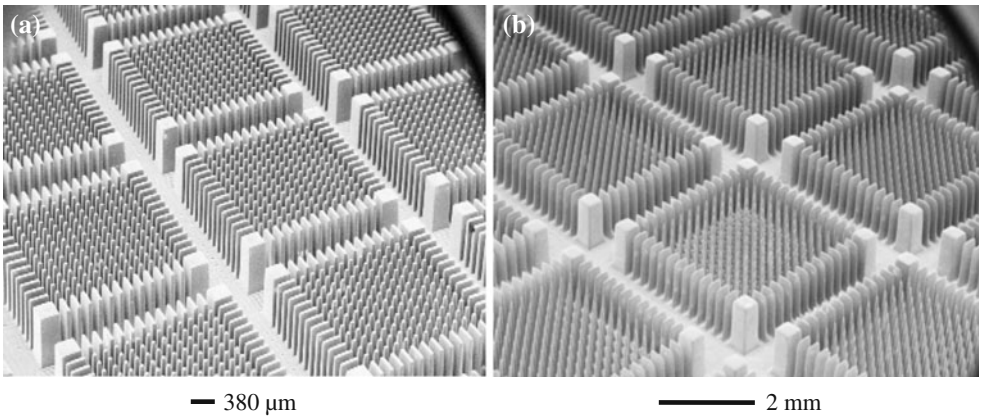


Fig. 7 SEM micrograph of the UEA after wet etching. (**a**) UEA after wafer-scale *dynamic* etching, (**b**) after wafer-scale *static* etching. Note the corner post and fins at the periphery of each array. These additional features help achieve uniformity in electrode geometry

2.7 Tip metallization

To facilitate charge transfer from electrode to neural tissue the electrode tips are coated with a metal layer, Fig. 2(g) and the process is called "tip metallization." Conventionally, Ti/Ir was sputter deposited and then electrochemically activated to form activated iridium oxide film (AIROF). A thin aluminum foil was used as a masking layer to protect the base of the device from sputtered metal. The aluminum foil is pierced by the electrodes to obtain the desired exposure. This is a single array process and cannot be implemented on wafer-scale (Campbell et al. 1991). Furthermore, aluminum foil masking process is manual and labor intensive.

A sputtered iridium oxide film (SIROF) process has been developed for tip metallization of the UEA. The unique properties of SIROF depend on the surface structure and the morphology of the films; hence, the process parameters have been optimized to procure efficacious and stable films. A detail description is given in previous publication (Negi et al. 2008).

In order to deposit SIROF on the tips of the UEA on wafer-scale, a novel photoresist based masking method was developed; Figure 8 illustrates the process flow. The tip exposure is controlled by a combination of two factors namely, spinning speed during photoresist coating (Manduca et al. 2001) and Ultra Violet (UV) light exposure time. Four layers of thick photoresist (AZ4620) were spin coated at 500, 400, 300 and 200 rpm. The wafers were kept in vacuum for 30 min to remove the bubbles. The wafers were pre-baked at 95°C for 5 min and then UV exposed for 30 s. The resist was developed in AZ 400 K for 2.5 min. The wafers were hard-baked at 50°C for 7 h. Figure 9 shows an SEM image of the UEA after photoresist coating on wafer-scale.

An adhesion test was carried out to validate the affect of photoresist on the adhesion of SIROF on the electrode tips. To test the adhesion of SIROF on the electrode tips, PDMS sample was developed in accordance with ASTM (American Standard of Testing and Materials) protocol. The Young's modulus of PDMS was measured by Instron 3360 and was found to be 220 kPa which is ten times more than the Young's modulus of nerve, typically 34 kPa (Manduca

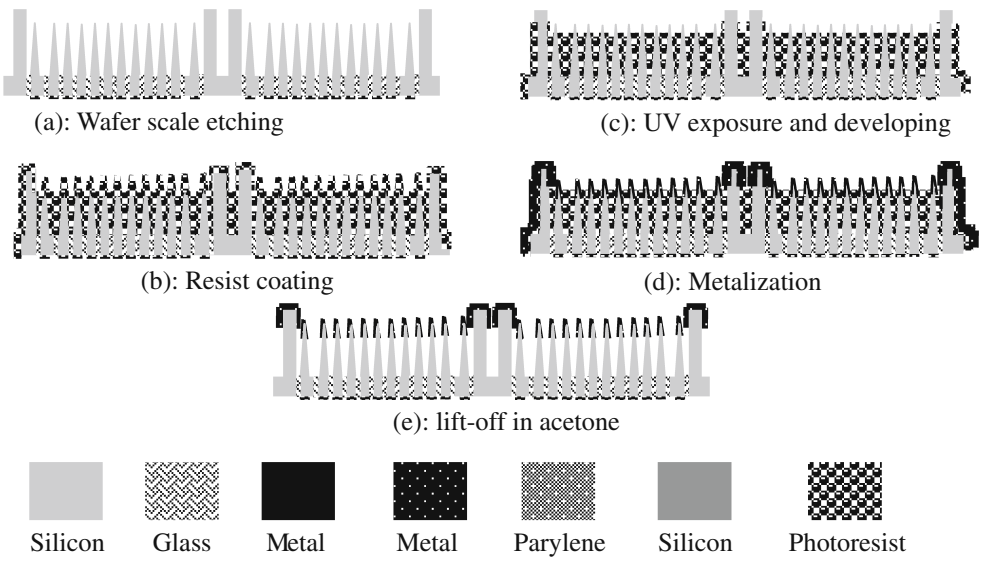


Fig. 8 Process flow for tip metallization on wafer scale using photoresist as a mask

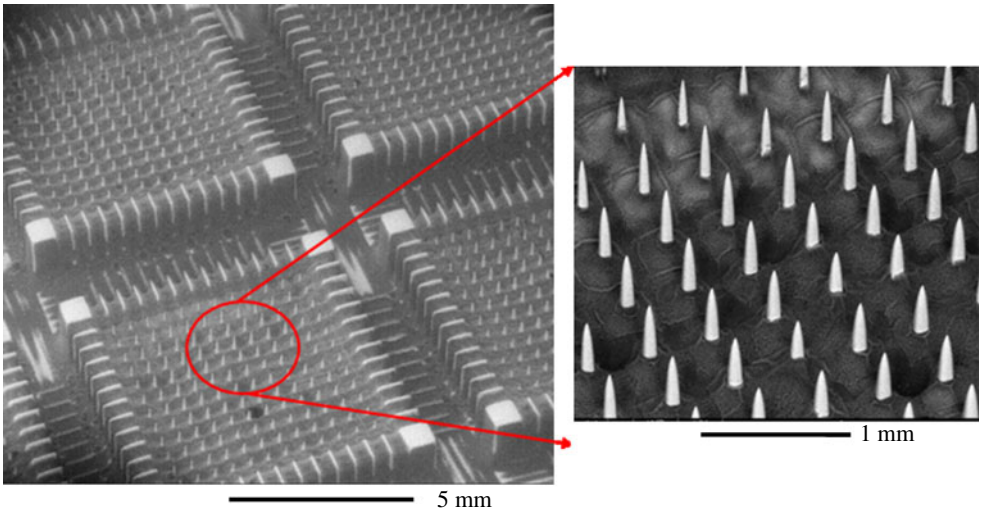


Fig. 9 SEM image of the UEA immersed in photoresist before tip-metalization. Note the sacrificial features (extra row of electrodes, fins, corner posts) surrounding the UEA. These additional features help achieve uniformity in tip exposure during photoresist coating (Bhandari et al. 2009a)

et al. 2001). Five SIROF coated UEAs were inserted into the PDMS sample using a pneumatic impulse insertion technique that has been used successfully in cerebral cortex, and that has been described elsewhere (Rousche & Normann 1992). The impact inserter was positioned to apply a pressure of 200 kPa on the array to facilitate insertion direction during impact. Each array was inserted five times to a depth of 1.5 mm. The tips of each array were examined under SEM pre and post poking. No delamination of tip metal was seen under the SEM indicating good adhesion of SIFOF to silicon.

2.8 Parylene deposition

To improve the biocompatibility of the electrode array, Parylene-C is deposited in each individual UEA by using low-pressure chemical vapor deposition (LPCVD), Fig. 2(i) (Hsu et al. 2007). It is desired that each electrode array should be completely covered (except the back-side, which needs to be wire-bonded) with the encapsulating layer. This in-turn requires that each array should be singulated prior to the deposition. This prior singulation impedes wafer-scale fabrication of the UEA, particularly Parylene deposition and de-insulation of electrode tips. Furthermore in order to promote the adhesion of Parylene to the underneath substrate the UEA is subjected to wet silanization process prior to Parylene deposition (Hsu et al. 2007). Though both the Parylene deposition and silanization are batch processes they often lead to broken electrodes while handling.

A method was developed, in which the wafer, Fig. 2(h), was mounted on a carrier wafer, by using a wafer grip (Dynatex, lot# 09290701-01-JA). Then the arrays were singulated into 10×10 electrode arrays, using dicing saw. The blade height was adjusted to 2 mm (wafer thickness) so that arrays remain intact on the carrier wafer. The wafer was then coated with Parylene-C using chemical vapor deposition (CVD) process, a detailed description of which is given elsewhere (Hsu et al. 2007). Adhesion promoter, Silquest A-174® silane (GE Silicones Inc., WV, USA), was applied on the wafer prior to Parylene-C deposition. 3 μm thick Parylene-C films were deposited using a Paratech 3000 Labtop deposition system (Paratech Coating, Inc., CA, USA). Parylene-C dimer precursor was acquired from Cookson Electronics Equipment, USA. The dimer was vaporized at 130°C and subsequently pyrolized into reactive monomers at 670°C. The base pressure before Parylene dimer sublimation was less than 10 mTorr.

2.9 Deinsulation

The Parylene-C encapsulation must be removed from the active electrode tips so that contact can be made to neural tissue, Fig 2(j). This is the most critical step as it defines the active area, called tip exposure. The geometrical surface area of the electrode tip has a significant impact on its electrical characteristics and selectivity. Uniformity in tip exposure is desired in order to predict the characteristics of an electrode array so that one can reliably interpret recorded signals during physiological experiments.

In conventional UEA manufacturing, tips are deinsulated using aluminum foil as a mask, by poking the electrodes through the foil to the desired exposure (Campbell et al. 1991). The exposed part of the electrodes is plasma etched while the aluminum foil protects rest of the device. This method of tip de-insulation has a few limitations. Repeatably and uniformly achieving tip exposure of 20 to 100 μm are very difficult. Also poking is a time consuming process: 15–20 min to poke one array. Poking is also operator dependent and hence is not a practical method for production. Handling arrays that have

been wrapped in the aluminum foil is also a challenge as the tip exposure can change during handling, and the arrays can even be damaged.

A novel wafer-scale method for deinsulating the tips of the UEA using a combination of photoresist masking and oxygen plasma etching was developed; Figure 10 illustrates the process flow. The tip exposure is controlled by varying the spin speed during photoresist coating of the electrode array. A detailed description of the process is given elsewhere (Bhandari et al. 2009a). Parylene was etched in two different plasma etching systems: an Oxford Plasmalab 80plus (Oxford Instruments Plasma Technology, Bristol, UK) and a March Plasmod (March Plasma Systems, Inc. CA, USA), which utilize capacitively and inductively coupled plasmas, respectively. The oxygen plasma etching parameters used for both tools are listed in Table 1. As the photoresist on tips of the electrodes was etched, the Parylene-C exposed to the oxygen plasma also gets etched, thereby, exposing the metal-coated electrode tips. Because Ir is an inert material and is not known to etch significantly in oxygen plasma, Ir served as an etch stop.

Tip deinsulation of the UEA requires a isotropic etch process, so that Parylene is uniformly removed from side-walls of the exposed tip of the electrode. Two etching systems are used to etch Parylene because even though March plasma provides favorable isotropic etching characteristics however because of high power setting the photoresist (used as mask) tends to flake as the etching progresses (typical etching time to completely remove Parylene is 20 min). In the case of the Oxford Plasmalab 80 plus, Parylene is etched only from the top of the electrode tips and even increasing the etching time does not fully remove the encapsulation from the side wall. This study is described in detail in another publication (Hsu et al. 2008). Thus, to deinsulate the tips of the electrode array the wafer is first etched in Oxford Plasmalab 80 plus and then in March Plasmod respectively. Figure 11 presents an SEM image of an electrode array deinsulated using the wafer-scale process and a spin speed of 100 rpm. The customized photoresist based masking process parameters were tested to ensure that the electrical and mechanical properties of Parylene were not compromised by the process. Tape test (ASTM D3359B) and the electrochemical impedance spectroscopy (EIS) results show that the photoresist process does not cause any change in the adhesion and dielectric properties or stability of Parylene-C (Bhandari et al. 2009a). Furthermore, to validate the photoresist removal (acetone and isopropyl alcohol) process, two arrays were subjected to the method described above, and were sent to Nelson Lab, Salt Lake City, for the mammalian cell culture media (MEM) elution test (procedure # STP0032REV 03). Each array was evaluated in 1 mL of mouse heteroploid connective tissue (L-929) extract and incubated for 72± 3 h at 37±1°C. The cytotoxicity scores range from 0–4, 0 being no cytotoxicity and 4 being severe cytotoxicity. Any score of 2 or less is considered “passing”. The MEM elution cytotoxicity test performed on the arrays at Nelson Laboratories showed a score of 0. The cytotoxicity results indicate that the photoresist cleaning procedure was effective in removing the photoresist. However, it may be possible that some residual photoresist might have been left on the electrode array but it did not significantly showed any cytotoxic effect because it was baked.

3 Discussion

Wafer-scale fabrication has several favorable attributes, including batch fabrication, high reproducibility of geometrical and electrical characteristics, and precise and easy customization of the recording / stimulating sites. It not only increases throughput but also reduces

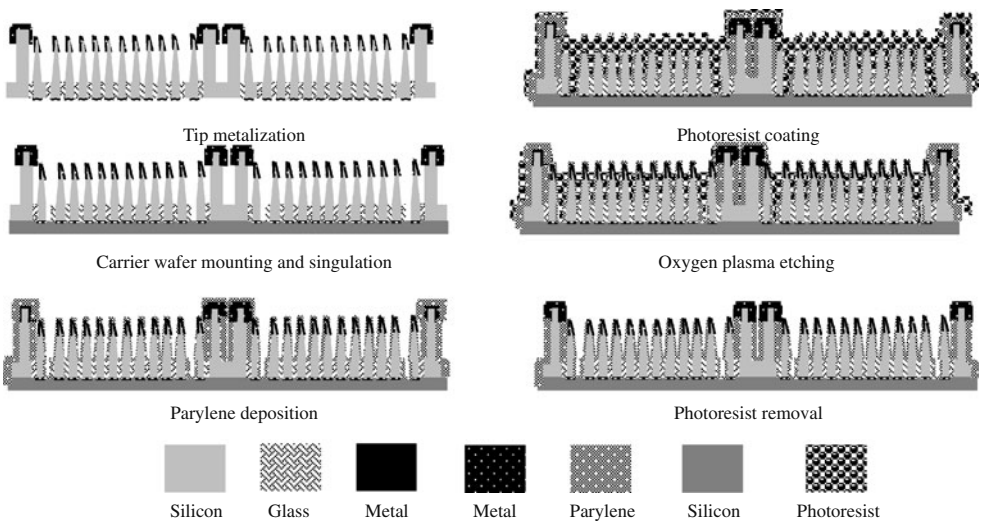


Fig. 10 Process for wafer-scale tip de-insulation of the UEA using photoresist as a mask

Table 1 Plasma etching conditions

	Oxford Plasmalab 80plus	March Plasmod
Etching characteristics	Anisotropic	Isotropic
Power	50 W	150
Pressure	100 mTorr	400 mTorr
Oxygen flow	50 sccm	No control
Etching time	75 min	5 min

lead time for array fabrication. It would take 8.5 working days to fabricate 45 arrays / wafer compared to 27 days by the conventional array-scale method. Table 2 compares the nonuniformity in geometrical and electrical characteristics of the arrays fabricated from the wafer-scale (three wafers) and conventional arrays-scale method (five arrays from different batches). The nonuniformity percentage was calculated as standard deviation multiplied by 100 and divided by the mean. Electrode impedances were measured by poking the electrodes into a conductive Agar (1% agarose gel), and impedances of individual electrodes were measured by contacting the bondpad on the back of each electrode. The agar was prepared from phosphate-buffered saline and agar powder in a weight ratio of 1:42. A Pt counter electrode probe was inserted in the agar. Impedances of individual electrodes were measured with a Cyberkinetics impedance tester (serial # 4290) sequentially using a probe signal of 100 nA (peak-to-peak) at 1 kHz frequency and 100 nA constant current. The nonuniformity percentage after dynamic etching across the wafer by wafer-scale etching is six times less than the single-array etching, while the nonuniformity in electrode length, after static etching, is six times less while width is 10 times.

Furthermore, the photoresist based wafer-scale deinsulation method allows uniformly exposed tip lengths, over a range of 30 to 350 μm in length (Bhandari et al. 2009a). The wafer-scale process leads to better uniformity in tip exposure. The nonuniformity in tip exposure achieved by the photoresist based wafer-scale deinsulation is around four times less than the mechanical aluminum-foil poking method, leading to reduction in non uniformity in impedance by half. Figure 12(a) and (b) shows SEM images of the UEA fabricated by the conventional array-scale method and wafer-scale method. The wafer-scale etching fabricates electrode columns with rounded corners, with a smooth and slightly positive tapered tip (column that narrows at the top), Fig. 12(a). Whereas, the conventional array-scale process fabricates electrode columns with sharp edges and **(a)** pyramidal shape, Fig. 12 (b). The importance of such features has not been quantified but may have significance in pushing the tissue out of the way instead of cutting during insertion (Edell et al. 1992; Beard et al. 1992).

Furthermore, the SIROF process along with photoresist based masking method allows wafer-scale tip metallization of UEA. The SIROF process requires no further conditioning and furthermore it reduces the cost of manufacturing and lead time. It must be noted that it takes approximately 2 h to activate one UEA with AIROF. There are 49 arrays in a 3-inch wafer, and hence it will take at least 98 h of parallel activation of

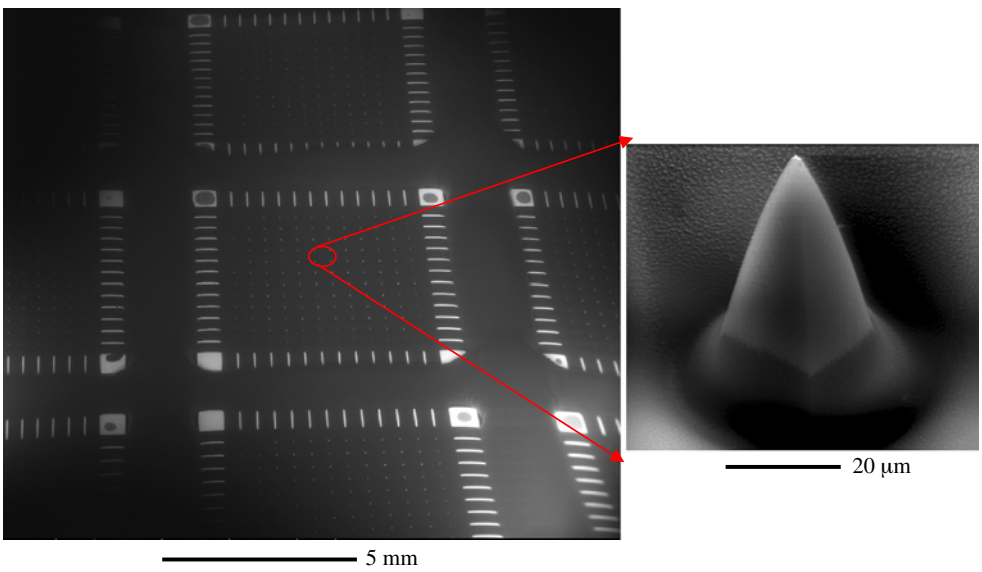


Fig. 11 SEM micrograph of electrode arrays immersed in photoresist after oxygen plasma etching. Also shown is the extra row of sacrificial electrodes in four corners, fins and corner post

Table 2 Comparison of nonuniformity in geometry and impedance of electrode arrays fabricated by the wafer-scale and the conventional array-scale method

Nonuniformity (%)	Wafer-scale process	Array-scale process
Dynamic etching :column top	1.5%±0.5	9.68±1.23
Static etching: (a) length	1.1 %±0.1	6.38%±4.6
(b) Shank width	1.36%±1.1	14%±5.15
Tip Exposure	4.08%±0.6	16.85%±3.42
Impedance	20.76%±2.32	43.21%±12.11

arrays from one wafer. SIROF process would completely eliminate the activation process. It must be appreciated that using SIROF as an electrode material will not only increase the throughput, but most importantly, reduce any variation from the activation process, which will increase the reliability of the arrays. Additionally, SIROF will be of particular importance for the wireless recording/stimulating arrays, which by definition will not have wires that would allow activation via cyclic voltammeter.

4 Conclusion

This paper describes a wafer-scale method of fabricating high aspect ratio (15:1) penetrating microelectrode arrays with a reliable and reproducible process. The technique enables a low cost process and reduces lead time. Novel fabrication process such as, grinding, wet-etching, tip metallization, tip deinsulation have been incorporated in the UEA fabrication. These processes are not only performed on wafer-scale but also overcome the limitations of the existing technology and improve the quality and controllability in geometrical and electrical characteristics of the UEA. The wafer-scale technique and the individual process steps are platform technology and can be implemented to other configurations of the UEA such as the slant (Branner et al. 2001; Bhandari et al. 2009b) and the convoluted electrode arrays (Bhandari et al. 2008). The major advantage of this method compared to other techniques employed for fabricating high aspect ratio implantable devices is the simplicity of the method. The degree of control achieved in the dimensions and impedance of the electrode array would help in better understanding of observed variations in physiological results.

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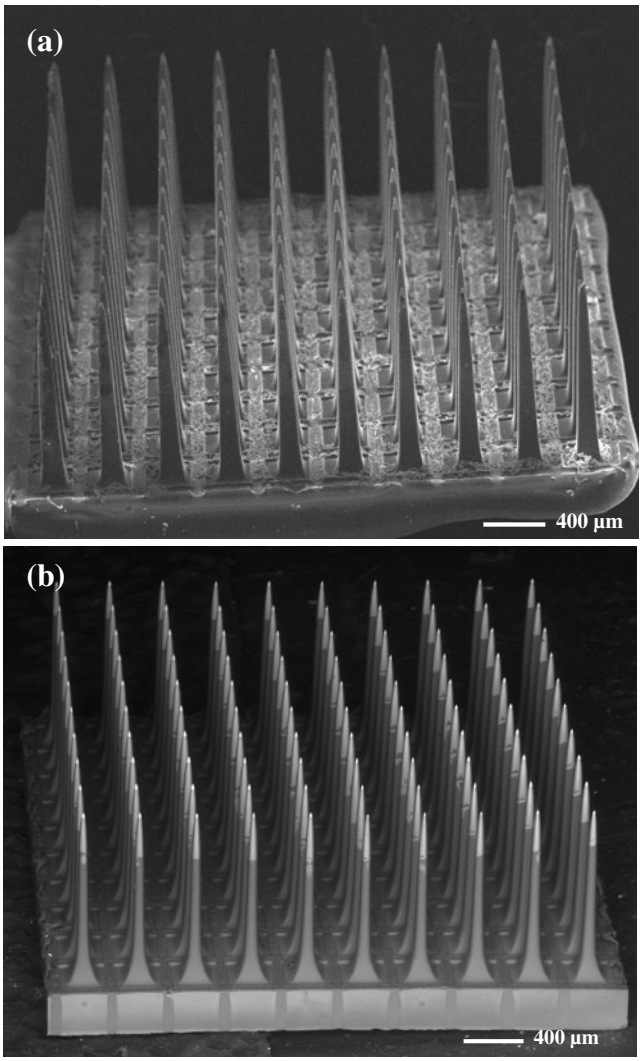

Fig. 12 SEM images of the UEA fabricated by: (**a**) array-scale method and (**b**) wafer-scale method. Notice the electrodes fabricated by the conventional method have sharp edges and have non-uniform tip exposure compared to the electrode arrays fabricated by the wafer-scale method, which have uniform geometry, rounded corners, and have small and uniform tip exposure

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