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An ultra-low power fully CMOS sub-bandgap reference in weak inversion

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Abstract
This paper presents a sub-1-V CMOS bandgap reference circuit with ultra-low power consumption, utilizing only 9 MOS transistors. The proposed circuit achieves nano-watt power consumption by biasing all transistors in the sub-threshold region. A three-branched configuration is utilized to create the bandgap voltage reference in the circuit. The proposed architecture generates CTAT and PTAT voltages without using any op-amp and BJT. In this circuit, the cascode structure are used to improve the line sensitivity (LS). In the proposed bandgap circuit, self-biased configuration is used without using an external bias circuitry. The first branch generates PTAT current and the second and third branches generate PTAT and CTAT voltages. The bandgap circuit is designed and simulated using Cadence in TSMC 0.18 µm CMOS technology. The results of post-layout simulation indicate that the bandgap voltage reference circuit generates a voltage reference of 644 mV, with a temperature coefficient (TC) of 78.5 ppm/°C within the temperature range of − 25 to 85 °C. The proposed circuit operates with a power supply of 0.9 V and consumes only 8.2 nW. Furthermore, the circuit exhibits a line sensitivity of 0.31%/V for power supply voltages ranging from 0.9 to 1.8 V. The Power Supply Ripple Rejection (PSRR) of the proposed circuit is about − 40 dB within the frequency range of 1–100 Hz.

Keywords Bandgap reference · Nano watt · Sub-1-V · Subthreshold · Ultra-low power

1 Introduction

In today's modern period, due to competition in market and industry, all devices and machines should be developed in terms of accuracy, power consumption, minimum required voltage, dimensions, and manufacturing costs, etc. In other words, various components of a device must be optimized to compete in industry and market. One crucial element that significantly affects the overall performance of devices is a bandgap references (BGR). Voltage references are frequently used in analog and electronic circuits. These circuits is usually used in bias circuitries, low-dropout regulators, DRAMs, flash memories, and data converters. The performance and accuracy of decoders and encoders, as well as the accuracy of conversion of a signal processing block in data converter systems, depends on the accuracy of the voltage references. Important parameters in design of voltage references are temperature coefficient (TC), line sensitivity (LS), power supply ripple rejection (PSRR), and power consumption [1–3].

Voltage references should be designed such that they stay unchanged towards the changes of process, supply voltage and temperature. In order to design a bandgap circuit that is independent of temperature, a complementary-to-absolute temperature (CTAT) voltage and a proportional to absolute temperature (PTAT) voltage should be generated and mixed to compensate the temperature changes [1]. A CTAT voltage can be generated through the base-emitter voltage of a diode-connected BJT or gate–source voltage of a MOS transistor. A PTAT voltage can be generated through the difference of the gate-source voltages of two transistors or difference of base-emitter voltages of two BJTs with different collector currents. For generating a voltage reference, the sum of PTAT and CTAT voltages with appropriate coefficients is mandatory [1–5].

There is a demand for small bandgap voltage reference that are insensitive to process, voltage, and temperature (PVT) variations while minimizing power dissipation. The

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reduction of power consumption and circuit dimensions not only necessitates the adoption of new technologies but also affects certain parameters, such as the maximum voltage headroom. As dimensions decrease, the threshold voltage also decreases. The amount of voltage reference should be decreased proportionally with the technology, to prevent a decrease in circuit lifespan, minimize power consumption, and lower chip temperature. Hence, sub-1-V and low-power supply voltage reference is an inevitable part of modern systems [5].

It is worth noting that while silicon references are commonly used in industries to reduce final costs by using standard CMOS technologies, Hedayati and et al. with the help of materials like silicon carbide (SiC), introduce a voltage reference that operates for a wide temperature range of 25–500 °C. However, this circuit suffers from high power consumption and such structure is not applicable in standard CMOS technologies [6]. In Ref. [7], a fractional bandgap is presented. Using emitter–base voltage of a BJT as a CTAT voltage and applying a current with positive TC to a resistor in a feedback loop, a near zero TC voltage is generated. Due to the use of op-amp and BJTs, the power consumption of the fractional bandgap is in micro watt range [7]. Banba and et al. [8] proposed a sub-1-V bandgap voltage reference by converting sum of two PTAT and CTAT currents to a voltage in a feedback loop. Due to use of op-amp and diodes, it also suffers from high power consumption and supply voltage. In [9] a switched-capacitor bandgap circuit is introduced in which no resistor is used. Using capacitors instead of resistors in [9] results in a high precision voltage reference. While an offset cancellation technique is used [9], but the power consumption of the op-amp is still a challenging issue.

Wang and et al. [10] used a MOS transistor in the weak inversion to reduce the power consumption and voltage headroom of the circuit. Also, the offset of op-amp has been suppressed in [10]. In [11] a cross-coupled structure for BGR is presented. But this circuit is suitable for the voltage references higher than one volt, which is not compatible with the recent technology nodes [11]. The line sensitivity has been significantly improved by using a self-adjusting circuit in [12]. All the transistors used in [12] operate in the sub-threshold region, which has reduced the power consumption of the circuit. However, this circuit has a high TC [12]. A self-biased nano-watt voltage and current reference has been presented in [13] by using a single resistor with zero temperature coefficient (TC). The main challenge in [13] is realizing such a zero TC resistor. A trimless voltage reference has been offered in [14] with using stack of LVT MOS transistor. This approach leads to improvement of occupied area and power consumption as well. Some other BGRs are also presented in literature [15, 16] that suffer from high power consumption.

In [17] a bandgap circuit is presented in which a modified beta multiplier bias circuit is used to reduce the mismatch caused by the contribution of the PMOS transistors op-amp and threshold mismatch between two NMOS transistors. A sub-1V voltage-mode reference circuit that sums the PTAT voltage with a scaled version of the CTAT voltage has been presented in [18]. The advantages of the proposed circuit compared to current-mode bandgap circuits are the elimination of a current mirror stage and minimizing the current mirror ratio of PTAT, which leads to error reduction. In order to achieve a low TC voltage reference, a curvature compensation technique is applied to a voltage-mode sub-bandgap reference circuit in [19] that results in flicker noise reduction and ease of op-amp requirements. Nagulapalli and et al. [20] introduce a bandgap reference circuit in which noise multiplication of the operational amplifier is limited by moving the resistor used in the emitter of BJT into its base. This resistance is combined with a CTAT resistance in the current mode bandgap reference.

In this work a simple three-branched design is proposed without the use of any op-amp and BJT. Only two resistors and MOS transistors have been used in the weak inversion region to significantly reduce the power consumption. The remains of the paper are organized as follows: Sect. 2 presents a study of the proposed BGR circuit. The proposed BGR is analytically examined in Sect. 3. The important parameters (like LS, PSRR, and TC) of a bandgap circuit are defined in Sect. 4. Section 5 presents the post-layout simulation results and the paper is concluded in Sect. 6.

2 Proposed BGR structure

The schematic of the proposed BGR structure is shown in Fig. 1. The behavior of the gate-source voltage of MOS transistors in weak inversion is similar to that of the emitter–base voltage of a BJT [5, 13, 21]. Therefore, the gate-source voltage of MOS transistors in sub-threshold is utilized as a CTAT voltage and the difference of gate-source voltages of two MOS transistors is used for generating a PTAT voltage. The proposed circuit has a self-biased structure that eliminates the need for any external bias circuitry. By employing the MOS devices in sub-threshold, the circuit can operate with low supply voltages (i.e. less than 1V) that results in a very low power consumption.

As shown in Fig. 1, the proposed circuit includes a start-up circuitry and a bandgap core. The start-up circuit consists of transistors M_{S1}, M_{S2}, and M_{S3} in which M_{S1} acts as a MOS capacitor. When the circuit is powered-up, gate of M_{S2} is charged via M_{S1} until it turns on, and when M_{S2} turns on, the gate voltage of M_4, M_5 and M_6 is pulled down and leads to the separation of the circuit from the zero point; as a result, the circuit returns to its desired operation. When

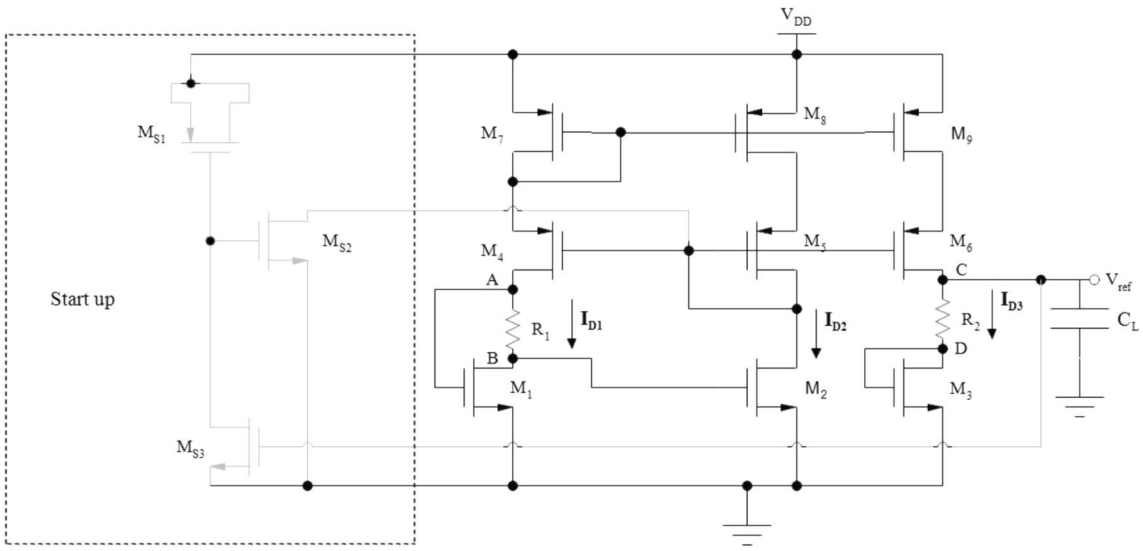


Fig. 1 Schematic of the proposed BGR with start-up circuit

the output voltage reaches its steady state value, M_{S3} turns on, and in this case, the gate voltage of M_{S2} transistor is pulled down and turns off. At this point, the start-up circuit completes its work and is disconnected from the bandgap core. Actually, due to self-biasing of the proposed BGR, the start-up circuit only helps the circuit to start quickly [22].

According to the Fig. 1, the bandgap core has three branches. In the first branch consists of M_1, to generate the required PTAT current ($I_{D1} = I_{PTAT}$), the gate-source voltage of transistor M_1 is connected to one side of R_1 (i.e. node A) and the gate-source voltage of transistor M_2 is connected to the other side of R_1 (i.e. node B). In this way a PTAT current given by $(V_{AB})\ /R_1 = (V_{GS1} - V_{GS2})/R_1$ is achieved. It is worth mentioning that transistors M_{7-9} are used in a cascode scheme with M_{4-6} to improve the PSRR and LS, and also reduce the impact of power supply noise on the reference voltage. The generated PTAT current I_{D1} is mirrored into the second branch by ratio of $\frac{(\frac{W}{L})_8}{(\frac{W}{L})_7}$. Similarly, with ratio of $\frac{(\frac{W}{L})_9}{(\frac{W}{L})_8}$, the current I_{D2} is mirrored into the third branch. I_{D3} passes through resistor R_2 and generates the required PTAT voltage. Supposing identical aspect ratio for M_7, M_8 and M_9, the generated PTAT voltage is equal to $V_{PTAT} = V_{CD} = R_2 \cdot I_{D3} = R_2.(\frac{V_{GS1-VGS2}}{R1})$. The mentioned current passes through a diode-connected transistor (i.e. M_3) and generates a CTAT voltage (V_{GS3}). Therefore, output voltage V_{ref} is obtained by applying a KVL from the output node of the circuit (C node) to ground as $V_{REF} = V_{CD} + V_{GS3}$, where $V_{CD} = R_2 . \frac{V_{GS1-VGS2}}{R1}$ is a PTAT voltage and V_{GS3} is a CTAT voltage.

Note that, here, all the currents of the three branches are assumed identical ($I_{D1} = I_{D2} = I_{D3}$). Finally, generated CTAT voltage (i.e. V_{GS3}) and PTAT voltage (i.e. voltage across R_2) are added to each other and the desired reference voltage is generated. The proposed design, operates with a nano-ampere current and ultra-low power consumption. Detailed analyses of the proposed circuit are presented below.

3 Mathematical analysis

The drain current of a MOS transistor in the weak inversion region is given by (1) [21]:

$$I_D = I_0\left(\frac{W}{L}\right)\exp\left(\frac{V_{GS}-V_{TH}}{nV_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{1}$$

where V_{TH}, V_{GS}, V_{DS} and V_T are the threshold, gate-source, drain-source, and thermal voltages, respectively and $\frac{W}{L}$ is MOS transistor aspect ratio. I_0 is drain's current when $V_{GS} = V_{TH}$ and is given by (2):

$$I_0 = \mu C_{ox}(n-1){V_T}^2 \tag{2}$$

in which n is the sub-threshold gradient coefficient. In subthreshold, when $V_{DS} > 4V_T$ the transistor is in the saturation region, and its current is independent of V_{DS}. To avoid the effect of changes in V_{DS} on the circuit, parameters of the transistor should be chosen to operate in saturation region. The approximate value of transistor's current in saturation is as follows:

$$\begin{aligned} I_D &= \mu C_{ox}(n-1)V_T^2\left(\frac{W}{L}\right).\exp\left(\frac{V_{GS}-V_{TH}}{nV_T}\right).\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right] \\ &\approx \mu C_{ox}(n-1)V_T^2\left(\frac{W}{L}\right)\exp\left(\frac{V_{GS}-V_{TH}}{nV_T}\right) \end{aligned} \tag{3}$$

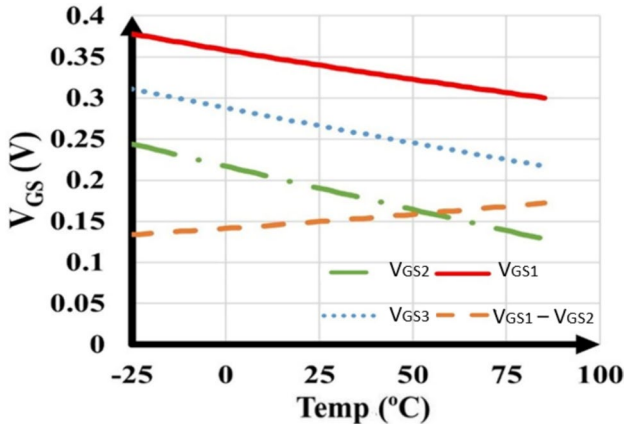


Fig. 2 V_{GS} of M_1, M_2 and M_3 transistors versus temperature

So the V_{GS} of transistors in subthreshold is given by (4):

$$V_{GS} = nV_T ln\left(\frac{I_D}{\mu C_{ox}(n-1)V_T{}^2\left(\frac{W}{L}\right)}\right) + V_{TH} \tag{4}$$

V_{GS} can be assumed as a CTAT voltage that can be represented for a MOS transistor as (5):

$$V_{GS}(T) = \beta_0 + \beta_1 T + \beta_2 T ln(T) \approx \beta_0 + \beta_1 T \tag{5}$$

The constant coefficients β_0, β_1, and β_2 depend on the technology and β_2 is high-order nonlinear effects which is considered negligible. The temperature dependancy of V_{GS1}, V_{GS2}, and V_{GS3} are shown in Fig. 2. In Fig. 2, the voltages V_{GS1}, V_{GS2}, and V_{GS3} show CTAT behaviour. $V_{GS1} - V_{GS2}$ is also is depicted in Fig. 2 and it represents a PTAT behaviour.

Using Kirchhoff law in Fig. 1, the current I_{D1} can be determined as (6),

$$I_{D1} = \frac{V_{AB}}{\mathrm{R1}} = \frac{V_{GS1} - V_{GS2}}{\mathrm{R1}} \tag{6}$$

and current I_{D2} is given by (7):

$$I_{D2} = K_1 I_{D1} \tag{7}$$

in which,

$$K_1 = \frac{(\frac{W}{L})_8}{(\frac{W}{L})_7} \tag{8}$$

The transistors M_4 to M_9 form a current mirror, so the current I_{D3} can be expressed as follows:

$$I_{D3} = K_2 I_{D2} \tag{9}$$

$$K_2 = \frac{(\frac{W}{L})_9}{(\frac{W}{L})_8} \tag{10}$$

Therefore the generated reference voltage is as (11):

$$V_{ref} = V_{GS3} + (\frac{\mathrm{R}_2}{\mathrm{R}_1}\frac{(\frac{W}{L})_8}{(\frac{W}{L})_7}\frac{(\frac{W}{L})_9}{(\frac{W}{L})_8})(V_{GS1} - V_{GS2}) \tag{11}$$

Obviuosly Eq. (11) is comprised of a PTAT term (i.e. $V_{GS1} - V_{GS2}$) and a CTAT term (i.e. V_{GS3}), and choosing propoer value for $\frac{\mathrm{R}_2}{\mathrm{R}_1}\frac{(\frac{W}{L})_8}{(\frac{W}{L})_7}\frac{(\frac{W}{L})_9}{(\frac{W}{L})_8}$ results in a zero TC V_{ref}. The required value for $\frac{\mathrm{R}_2}{\mathrm{R}_1}$ can be obtained by derivation of (11) with respect to temperature and setting it equal to 0 as follows:

$$\begin{aligned}\frac{\partial Vref}{\partial T} =& \frac{\partial(\beta_{0,3} + \beta_{1,3}T)}{\partial T} \\ &+ \frac{\mathrm{R}_2}{\mathrm{R}_1}\frac{(\frac{W}{L})_8}{(\frac{W}{L})_7}\frac{(\frac{W}{L})_9}{(\frac{W}{L})_8}\left[\frac{\partial(\beta_{0,1} + \beta_{1,1}T)}{\partial T}\right. \\ &\left. - \frac{\partial(\beta_{0,2} + \beta_{1,2}T)}{\partial T}\right] = 0\end{aligned} \tag{12}$$

$$\frac{\mathrm{R}_2}{\mathrm{R}_1}\frac{(\frac{W}{L})_8}{(\frac{W}{L})_7}\frac{(\frac{W}{L})_9}{(\frac{W}{L})_8} = \frac{\beta_{1,3}}{\beta_{1,2} - \beta_{1,1}} \tag{13}$$

According to Fig. 2 the temperature coefficient (TC) of PTAT voltage is 0.345 mV/°C, while the TC of the CTAT voltage is − 0.845 mV/°C. Therefore, supposing $\frac{(\frac{W}{L})_8}{(\frac{W}{L})_7}\frac{(\frac{W}{L})_9}{(\frac{W}{L})_8} = 1$ and considering Eq. (13), requierd $\frac{\mathrm{R}_2}{\mathrm{R}_1}$ is given by (14):

$$\frac{\mathrm{R}_2}{\mathrm{R}_1} = \frac{0.845}{0.345} = 2.5 \tag{14}$$

4 Line Sensitivity, PSRR and Temperature coefficient

Line sensitivity (LS) explains the sensitivity of the voltage reference to the supply voltage. According to this description, lower LS results in lower dependency of V_{ref} to V_{DD}. LS is directly related to Power Supply Rejection Ratio (PSRR) as well, and minimizing LS results in mimimizing low frequency PSRR.

The LS for a voltage reference can be determined using (15):

Table 1 Circuit parameters

Transistor	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9
W(μm)	0.9	42	5	18	18	1	1	7	7
L(μm)	20	20	20	20	20	20	20	20	20
Resistor				R1					R2
Value				49.2M					125M

$$LS = \frac{\frac{\Delta Vref}{\Delta Vdd}}{Vref} \times 100\% \tag{15}$$

where, ΔV_{ref} represents voltage reference variations, while ΔV_{dd} denotes supply voltage variations. It is worth noting that employing a cascode structure reduces LS, though it may also increases the minimum required supply voltage.

PSRR describes the effect of power supply noise (small-signal variation) on voltage reference. It is also defined as (16):

$$\text{PSRR} = 20\log\left(\left|\frac{v_{ref}}{v_{dd}}\right|\right) \tag{16}$$

By using the small-signal equivalent circuit and simplifying it, the value of $\frac{v_{ref}}{v_{dd}}$ for Fig. 1 can be obtained as (17):

$$\left(\frac{v_{ref}}{v_{dd}}\right) \approx \frac{(R_2 + \frac{1}{g_{m3}}||r_{o3})}{(R_2 + \frac{1}{g_{m3}}||r_{o3}) + g_{m6}r_{o6}r_{o9}}) \tag{17}$$

The temperature coefficient of a bandgap reference is defined as (18). Apparently low TC is desirable to acheive a tempereture independent reference voltage.

$$TC = \frac{V_{ref(maximum)} - V_{ref(minimum)}}{(T_{maximum} - T_{minmum}) \times V_{ref(atT=27°C)}} \tag{18}$$

5 Post layout simulation results

To verify the performance of the suggested bandgap reference (BGR) circuit in Fig. 1, a prototype of the circuit is designed using TSMC 0.18-µm CMOS technology, and the circuit parameters are shown in Table 1. The circuit was designed with an active area of 480µm×840µm. All required resistors are implemented by using high-resistance polysilicon (HpolyR). Since all resistors have identical temperature coefficient so the ratio of $\frac{R_2}{R_1}$ in (11) remains independent of temperature and does not affect the temperature coefficient of V_{ref}. To mitigate the effect of channel length modulation, the cascode transistors should be sufficiently large to reduce the line sensitivity (LS) of the produced voltage reference.

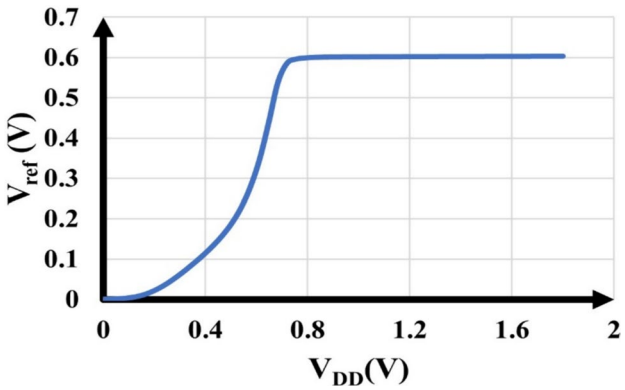


Fig. 3 Supply dependency of the proposed BGR

The current of the circuit in Fig. 1 is set by the value of R_1. Therefore, R_1 should be adjusted to maintain the current of the first branch in nano ampere range (here, 3.033nA) for achieving ultra-low power consumption.

Figure 3 shows the post layout simulation results of supply dependency of the proposed circuit at TT corner. As seen, over a wide range of power supply variations from 0.8 to 1.8V, LS is as low as 0.31%/V that indicates ultra-low dependency of the generated reference voltage to power supply variation. The circuit consistently produces a constant voltage of 644 mV, while drawing a total current of only 9.1 nA from the 0.9 V power supply, resulting in an ultra-low power consumption of 8.2 nW.

The simulated reference voltage vs. temperature is depicted in Fig. 4. According to Fig. 4, the circuit's temperature coefficient (TC) is 78.5 ppm/°C over the temperature range of − 25 to 85 °C, that confirms the voltage reference has a good robustness against temperature variations. Figure 5 illustrates the simulated V_{ref} versus V_{DD} variation in different process corners. It shows the BGR sensitivity to the power supply variation in all process corners. Line sensitivity (LS) of the circuit is 0.48%/V, 0.30%/V, 0.34%/V and 0.33%/V respectively in the SS, FF, SF and FS corners.

The simulated V_{ref} versus temperature in different process corners is depicted in Fig. 6. The TC is measured to be 78.5 ppm/°C for TT corner while the TC is 92.4 ppm/°C for

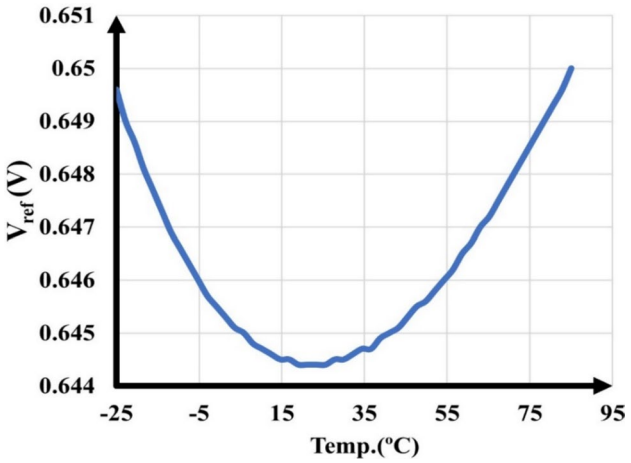


Fig. 4 Thermal behavior of the proposed BGR

FF. The TC is 136 ppm/°C for the FS corner and it is 98.2 ppm/°C at SF corner. For SS corner the TC is 79.8 ppm/°C. Hence, the simulation results in Fig. 6 indicate that the proposed circuit has a low dependency on the process corner.

Figure 7 demonstrates the PSR of the proposed circuit. According to Fig. 7 the effect of power supply noise on the voltage reference has 40 dB attention in the frequency range of 1–100 Hz.

To estimate the effect of process and fabrication errors on the circuit, Monte Carlo simulation results for 1000 trials are shown in Fig. 8. In Fig. 8a the average generated reference voltage is 644.23 mV with a standard deviation of 16.24 mV. As seen in Fig. 8b, the circuit has an average TC of 81.59 ppm/°C and the average LS in Fig. 8c is 0.322%/V. Totally, Monte Carlo simulation results show a good robustness of the BGR to the process and fabrication errors.

While the Monte Carlo simulation results in Fig. 8 show the robustness of the circuit against process variation, the exact value of generated V_{ref} may vary from one process corner to another corner in Fig. 6. It is worth mentioning

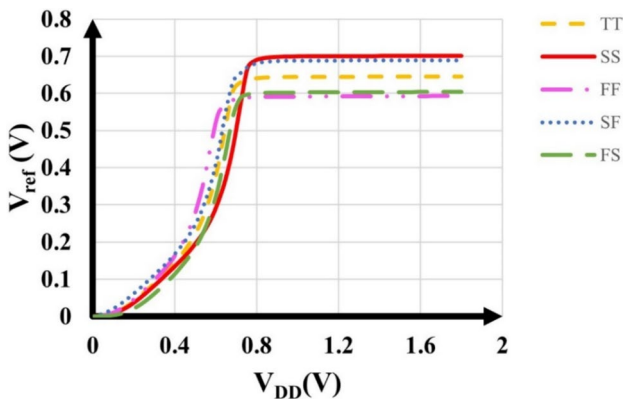


Fig. 5 Line sensitivity at different process corners

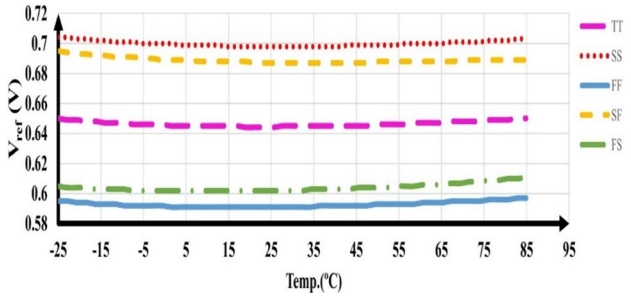


Fig. 6 Thermal behavior of BGR at all process corners

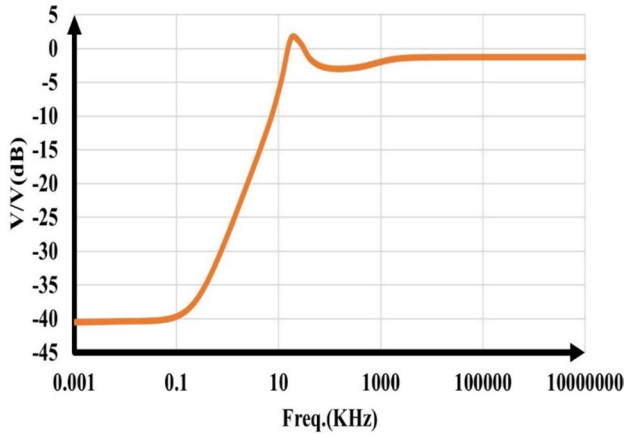
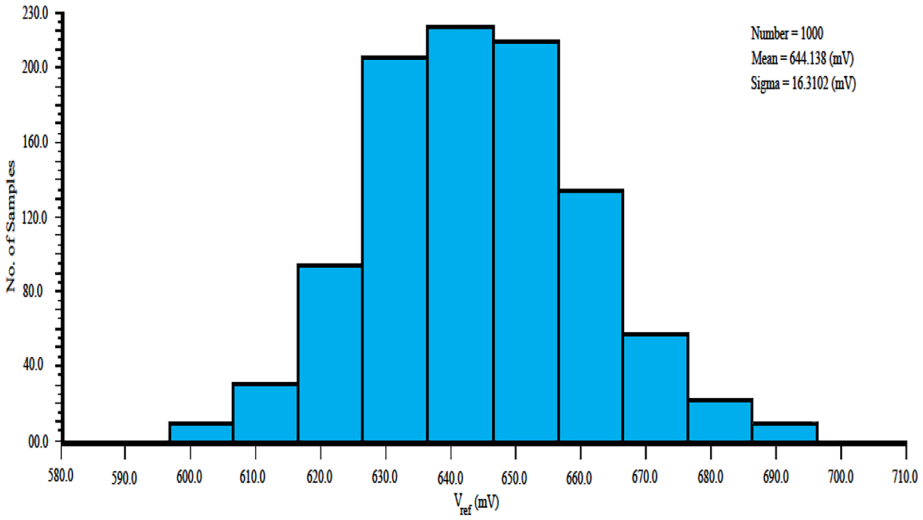
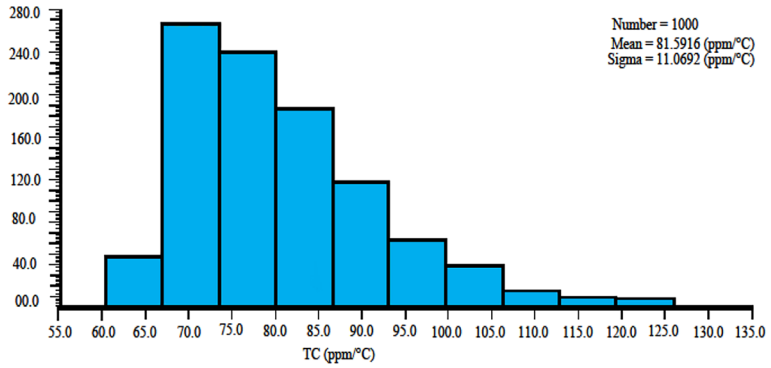


Fig. 7 PSRR of the proposed BGR

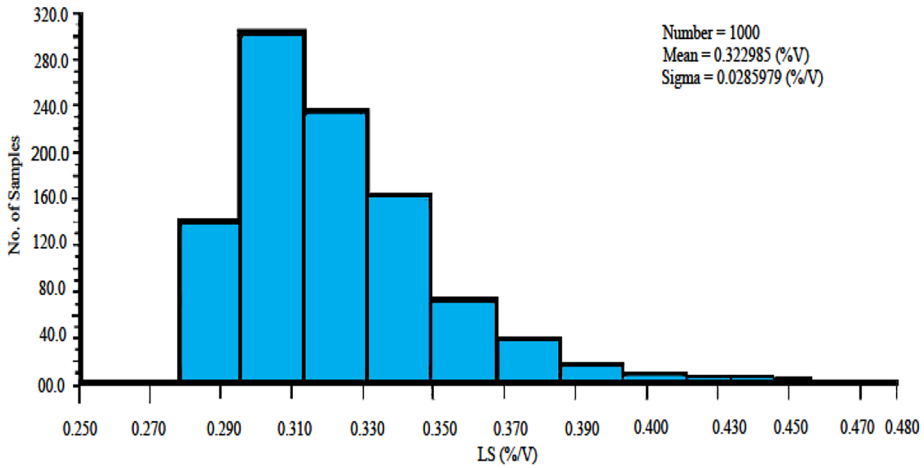
that in low power BGRs the impact of process deviation is often greater due to the exponential characteristics of subthreshold currents. However, if more accurate V_{ref} at all process corners are required, using trimming techniques (like [23]) is mandatory. Actually trimming circuits [23] usually adjust V_{ref} by sinking/sourcing additional current from/to the bandgap core. It is important to mention that, taking into account both the area requirements and the relatively minor deviation of this circuit compared to similar types of BGRs, this work opts not to employ any trimming circuitry.

The power spectral density (PSD) of the proposed BGR is shown in Fig. 9 for different load capacitances (C_L). Although, due to the extremely low power consumption of the proposed circuit in the subthreshold region, it tends to exhibit poor noise performance, but the noise level of the circuit is still promising. According to the simulation results, noise of the circuit is 4 $\mu V/\sqrt{Hz}$ at the frequency of 100 Hz for $C_L = 0.5$ pF. As expected, higher value of C_L results in lower noise power at the output. For example, the output noise of the circuit at frequency of 1 MHz, is 8.46, 4.26, 2.13 $nV/\sqrt{Hz}$, respectively, for C_L of 0.5, 1 and 2 pF. Apparently, the main source of low frequency noise





(b)



(c)

Fig. 8 Monte-Carlo simulation results of **a** generated reference voltage, **b** TC and **c** LS

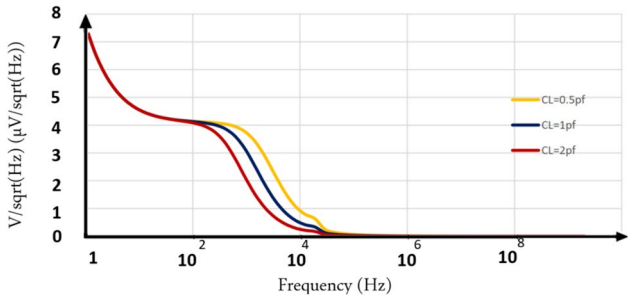


Fig. 9 Noise spectrum of proposed BGR

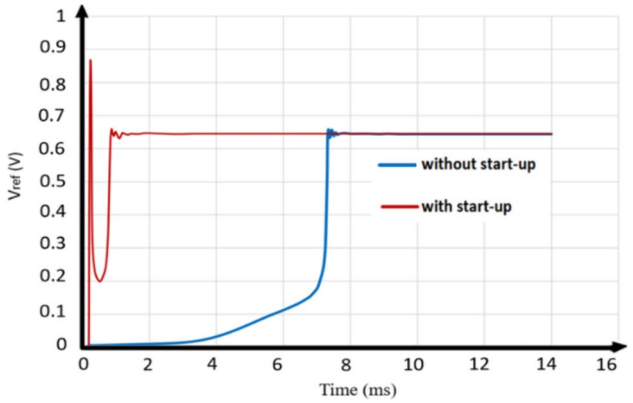


Fig. 10 Start-up time of the circuit with/without start-up circuit

(here < 100Hz) in BGRs is caused by flicker noise of MOS transistors, while the thermal noise is dominant at high frequencies (here > 100Hz).

Although the proposed BGR has a self-biased configuration and needs no start-up circuit, a conventional start-up circuit is used in Fig. 1 to accelerate the circuit's transition to a normal operating state after power-up. Transient response of the reference voltage after power-up with and without start-up circuit is shown in Fig. 10. As seen, the start-up circuit reduces the start-up time from 10 ms to less than 2 ms and results in a faster start-up.

The layout of the circuit has been optimized to utilize the minimum chip area. As shown in Fig. 11 the chip area of the BGR is as small as 480 μm × 840 μm.

For comparison, the performance summary of the proposed BGR and some similar prior works are shown in Table 2. The performance of the circuit is amongst the best prior works.

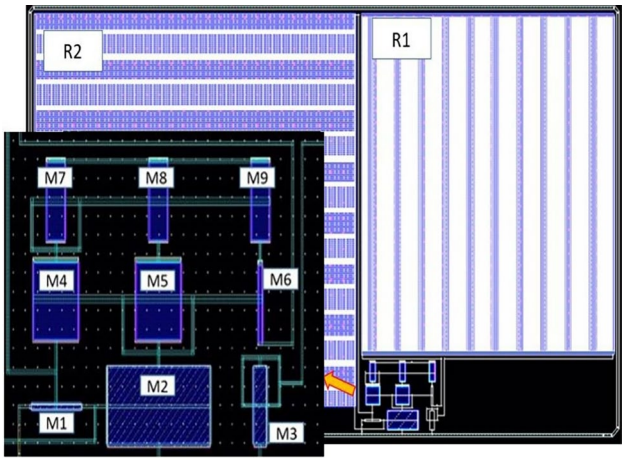


Fig. 11 Layout of the proposed circuit

6 Conclusion

A low-power BGR has been developed that consits of three branches with nine MOS transistors and two resistors. All transistors have been biased in weak inversion region. The circuit generates a PTAT current by using the gate-source voltage difference of two MOS transistors. This current is then mirrored into the second and third branches and passed through a resistor to generate a PTAT voltage. This PTAT voltage is combined with the V_{GS} of a diode-connected transistor (as a CTAT voltage) to generate the voltage reference. The circuit has been simulated and post-layout results confirm its performance. The post-layout simulation results demonstrate that the circuit produces a voltage reference of 644 mV with a TC of 78.5 ppm/°C within the temperature range of − 25 to 85 °C. The circuit operates with a power supply of 0.9 V and consumes only 8.2 nW. The line sensitivity of the circuit was measured 0.31%/V, indicating a minimal change in the voltage reference for power supply voltages ranging from 0.9 to 1.8 V. The PSRR of the proposed circuit is − 40dB within the frequency range of 1–100 Hz, Furthermore, the chip area of this circuit has been significantly reduced compared to similar designs. The simulation results demonstrate that the proposed circuit exhibits a good robustness against process, supply voltage and temperature (PVT) variations, making it a promising solution for ultra-low power applications.

Table 2 Performance summary of the circuit and some simillar prior works

References	This work	[24]	[12]	[13]	[18]	[21]	[25]
Year	–	2010	2019	2020	2021	2022	2016
Technology	180 nm	180 nm	180 nm	180 nm	45 nm	180 nm	180 nm
V_{ref} (mV)	644	263.5	151	346	500	494	323
V_{DD} (V)	0.8 to 1.8	0.45 to 2	0.4 to 1.8	0.8 to 2	> 1.05	0.8 to 1.8	0.65 to 1.8
Power (nW)	8.2	2.6	1	12	7.56	3.48	4000
TC (ppm/°C)	78.5	142	89.83	21.98	24.4	58.4	15
LS (%/V)	0.31	0.44	0.163	0.31	0.15	0.7	6.19
TR (°C)	− 25 to 85	0–125	− 40 to 125	− 40 to 125	− 40 to 125	− 40 to 85	− 60 to 130
PSRR (dB)	− 40	− 45	− 73	− 60	− 60	− 49.06	–

Author contributions Conceptualization: [Emad Ebrahimi] Methodology: [Reza Mohammadi Nowruzabadi and Javad Mostofi Sharq] Formal analysis and investigation: [Reza Mohammadi Nowruzabadi and Javad Mostofi Sharq], Writing - original draft preparation: [Reza Mohammadi Nowruzabadi and Javad Mostofi Sharq] Writing - review and editing: [Emad Ebrahimi] Supervision: [Emad Ebrahimi]

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Declarations

Conflict of interest The authors have no competing interests to declare that are relevant to the content of this article.

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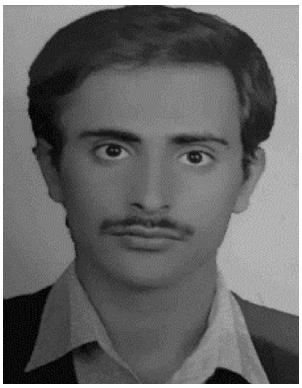

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