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A floating meminductor emulator using modified differential voltage current conveyor transconductance amplifier and its application

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Abstract
In this paper, a modified differential voltage current conveyor transconductance amplifier (MDVCCTA) based meminductor emulator has been proposed. The proposed meminductor is realized using one MDVCCTA, one resistor, and two grounded capacitors that leads to a very simple configuration. The emulator is working for a significant range of frequencies up to 80 MHz. The transient and non-volatility tests are found to be satisfactory. The corner and Monte Carlo analyses are done to verify the robustness of the proposed design. In addition, to assess the endurance of the recommended meminductor emulator, its workability with variations in supply voltage, temperature, and component values has been investigated. The pinched hysteresis loops that are fingerprints for the meminductor emulator are not deformed for any such variations. A comparison of suggested meminductor with those available in literature has been done based on several performance parameters. Two applications that demonstrate the viability of the suggested meminductor emulator have also been comprehended.

Keywords Modified differential voltage current conveyor transconductance amplifier · Meminductor emulator · Pinched hysteresis loop · Adaptive learning circuit · Chaotic oscillator · Mem-elements

1 Introduction

Mem-elements (memristor, meminductor, and memcapacitor) are now being used in a variety of applications including brain-inspired neuromorphic computing [1, 2], secure communications [3], artificial intelligence circuits [4], neural networks [5], non-volatile memories [6], in-memory computation [7], etc. Their wide range of applications is possible due to the unique features offered such as non-linear behaviour, and the inherent memory properties that open a window for in-memory computation. These two unique characteristics of mem-elements make them superior to the conventional circuit elements i.e., resistors, capacitors, and inductors. The properties offered by mem-elements cannot be replicated by combining the properties of the conventional circuit elements. Due to this fact, mem-elements are now treated as specific elements that are dominating many areas of science and engineering including electronics and communication, electrical, computer science, biological sciences, etc. All credit goes to Prof. Leon Chua who envisaged the memristor long back in 1971 in his seminal paper [8]. Later, Prof. Chua and Prof. S. M. Kang generalized the idea of memristive systems in 1976 [9]. In current scenarios, memristive systems are viewed as the future of electronics [10]. The constraints of CMOS technology have become a bottleneck to advancing the performance of systems in terms of speed, area, and power dissipation. These limitations are due to the adverse effects of CMOS technology which became dominating when the size of CMOS is reduced beyond the limit and no further improvement is possible. Memristor (memory-resistor) has paved the way as an alternative of CMOS technology due to its inherent ability of tininess and very low power consumption. Due to above-mentioned facts, the coming era of electronics and computer engineering belong to memristors and the two other

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members of the mem-elements namely memcapacitors and meminductors. A lot has already been done on memristor and it is presently available as an off-the-shelf component in the market. However, the same cannot be said for memcapacitor and meminductor. Consequently, the goal of this paper is to realize a simple meminductor emulator configuration. Mem-elements possess almost similar characteristics when a periodic signal is applied across their terminals. Pinched hysteresis loops (PHLs) are observed that indicate the existence of memory inside them. These PHLs have been observed between charge (q) and flux (ϕ) for memristor (M_R), whereas it is observed between charge (q) and voltage (v), and flux (ϕ) and current (i), for memcapacitor (M_C) and meminductor (M_L) respectively. The inter-relations among these mem-elements are given in Fig. 1 [11]. The following equations serve as a definition of meminductive systems.

$$\rho(t) = \int_{-\infty}^{t} \phi(t)dt \tag{1}$$

$$q(t) - \int_{-\infty}^{t} i(t)dt \tag{2}$$

$$d\rho = M_L dq \tag{3}$$

where M_L represents the meminductance of the emulator. From Eqs. (1), (2), and (3), the relation between flux (ϕ) and current (i) is deduced as:

$$\phi(t) = M_L i(t) \tag{4}$$

where i(t) and ϕ(t) are the meminductive current and induced flux respectively. The flux ϕ(t) of meminductor is defined as:

$$\phi(t) \int_{-\infty}^{t} V_{in}(t)dt \tag{5}$$

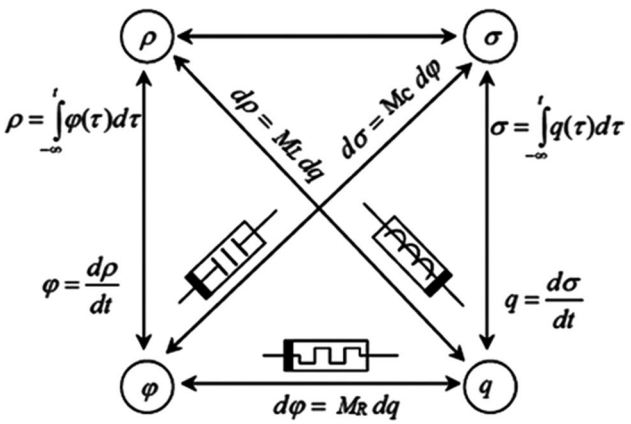

Fig. 1 Interrelations among mem-elements [11]

where $V_{in}(t)$ is the periodic signal applied across the meminductor.

In the literature, a number of meminductor emulators have been reported. The significant meminductors available in open literature have been summarized in Table 1. The objective of the work in this paper is to develop a single active building block (ABB) based floating meminductor emulator. The focus has been on realizing an electronically tunable meminductor with a simple structure, sparse use of passive components, and broad frequency operation.

The structure of the proposed meminductor is very simple and requires only one modified differential voltage current conveyor transconductance amplifier (MDVCCTA), one resistor, and two capacitors. The incremental and decremental modes of operation can be obtained by adding one switch at the input side. The proposed meminductor has the following characteristics: (i) the circuit is very simple and does not require any multipliers (ii) both incremental and decremental modes can be obtained (iii) flexible to use in both grounded and floating modes (iv) large frequency range (v) does not use any memristor. Various features such as, the number of analog building blocks, operating frequency, multiplier/multiplier-less, electronic tunability, number of passive components, floating/grounded mode, inductor/inductor-less, flux/charge controlled, incremental/decremental configurations, matching conditions, control parameters, and power supply are used to compare the proposed meminductor to previously reported circuits in the literature.

The following conclusions are drawn in view of the comparison shown in Table 1:

1. The proposed circuit uses only one MDVCCTA, whereas previously reported circuits in reference no. [13–35, 38, 39, 41, 42, 44–48, 50, 51, 53, 55–58, 61–63] use more than one building block.
2. The proposed emulator design does not require any memristor, whereas the circuits reported in reference no. [12, 14–16, 21, 25, 26, 37, 40, 43, 52, 53, 57] require a memristor for their implementation.
3. The recommended circuit is electronically tunable, but the meminductors reported in reference numbers [12–30, 36, 43, 49, 53, 56–59, 62] are not electronically tunable.
4. The suggested emulator can be operated in both grounded and floating modes, but the emulators reported in reference no. [12–15, 18, 22, 23, 27, 32–34, 36, 43, 46–49, 52, 53, 56–58, 60, 62] can only be operated in grounded mode.
5. The meminductor emulator of reference numbers [13, 18–20, 22–24, 27, 28, 31–33, 48, 49, 61] use multiplier but in the proposed circuit no multiplier is needed.
6. The meminductor emulators reported in reference numbers [12, 13, 16–24, 26–29, 31, 32, 35–37, 40, 43,

Table 1 Comparison with the work available in open literature

Ref. no.	No. and count of ABB	No. of R, C, L and M_R	Multiplier less	Operating Freq.	Electronic tunability	Power dissipation	Floating (F)/ Grounded (G)	Power supply	Flux(F)/ Charge (Q) controlled	Incremental(I)/ Decremental (D)	Control parameters	Need for matching conditions
[12]	1-OPAMP	1(R), 1(C), 0(L), 1(M_R)	Yes	8Hz	No	NA	G	–	–	–	R, C	No
[13]	3-OPAMP	2(R), 2(C), 1(L), 0(M_R)	No	300Hz	No	NA	G	±5V	Q	D	R, C	No
[14]	2-OPAMP	4(R), 1(C), 0(L), 1(M_R)	Yes	–	No	NA	G	–	F	D	R, C	Y
[15]*	2-OPAMP	7(R), 3(C), 0(L), 1(M_R)	Yes	2MHz	No	NA	G	±15V	F	D	R, C	No
[16]	3-OPAMP	6(R), 1(C), 0(L), 1(M_R)	Yes	10kHz	No	NA	F	–	F	D	R, C	NO
[17]	3-CFOA	2(R), 2(C), 0(L), 0(M_R)	Yes	10Hz	No	NA	F	–	F	D	R, C	Y
[18]	4-OPAMP	10(R), 2(C), 0(L), 0(M_R)	No	180Hz	No	NA	G	–	F	D	R, C	NO
[19]	6-OPAMP	9(R), 2(C), 0(L), 0(M_R)	No	800Hz	No	NA	F	–	F	D	R, C	Y
[20]	6-OPAMP	14(R), 2(C), 0(L), 0(M_R)	No	3kHz	No	NA	F	–	F	D	R, C	N
[21]	4-CCII+1-OPAMP	1(R), 1(C), 0(L), 1(M_R)	Yes	36.9Hz	No	NA	F	±15V	Q	D	R, C	N
[22]	2-CCII+3-OPAMP	8(R), 2(C), 0(L), 0(M_R)	No	800Hz	Now	NA	G	±5V	F	D	R, C	N
[23]	1-CCII+6-OPAMP	9(R), 2(C), 0(L), 0(M_R)	No	400Hz	No	NA	G	±5V	Q	D	R, C	Y
[24]	5-CCII+1-OPAMP	4(R), 2(C), 0(L), 0(M_R)	No	5kHz	No	NA	F	–	F	–	R, C	N

Table 1 (continued)

Ref. no.	No. and count of ABB	No. of R, C, L and M_R	Multiplier less	Operating Freq.	Electronic tunability	Power dissipation	Floating (F)/ Grounded (G)	Power supply	Flux(F)/ Charge (Q) controlled	Incremental(I)/ Decremental (D)	Control parameters	Need for matching conditions
[25]	4-CCII	1(R), 1(C), 0(L), 1(M_R)	Yes	---	No	NA	F	–	F	D	R, C	N
[26]	2-CCII	1(R), 1(C), 0(L), 1(M_R)	Yes	24.1Hz	No	NA	F	–	F	D	R, C	N
[27]	3-CCII	3(R), 2(C), 0(L), 0(M_R)	No	10Hz	No	NA	G	–	F	D	R, C	N
[28]	5-CCII	6(R), 2(C), 0(L), 0(M_R)	No	130kHz	No	NA	F	–	Q	D	R, C	Y
[29]	4-AD844+ 1-OPAMP	5(R), 2(C), 0(L), 0(M_R)	Yes	22kHz	No	NA	F	–	F	D	R, C	Y
[30]	4-AD844+1-OPAMP	6(R), 2(C), 0(L), 0(M_R)	Yes	1.5MHz	No	NA	F	–	Q	D	R, C	N
[31]	1-OTA+1-OPAMP	8(R), 2(C), 0(L), 0(M_R)	No	5kHz	Yes	NA	F	–	F	D	R, C, G_m	N
[32]*	2-OTA+ 1-multiplier	2(R), 2(C), 0(L), 0(M_R)	No	10kHz	Yes	2.25mW	G	–	F	D	R, C, G_m	N
[33]*	2-OTA+1-DVCC	1(R), 2(C), 0(L), 0(M_R)	No	10MHz	Yes	120µW	G	±1.2V	F	Both	R, C, G_m	N
[34]*	1-OTA+1-VDTA	0(R), 2(C), 0(L), 0(M_R)	Yes	3MHz	Yes	NA	G	±1.2V	F	Both	C, G_m	N
[35]*	2-OTA	0(R), 2(C), 0(L), 0(M_R)	Yes	900kHz	Yes	NA	F	±0.9V	F	Both	C, G_m	N
[36]	1-OTA	1(R), 1(C), 1(L), 0(M_R)	Yes	500Hz	No	NA	G	–	Q	D	R, C, G_m	N
[37]*	1-CBTA	0(R), 1(C), 0(L), 1(M_R)	Yes	100kHz	Yes	NA	F	–	Q	Both	C, G_m	N

Table 1 (continued)

Ref. no.	No. and count of ABB	No. of R, C, L and M_R	Multiplier less	Operating Freq.	Electronic tunability	Power dissipation	Floating (F)/ Grounded (G)	Power supply	Flux(F)/ Charge (Q) controlled	Incremental(I)/ Decremental (D)	Control parameters	Need for matching conditions
[38]*	2-VDTA	0(R), 2(C), 0(L), 0(M_R)	Yes	1.5MHz	Yes	NA	F	±0.9V	F	D	C, G_m	Y
[39]*	1-VDTA+ 1CDBA	0(R), 2(C), 0(L), 0(M_R)	Yes	2MHz	Yes	NA	F	±0.9V	F	Both	C, G_m	N
[40]*	1-VDCC	0(R), 1(C), 0(L), 1(M_R)	Yes	700kHz	Yes	NA	F	±0.9V	Q	Both	C	N
[41]*	2-VDTA	1(R), 2(C), 0(L), 0(M_R)	Yes	1MHz	Yes	NA	F	±0.9V	F	D	C, G_m	N
[42]*	2-OTA+1-CDBA	0(R), 2(C), 0(L), 0(M_R)	Yes	2MHz	Yes	NA	F	±0.9V	F	Both	C, G_m	N
[43]	1-OPAMP	3(R), 1(C), 0(L), 1(M_R)	Yes	126kHz	No	NA	G	±15V	C	I	R, C	Y
[44]*	1- 1-VDGA+ 1-CDBA	0(R), 2(C), 0(L), 0(M_R)	Yes	10MHz	Yes	100.35µW	F	±0.9V	F	Both	C, G_m	N
[45]*	1-VDIBA+1-CF	0(R), 2(C), 0(L), 0(M_R)	Yes	11MHz	Yes	9.99mW	F	±0.9V	F	Both	C, G_m	N
[46]*	3-OTA	0(R), 2(C), 0(L), 0(M_R)	Yes	10MHz	Yes	120µW	G	±1.2V	F	Both	C, G_m	N
[47]!	3-OTA	0(R), 2(C), 0(L), 0(M_R)	Yes	100 kHz	Yes	82.6 µW	G	±1.2V	F	I	C, G_m	N
[48]*	2-DDCC+ 1-MOS	2(R), 1(C), 0(L), 0(M_R)	No	1.5kHz	Yes	NA	G	–	F	Both	R, C	N
[49]	1-DOCCII+1-CCII	2(R), 2(C), 1(L), 0(M_R)	No	700Hz	No	NA	G	±12V	C	D	R, C	N
[50]*	1-VDTA+ 1-DOCCII	1(R), 2(C), 0(L), 0(M_R)	Yes	200kHz	Yes	8.58mW	F	–	F	Both	R, C, G_m	Y

Table 1 (continued)

Ref. no.	No. and count of ABB	No. of R, C, L and M_R	Multiplier less	Operating Freq.	Electronic tunability	Power dissipation	Floating (F)/ Grounded (G)	Power supply	Flux(F)/ Charge (Q) controlled	Incremental(I)/ Decremental (D)	Control parameters	Need for matching conditions
[51]*	1-MVDCC + 1-OTA	1(R), 2(C), 0(L), 0(M_R)	Yes	300kHz	Yes	NA	F	±0.9V	F	D	R, C, G_m	N
[52]*	1-VDBA	0(R), 2(C), 0(L), 1(M_R)	Yes	4.9Hz	Yes	NA	G	±1.5V	F	I	C	N
[53]	2-OPAMP	3(R), 1(C), 0(L), 1(M_R)	Yes	5kHz	No	NA	G	±9V	F	I	R, C	Y
[54]*	1-MOVDTA	0(R), 2(C), 0(L), 0(M_R)	Yes	50MHz	Yes	0.86mW	F	±0.9V	F	Both	C, G_m	N
[55]*	2-OTA+1-CDTA	0(R), 2(C), 0(L), 0(M_R)	Yes	1MHz	Yes	NA	F	±0.9V	C	Both	C, G_m	N
[56]*	1-OTA+1-CDBA+ 1-CCII	1(R), 2(C), 0(L), 0(M_R)	Yes	1MHz	No	NA	G	±0.9V	F	Both	R, C, G_m	N
[57]*	2-OPAMP	4(R), 1(C), 0(L), 1(M_R)	Yes	550kHz	No	NA	G	±9V	F	D	R, C	Y
[58]*	2-CDTA	0(R), 2(C), 0(L), 0(M_R)	Yes	500kHz	No	NA	G	±0.9V	F	D	C, G_m	N
[59]*	1-MVDVTA	1(R), 2(C), 0(L), 0(M_R)	Yes	500kHz	No	NA	F	±0.9V	F	I	R, C, G_m	N
[60]*	1-VDTA+ 2-MOS	0(R), 2(C), 0(L), 0(M_R)	Yes	25MHz	Yes	5.93mW	G	±0.9V	F	D	C, G_m	N
[61]*	1-OTA+ 1-MOOTA	1(R), 2(C), 0(L), 0(M_R)	No	1MHz	Yes	3.87mW	F	±1.25V	C	D	R, C, G_m	N
[62]	1-CCII+1-OTA	1(R), 1(C), 1(L), 0(M_R)	Yes	100kHz	No	NA	G	–	C	D	R, C, G_m	N
[63]*	1-VDBA+ 1-CDBA	1(R), 2(C), 0(L), 0(M_R)	Yes	2MHz	Yes	NA	F	±0.9V	F	Both	R, C, G_m	N

Table 1 (continued)

Ref. no.	No. and count of ABB	No. of R, C, L and M_R	Multiplier less	Operating Freq.	Electronic tunability	Power dissipation	Floating (F)/ Grounded (G)	Power supply	Flux(F)/ Charge (Q) controlled	Incremental(I)/ Decremental (D)	Control parameters	Need for matching conditions
Proposed work*	1-MDVCCTA	1(R), 2(C), 0(L), 0(M_R)	Yes	15MHz (perfect pinched point) 80 MHz (shifted pinched point)	Yes	3.82mW	G+F	±0.9V	F	Both	R, C, G_m	N

*Implemented using 0.18 µm technology parameter, †Implemented using 0.09 µm technology parameter, *R* Resistor, *C* Capacitor, *L* Inductor, *MR* Memritor, **Freq*. Frequency, *OPAMP* Operational Amplifier, *OTA* Operational transconductance amplifier, *DVCC* differential voltage current conveyor, *CCII* Second generation current conveyor, *CBTA* Current buffered transconductance amplifier, *VDTA* Voltage differencing transconductance amplifier, *CDBA* Current differencing buffered amplifier, *VDCC* Voltage differencing current conveyor, *VDGA* Voltage differencing gain amplifier, *VDIBA* Differencing inverting buffered amplifier, *CF* Current follower, *VDBA* Voltage differencing buffered amplifier, *MO-OTA* Multiple output operational transconductance amplifier, *MVDVTA* Modified voltage differencing voltage transconductance amplifier, *MVDCC* Modified voltage differencing current conveyor, *DDCC* Differential difference current conveyors

48, 48–53, 57–59] work satisfactorily in the operating frequency between Hz to kHz range but the proposed circuit operates up to MHz range. The operating frequency of the meminductor emulator reported in reference [54] is 50 MHz and in [60] is 25 MHz, whereas the proposed meminductor works up to 80 MHz with some shifting in cross-over point.

7. The limitation of the proposed meminductor emulator is the restricted range of tunability and shifted pinched point at higher frequencies.
8. The meminductor emulator of reference numbers [13, 15, 21–23, 32–34, 49, 52, 53, 57, 61] use high power supply voltage but in the proposed circuit use only ± 0.9 V.
9. The meminductor reported in the reference numbers [13, 21, 23, 28, 30, 36, 37, 40, 49, 55, 61, 62] are operated on charge-controlled mode whereas the proposed circuit operated on flux-controlled mode.
10. The proposed meminductor is working on both incremental and decremental mode but previously reported circuits in reference no [13–32, 36, 38, 41, 47, 49, 51–53, 57–62] is working on one mode only.
11. The meminductor reported in the reference numbers [14, 17, 19, 23, 28, 29, 38, 50, 53, 57] use matching conditions but the proposed circuit does not need any matching condition.

The work in the paper has been divided into 7 sections, including the 1st introductory section. Section 2 gives a brief description of the ABB used to design the suggested meminductor emulator. The explanation of the recommended meminductor along with its mathematical analysis has been given in Sect. 3. LTSpice results observed in 0.18 µm technology along with their appropriate discussion have been presented in Sect. 4. Section 5 focuses on the precision analysis and study of non-ideal aspects related to the proposed meminductor emulator. The section delineates variations in its fundamental characteristics concerning changes in temperature, supply voltage, and component parameters. Furthermore, it provides an in-depth exploration of the influence of non-idealities and parasitic components within the MDVCCTA block. Application of the suggested meminductor in implementing chaotic oscillator and adaptive learning circuit has been explained in Sect. 6. Finally, the conclusion summary of the work is given in Sect. 7.

2 Description of MDVCCTA

The differential voltage current conveyor transconductance amplifier (DVCCTA) is a comparatively new ABB proposed by Pandey and Paul in 2011 [64]. It integrates the traits of a transconductance amplifier (TA) and a

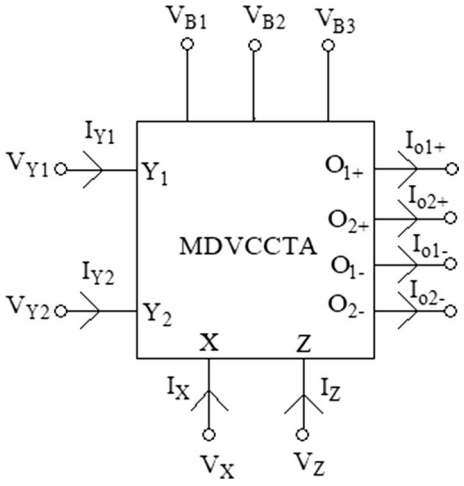

Fig. 2 Block diagram of MDVCCTA [64]

differential difference current conveyor (DDCC) [65]. The DVCCTA incorporates the adaptable and distinctive characteristics of DDCC, such as the simplicity with which differential and floating input circuits can be implemented, with the flexibility of in-built parameter tuning. The modified differential voltage current conveyor transconductance amplifier (MDVCCTA) is a modified version of a DVCCTA, which possess two transconductance amplifiers. The block diagram representing the input and output terminals of MDVCCTA is shown in Fig. 2. Y_1 and Y_2 are the differential input voltage terminals. X and Z are intermediate terminals responsible for generating voltage and current proportional to input voltage based on components attached to these terminals. O_+ and O_- are output current terminals of the transconductance amplifier unit and generate current proportional to the voltage developed at the Z terminal. The two transconductance gains of this unit can be controlled by biasing voltage V_{B2} and V_{B3}.

The matrix equation depicting the port relations of MDVCCTA is given by Eq. (6).

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z1} \\ I_{O1\pm} \\ I_{O2\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & \pm G_{m1} \\ 0 & 0 & 0 & \pm G_{m2} \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix} \tag{6}$$

In Eq. (6), G_{m1} and G_{m2} represent the transconductance gains of MDVCCTA. Assuming symmetric differential pairs, transconductance for the proposed circuit can be written as:

$$G_{m1,2} = K_{1,2}\left(V_{B2,B3} - V_{SS} - 2V_{th}\right) \tag{7}$$

here, β represents the transconductance parameter of the corresponding MOSFET, V_{SS} is the negative supply voltage and V_{th} is the threshold voltage of a MOSFET. In addition, V_{B2} and V_{B3} are the biasing voltages responsible for controlling the biasing current of first and second transconductance amplifiers respectively. Here, K_1 and K_2 are the transconductance parameters defined as:

$$K_1 = \frac{\sqrt{\beta_{13}\beta_{14}\beta_{16}}}{\sqrt{2}\left(\sqrt{\beta_{13}} + \sqrt{\beta_{14}}\right)} \tag{8}$$

$$K_2 = \frac{\sqrt{\beta_{30}\beta_{31}\beta_{33}}}{\sqrt{2}\left(\sqrt{\beta_{30}} + \sqrt{\beta_{31}}\right)} \tag{9}$$

The MOSFET-based complete circuit of MDVCCTA is illustrated in Fig. 3.

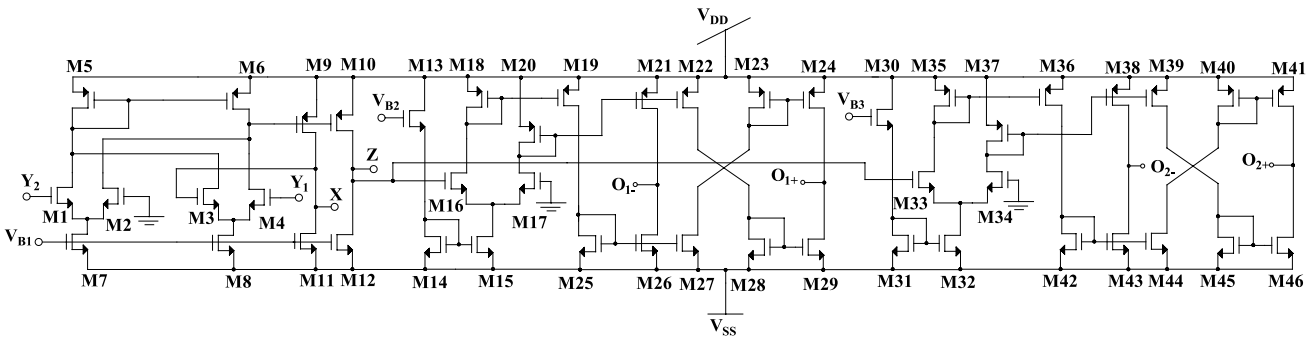

Fig. 3 Circuit diagram of MDVCCTA

3 Proposed MDVCCTA-based electronically tunable floating meminductor

Figure 4 depicts the complete design of meminductor emulator proposed in the paper. In this circuit, the differential input signal is directed between Y_1 and Y_2 terminals of MDVCCTA. This differential signal is transferred to the "X" terminal, where the resistor R_1 generates a current proportional to an input voltage signal. Further, this current is copied at the "Z" terminal of the MDVCCTA block. This current charge the capacitor C_1 connected at this node, leading to the generation of a voltage V_Z at the "Z" terminal. A current directly proportional to V_Z appears at the output terminal ($O_{\pm}$), which leads to a similar current to be drawn from the input voltage source. The output terminals are shorted to input Y terminals. These arrangements lead to the inductive behaviour of the circuit depicted in Fig. 4. A capacitor C_2 is connected to V_{B3} and as shown in the circuit, the current flowing through O_{1-} terminal charges this capacitor. This current being proportional to the input voltage (V_{in}), makes a feedback connection that ensures the meminductive input current to be dependent on the input flux (ϕ). This leads to the meminductive behaviour of the circuit.

3.1 Derivation of meminductance of proposed meminductor

The proposed meminductor can be used in incremental configuration ("x" connected to "a" and "y" connected to "b") as well as decremental configuration ("x" connected to "b" and "y" connected to "a"). Using the terminal equations of MDVCCTA depicted in Eq. 6 and performing basic analysis of the meminductor circuit given in Fig. 4 for incremental configuration, the terminal voltages V_X (Voltage at X terminal), V_Z (Voltage at Z terminal) and V_{B3} (Voltage at V_{B3} terminal) can be represented as:

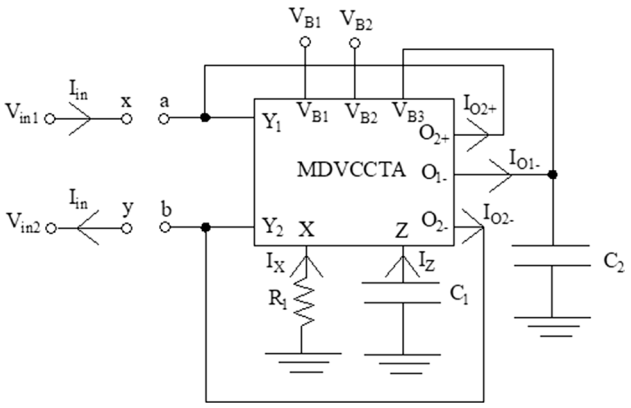

Fig. 4 MDVCCTA based proposed meminductor emulator

$$V_X = V_{Y1} - V_{Y2} = \left(V_{in1} - V_{in2}\right) = V_{in}(say) \tag{10}$$

$$V_Z = V_{C1} = -\frac{1}{C_1}\int_0^t I_Z dt = -\frac{1}{C_1}\int_0^t I_X dt \tag{11}$$

$$V_Z = -\frac{1}{C_1}\int_0^t \frac{-V_X}{R_1} dt = \frac{1}{C_1 R_1}\int_0^t V_{in} dt \tag{12}$$

Applying Kirchoff's voltage law, V_{B3} can be derived as:

$$V_{B3} = V_{C2} = \frac{1}{C_2}\int_0^t I_{O1-} dt = -\frac{1}{C_2}\int_0^t G_{m1} V_Z dt \tag{13}$$

Using the integral relations given by Eqs. (5) and (1), and performing mathematical simplification, Eqs. (9) and (10) can be expressed as:

$$V_Z = \frac{1}{C_1 R_1}\phi(t) \tag{14}$$

$$V_{B3} = -\frac{G_{m1}}{C_1 C_2 R_1}\rho(t) \tag{15}$$

Equations (14) and (15) have been written considering all the capacitances to be initially relaxed. Analysing circuit of MDVCCTA based meminductor shown in Fig. 4, input current (I_{in}) can be expressed as:

$$I_{in} = -I_{O1+} = -G_{m2} V_Z \tag{16}$$

Here, G_{m1} and G_{m2} are the two transconductance gains of the MDVCCTA block, that are defined by Eq. (7). Combining Eqs. (14) and (16) and later substituting G_{m2} and V_{B3} from Eqs. (7) and (15) respectively, I_{in} can be expressed as:

$$I_{in} = \frac{K_2}{C_1 R_1}\left[\frac{G_{m1}}{C_1 C_2 R_1}\rho(t) + V_{SS} + 2V_{th}\right]\phi(t) \tag{17}$$

From Eq. (17) and considering relation (4), M_L^{-1} of the proposed meminductor is given as:

$$M_L^{-1} = \left[\frac{K_2}{C_1 R_1}\left(V_{SS} + 2V_{th}\right) + \frac{K_2 G_{m1}}{C_1^2 C_2 R_1^2}\rho(t)\right] \tag{18}$$

fixed termvariable term

From Eq. (18), it can be analysed that meminductance of the suggested meminductor comprises of a fixed component and a variable component. The fixed term is dependent on the MOSFET threshold voltage and the circuit's negative supply voltage. However, the variable term depends on input voltage and can be controlled by passive components (C_1, C_2 and R_1) and transconductance of the amplifier.

The suggested meminductor design given in Fig. 4 can be used in decremental mode by connecting "x" node to "b" and

Table 2 Feature size of the MOSFETs of MDVCCTA block

MOSFET	W/L (μm/μm)	MOSFET	W/L (μm/μm)
M1-M4, M7, M8, M11-M13, M30	5/0.5	M18-M24, M35-M41	12.5/0.5
M5, M6, M9, M10	7.5/0.5	M14-M17, M25-M29, M31-M34, M42-M46	4/0.5

"y" node to "a" in the switch shown in Fig. 4. The derivation of meminductance of the proposed circuit in this configuration can be carried out using the steps similar to the incremental mode derivation. In this case, the terminal voltage and current equations can be derived as:

$$V_Z = -\frac{1}{C_1 R_1}\phi(t) \tag{19}$$

$$V_{B3} = \frac{G_{m1}}{C_1 C_2 R_1}\rho(t) \tag{20}$$

$$I_{in} = -I_{O1-} = G_{m2} V_Z = \frac{K_2}{C_1 R_1}\left[-\frac{G_{m1}}{C_1 C_2 R_1}\rho(t) + V_{SS} + 2V_{th}\right]\phi(t) \tag{21}$$

Using Eq. (21) and Eq. (4), $M_L{}^{-1}$ of the proposed meminductor in decremental configuration is given as:

$$M_L^{-1} = \left[\frac{K_2}{C_1 R_1}\left(V_{SS} + 2V_{th}\right) - \frac{K_2 G_{m1}}{C_1^2 C_2 R_1^2}\rho(t)\right] \tag{22}$$

Fixed termVariable term

In decremental configuration, the fixed term is positive while the variable term of meminductance is negative. However, the magnitude and dependency of both the terms are same as that of the incremental configuration.

In the derivation of the incremental and decremental meminductance relations for the proposed emulator, G_{m1} is supposed to be fixed. However, this gain term can be adjusted by regulating the bias voltage applied at V_{B2} terminal, imparting tunability feature to the proposed emulator.

4 Simulation results and discussion

The simulation results of the meminductor circuit designed in the paper have been shown in this section. These results have been generated in the LTspice tool. The MOSFETs of the CMOS-based MDVCCTA circuit have been implemented with a 0.18 μm model file. Supply voltage of ± 0.9 V, $V_{B1} = 0.1$ V and $V_{B2} = 0.4$ V have been used for the simulation of the MDVCCTA block. The feature size of the MOSFETs has been listed in Table 2. The basic characteristics of the suggested meminductor emulator have been plotted with $C_1 = C_2 = 5$pF and $R_1 = 1$kΩ.

4.1 Simulation results of proposed floating meminductor when operated in incremental configuration

Initially, the proposed meminductor emulator's characteristics working as an incremental meminductor have been studied. To achieve incremental mode, the switch is connected as "x" to "a" and "y" to "b". To examine the inductive behaviour of the proposed configuration, its transient response is observed with a bipolar signal of 100 mV amplitude and 10 kHz frequency. The waveforms observed for input current and flux (ϕ) have been shown in Fig. 5. The flux ($\phi = \int V_{in} dt$) was measured at the input terminal. The phase lag witnessed in flux and current waveforms determine the inductive nature of the proposed circuit.

Non-volatile behaviour is one of the most important fingerprints for meminductors. When a pulse signal is provided, it anticipates that the meminductance will change correspondingly during the pulse's ON time, while it retains its value during the OFF time of the pulse. To observe the non-volatile behaviour of the circuit, a pulse signal of 25 mV amplitude, with 1 μs ON period and 10 μs OFF period has been applied. The resultant meminductance is depicted in Fig. 6. This meminductance (M_L) has been obtained by dividing the flux (ϕ) by the input current.

(I_{in}). From this figure, it is evident that the meminductance remains constant during the OFF period of the input pulse but varies during the ON phase, validating the concept that the proposed meminductor is non-volatile.

Another essential feature of a meminductor is a pinched hysteresis loop (PHL) in flux (ϕ) vs. current (i) plane, when a bipolar signal is applied. A sinusoidal signal of 10 kHz frequency and 100 mV amplitude has been applied to the suggested meminductor and the response observed is plotted in Fig. 7.

The dumbbell shape of the PHL curve with zero-crossing, as seen in Fig. 7, further supports the proposed circuit's meminductive behaviour. The PHL curves are seen in the proposed meminductor for a wide range of input frequency signals. These loops for frequencies varying from 40 kHz to15MHz have been drawn in Fig. 8a and b. To obtain the PHL curves with zero-crossing for the specified range of frequencies, the passive components have been adjusted. The decreasing area of the PHL lobes with an increase in frequency is another essential feature

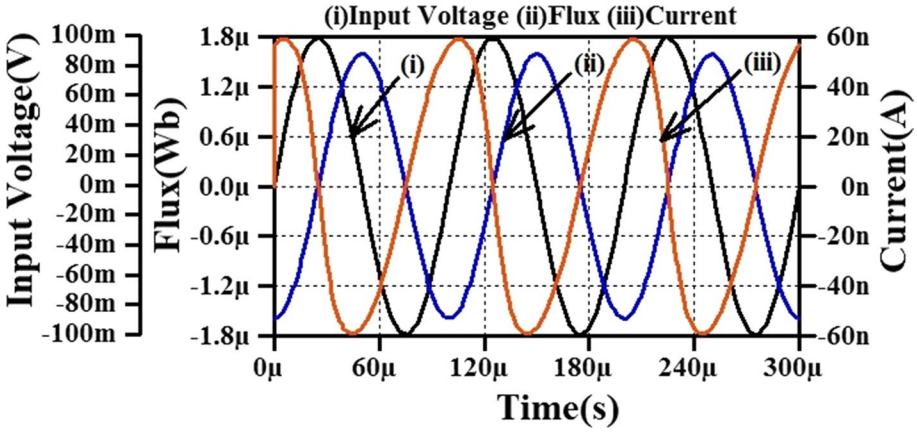

Fig. 5 Transient analysis of proposed meminductor

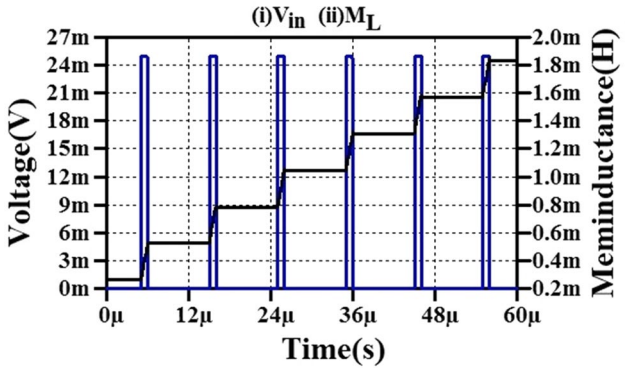

Fig. 6 Waveform showing variations in meminductance caused by the introduction of a pulse signal

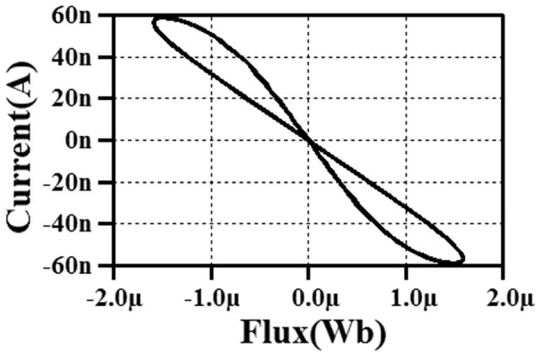

Fig. 7 Response of the proposed meminductor to a 10 kHz sinusoidal signal

of a meminductive device. The PHL curves of Fig. 8 provide a good visual representation of this characteristic.

Several applications demand capacitive tuning of a circuit. The circuit's capacitance tunability feature is determined by the property of change in PHL shape with changes in capacitance. To investigate this feature in the proposed meminductor, its response in φ vs. i plane for 10 kHz sinusoidal signal with different values of C_1 and C_2 has been analyzed. The curves obtained for varying C_1 and C_2 from 5 to 15pF have been plotted in Fig. 9. These curves shown in Fig. 9 depict the capacitance tunability feature of the proposed meminductor.

Electronic tunability is a feature that allows variations in key parameters of a circuit with changes in applied bias voltage or bias current. To illustrate the electronic tunability behaviour of the proposed meminductor, its PHL has been plotted in Fig. 10 for different values of V_{B2}. All these cures have been drawn for an input signal of 10 kHz, 100 mV sinusoidal signal.

4.2 Simulation results of proposed floating meminductor emulator when operated in decremental configuration:

The curves plotted in Figs. 7, 8, 9, 10 are for incremental configuration of the suggested meminductor emulator. It can be operated in decremental configuration, provided the switch is positioned to get the links between "x" to "b" and "y" to "a". The transient analysis curve and the PHL curve observed for this configuration for 10 kHz, 100 mV sinusoidal signal have been shown in Fig. 11a and b respectively. These curves for input signal frequency varying from 40 kHz to 15 MHz are shown in Fig. 12. All these curves show that the proposed meminductor operates satisfactorily in decremental configuration for frequencies range of 40 kHz–15 MHz.

At higher frequencies, shifting in the pinched point (v = 0, i = 0) is observed in PHL curves. The shifting of pinched point can be mitigated with proper selection of values of capacitors. The PHL curves observed are not deformed up to 80 MHz frequency, as can be seen in Fig. 13a–d.

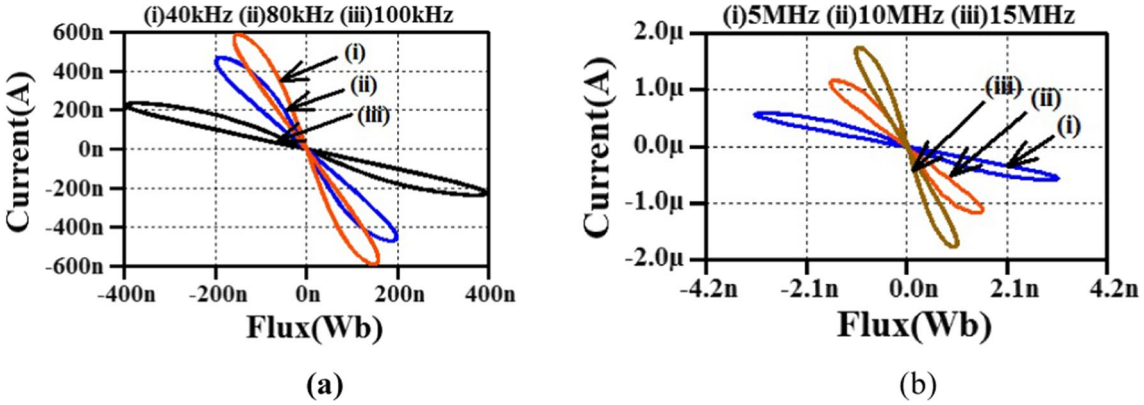

Fig. 8 PHL curves observed for the proposed meminductor for a frequency range (**a**) 40 kHz to 100 kHz and (**b**) 5–15 MHz

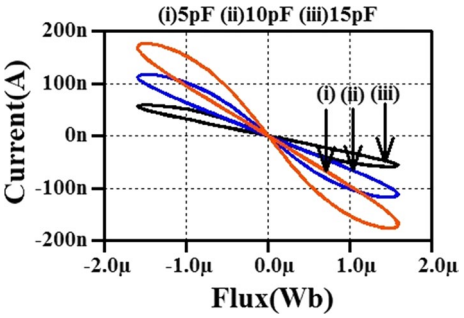

Fig. 9 PHL curves observed for the proposed meminductor for different values of capacitors

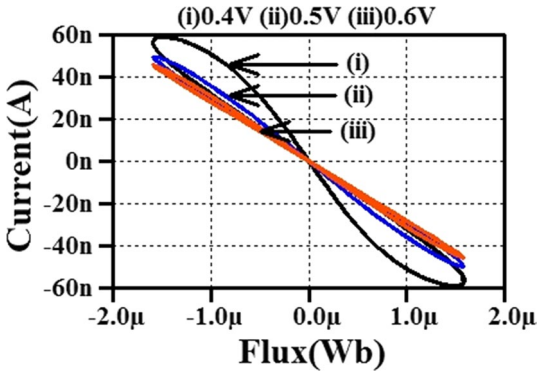

Fig. 10 PHL curves obtained for different values of V_{B2}

5 Precision analysis of proposed meminductor

Practically, a device will be subjected to different environmental and manufacturing conditions leading to variations in its behaviour. To check the tolerance of a device in a practical environment its behaviour must be examined under different values of parameters. The effects of varying the suggested meminductor's parameters have been examined in this section.

5.1 Temperature variation analysis

The proposed meminductor's behaviour with temperature fluctuations ranging from −55 °C to + 125 °C has been investigated. PHL curves obtained for incremental and decremental configuration of the proposed meminductor for the specified range of temperature variations have been shown in Fig. 14a and b. These figures illustrate how the proposed meminductor exhibits minor variations in the PHL curves' shapes, resulting in successful operation as meminductor within the designated temperature range.

5.2 Monte-Carlo analysis

A MOSFET is subjected to variations in aspect ratio and threshold voltage while being manufactured in a real environment. Monte Carlo (MC) analysis has been carried out to assess the effects of variations in the proposed meminductor's properties caused by fabrication limitations experienced by the constituent MOSFETs. The MC analysis has been performed with 5% variations in aspect ratio and the threshold voltage of MOSFETs using the Gaussian distribution function. The MC plots of PHL curves for a sinusoidal signal of 10 kHz frequency have been drawn in Fig. 15a and b for threshold variations for incremental and decremental meminductors respectively. These curves have been plotted for 100 runs. These MC plots illustrate that the shape of PHL curves is maintained while demonstrating only minor alterations because of changes in the MOSFET specifications, supporting the meminductive behaviour of the proposed circuit over the complete mismatch range.

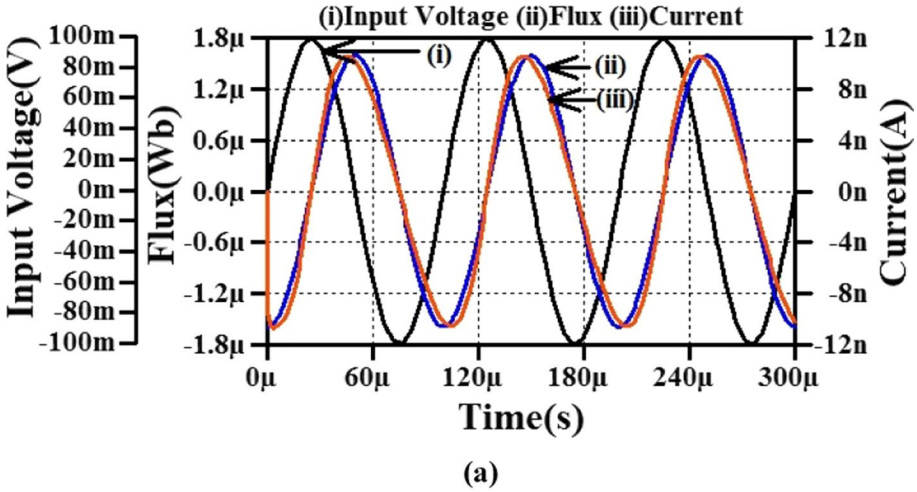

Fig. 11 (**a**) Transient analysis and (**b**) the PHL plotted on ϕ vs. i plane for the decremental configuration of proposed meminductor for a sinusoidal frequency of 10 kHz

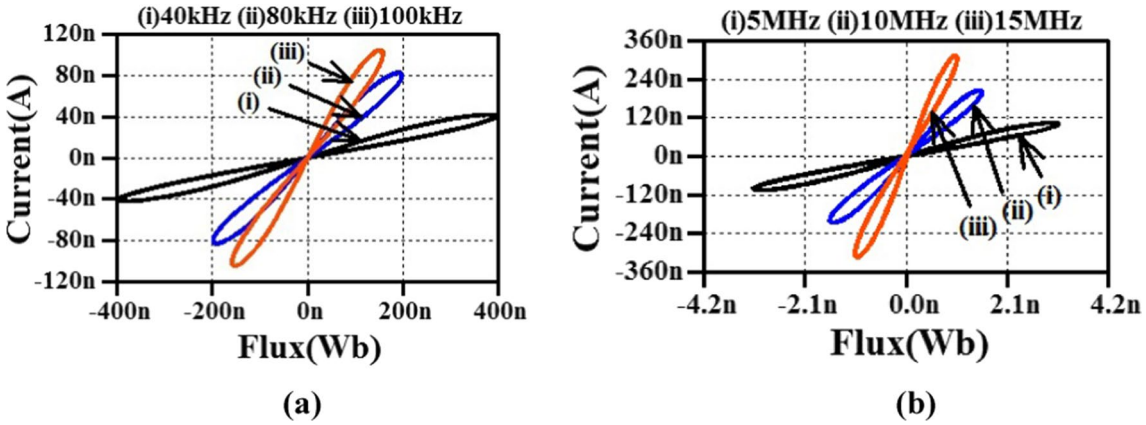

Fig. 12 PHL curves observed for the decremental configuration of proposed meminductor for a frequency range of 40 kHz to15MHz

5.3 Corner analysis

Based on fabrication technology and design environment, a MOSFET can undergo variations in design parameters. It has been observed that there is an upper and lower limit to the variations that can appear during a particular fabrication process. In view of this, 4 design corners have been specified for CMOS-based circuits. These design corners are: fast–fast (FF), fast-slow (FS), slow-fast (SF) and slow-slow (SS). In all these corners, the first term signifies the NMOS characteristic, and the second term represents PMOS behaviour. To ensure the robust operation of the proposed circuit, its behaviour at four different corners has been studied. The PHL curves observed

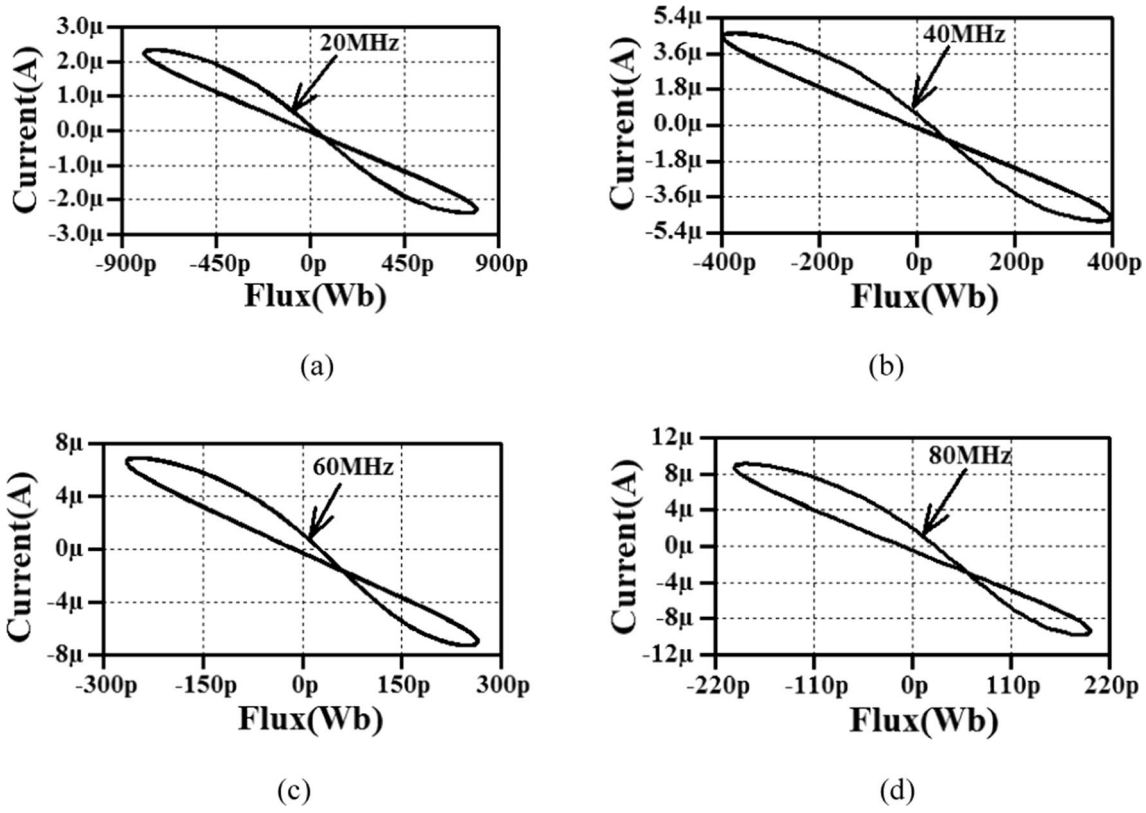

Fig. 13 PHL curves observed for the incremental configuration of proposed meminductor for a frequency range of 20–80 MHz

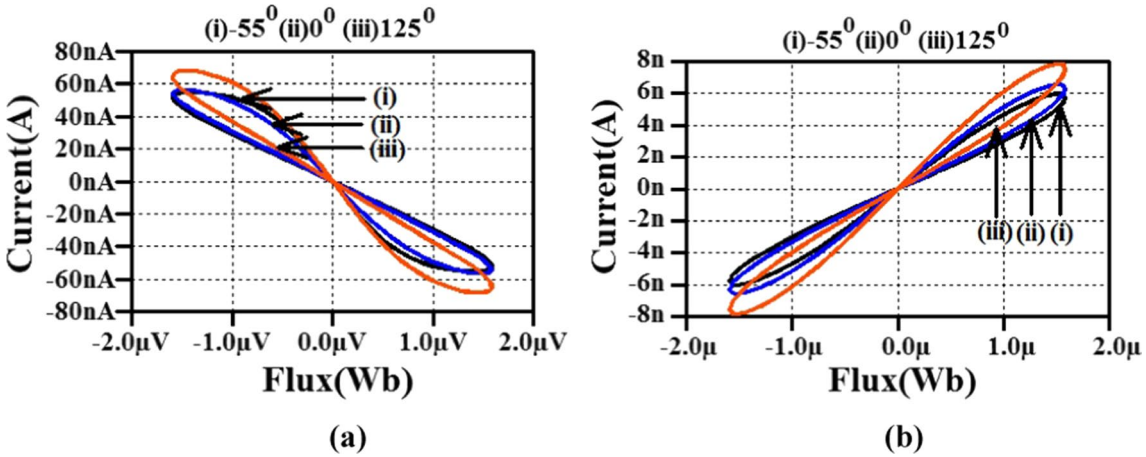

Fig. 14 PHL curves of proposed meminductor for temperature fluctuations from −55 to 125 °C (**a**) Incremental (**b**) Decremental

for these design corners along with typical curves for a sinusoidal signal of 10 kHz have been shown in Fig. 16. From Fig. 16, it can be analysed that the PHL loops are observed at all the corners, confirming the effective functioning of the suggested design in the entire design space.

5.4 Supply voltage variations

To analyse the effect of supply voltage variations on the behaviour of the proposed meminductor, the MDVCCTA block has been subjected to a variation of ± 10% in supply voltage. The proposed meminductor incorporating this MDVCCTA block is simulated with a sinusoidal signal of

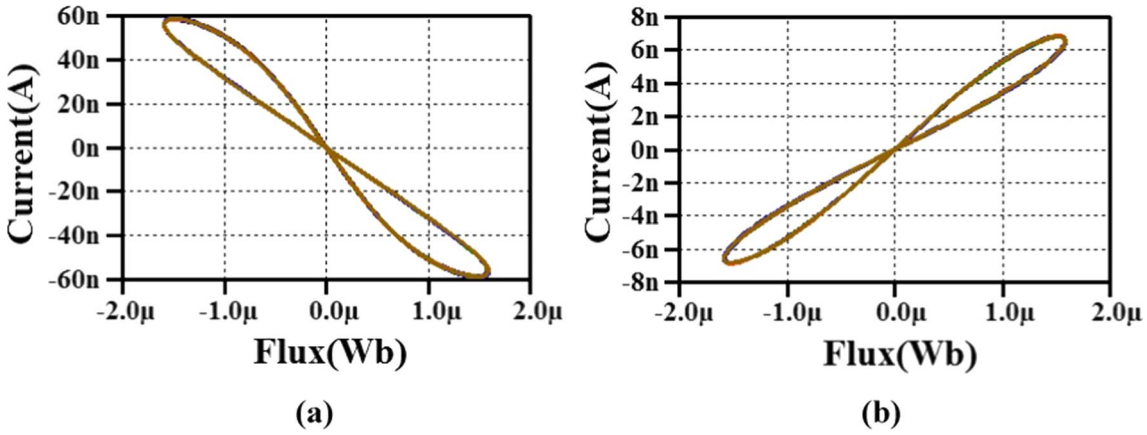

Fig. 15 PHL curves observed with Monte Carlo analysis for the proposed meminductor for 5% variations in (**a**) aspect ratio (**b**) threshold voltage

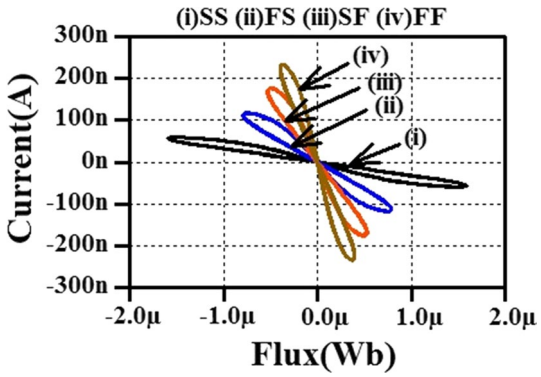

Fig. 16 PHL curves observed with corner analysis for the proposed meminductor emulator

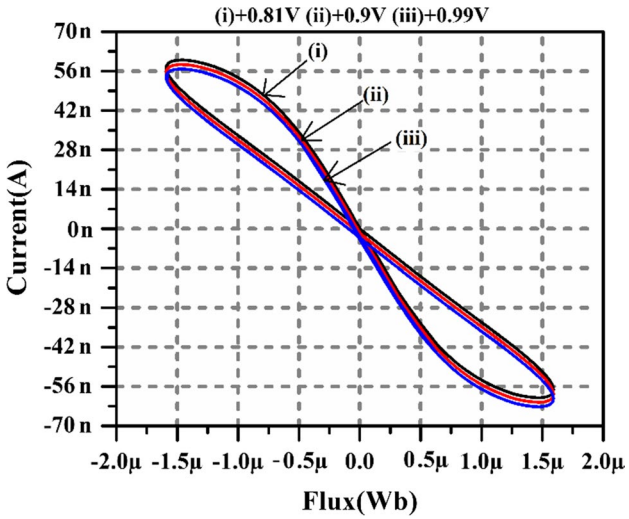

Fig. 17 PHL curves of the proposed meminductor observed with ± 10% deviations in supply voltage

10 kHz frequency and the resultant PHL curve observed in ϕ vs. i plane has been recorded in Fig. 17. These waveforms plot the PHL curves for variations in supply voltage from 0.81 to 0.99 V for V_{DD} and −0.81 to −0.99 V for V_{SS}. PHL curves shown in Fig. 17 confirm that the proposed meminductor operates satisfactorily with minor changes in lobe shape for ± 10% deviations in supply voltage.

5.5 Variations due to resistance tolerance

Precise values of the components can never be achieved at the time of fabrication. There is always some tolerance in the component values, which may sometimes lead to circuit failure. To examine the effect of the variations in resistance values, the proposed meminductor has been simulated for different values of resistors. The PHL curves for the incremental and decremental meminductor, observed with different values of R_1 (10kΩ, 20kΩ, and 30kΩ) have been plotted in Fig. 18.

The figures from Figs. 14, 15, 16, 17, 18 show the tolerance of the proposed meminductor to changes in temperature, supply voltage, and component characteristics. All of these figures reveal that the PHL lobe's shape changes slightly while preserving the necessary shape when any of these parameters changes.

5.6 Non-ideal and parasitic analysis

The mathematical analysis and derivations presented in Sect. 3 were based on the assumption that the MDVCCTA depicted in Fig. 4 is ideal. In this analysis, the current and voltage transfers at various ports of the MDVCCTA block were treated as ideal, as indicated by Eq. (6). Additionally, the presence of parasitic elements in the active devices used to implement the block were disregarded. In this section,

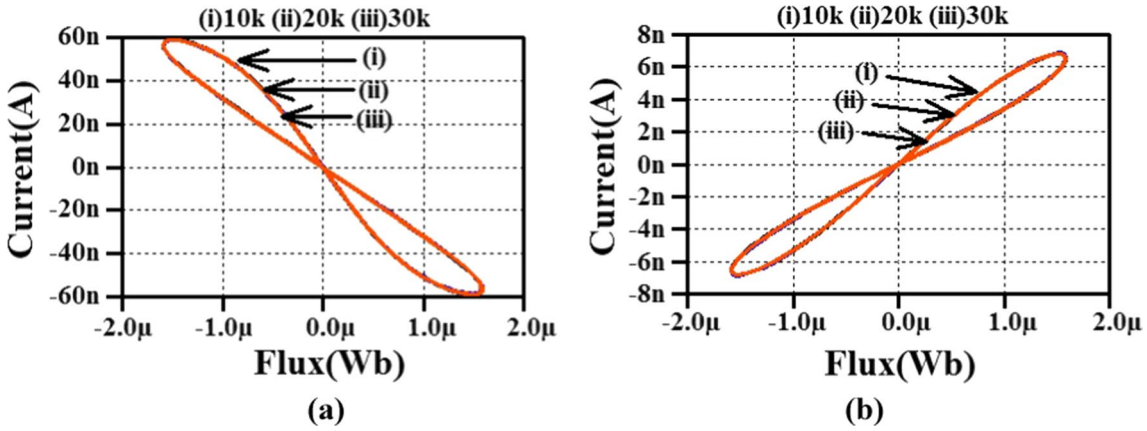

Fig. 18 PHL curves of the proposed meminductor observed with ± 10% deviations in R_1 (**a**) Incremental (**b**) Decremental

the meminductance of the proposed block has been derived while considering the impact of these non-ideal parameters and parasitic components. The port matrix of the MDVCCTA, accounting for non-idealities, can be expressed as:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_{Z1} \\ I_{O1\pm} \\ I_{O2\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha & -\alpha & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \pm\gamma G_{m1} \\ 0 & 0 & 0 & \pm\gamma G_{m2} \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix} \tag{23}$$

In Eq. (23), α and β denote the non-ideal voltage and current gains at terminals 'X' and 'Z' of the MDVCCTA, while γ represents the non-ideal parameter affecting the transconductance gain at port 'O' of the MDVCCTA. These parameters assume a value of unity in the ideal case. The equivalent circuit of the proposed meminductor, accounting for parasitic capacitors and resistors at various terminals of the MDVCCTA block, is illustrated in Fig. 19 [66].

To simplify the analysis, one terminal of the input voltage source is grounded. In this circuit, each parasitic component is identified by a superscript corresponding to the terminal at which it is present, while R_s represents the source resistance. Taking into account the non-idealities expressed by Eq. (23) and the parasitic components depicted in Fig. 19, the subsequent section provides the mathematical analysis of the meminductance for the proposed emulator.

Considering the specified non-idealitites and parasitics, port equations of MDVCCTA can be expressed as:

$$V_X = \alpha V_{Y1} \tag{24}$$

$$I_X = -\frac{V_X}{R_1 + R_X} \tag{25}$$

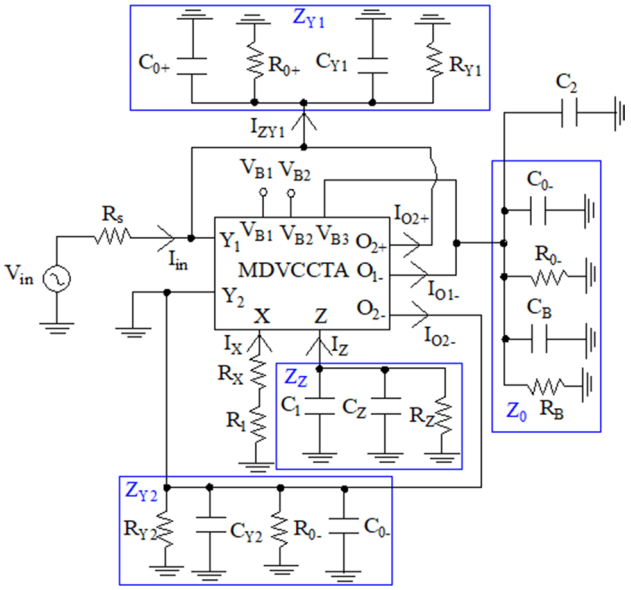

Fig. 19 Equivalent circuit of the proposed meminductor including the parasitic capacitors and resistors at different terminals

$$I_{01+} = \gamma G_{m1} V_Z \tag{26}$$

$$I_{02+} = \gamma G_{m2} V_Z \tag{27}$$

Simple analysis of node 'Z' reveals:

$$V_Z = -I_Z \bullet Z_Z = -\beta \bullet I_X \bullet Z_Z \tag{28}$$

Substituting the value of I_X and V_X from Eqs. (24) and (25), yields:

$$V_Z = \alpha\beta Z_Z \bullet \frac{V_{Y1}}{(R_1 + R_X)} \tag{29}$$

Applying Kirchoff's current law at node 'Y_1' gives:

$$I_{in} = \frac{V_{Y1}}{Z_{Y1}} - I_{02+} \tag{30}$$

Using Eqs. (23) and (29), I_{in} can be expressed as:

$$I_{in} = \frac{V_{Y1}}{Z_{Y1}} - \alpha\beta\gamma Z_Z \bullet \frac{G_{m2}V_{Y1}}{(R_1 + R_X)} \tag{31}$$

Considering source resistor (R_s), Eq. (31) can be expressed as:

$$\frac{V_{in} - V_{Y1}}{R_S} = \frac{V_{Y1}}{Z_{Y1}} - \alpha\beta\gamma Z_Z \bullet \frac{G_{m2}V_{Y1}}{(R_1 + R_X)} \tag{32}$$

Simplifying Eq. (32), V_{Y1} can be obtained as:

$$V_{Y1} = \frac{Z_{Y1}(R_1 + R_X)}{(Z_{Y1} + R_S)(R_1 + R_X) - \alpha\beta\gamma G_{m2}R_S Z_Z Z_{Y1}} \bullet V_{in} \tag{33}$$

From Eq. (28), it can be analyzed that:

$$V_Z = -\frac{I_Z}{\frac{1}{R_Z} + s(C_1 + C_Z)} \tag{34}$$

Assuming, $1/R_Z << s(C_1+C_Z)$ for the operating frequency range, Eq. (34) can be simplified as:

$$V_Z \approx -\frac{I_Z}{s(C_1 + C_Z)} = -\frac{1}{(C_1 + C_Z)}\int_0^t I_Z dt \tag{35}$$

Using Eqs. (23), (24), (25), and (33), along with Eq. (5) that represents flux of meminductor as time integral of input voltage, V_Z can be defined as:

$$V_Z = \frac{\alpha\beta}{(C_1 + C_Z)(R_1 + R_X)} \bullet \frac{Z_{Y1}(R_1 + R_X)}{(Z_{Y1} + R_S)(R_1 + R_X) - \alpha\beta\gamma G_{m2}R_S Z_Z Z_{Y1}}\phi(t) \tag{36}$$

Simple analysis of Fig. 18 shows that:

$$V_{B3} = I_{01-} \bullet \left(Z_0 \parallel \frac{1}{sC_2}\right) = I_{01-} \bullet \frac{1}{\frac{1}{R_{0-}} + \frac{1}{R_B} + s(C_{0-} + C_B + C_2)} \tag{37}$$

Assuming, $\left(\frac{1}{R_{0-}} + \frac{1}{R_B}\right) \ll s(C_{0-} + C_B + C_2)$, and substituting I_{01-} from Eqs. (23), (37) can be simplified as:

$$V_{B3} = -\frac{\gamma G_{m1}V_Z}{s(C_{0-} + C_B + C_2)} = -\frac{\gamma G_{m1}}{(C_{0-} + C_B + C_2)}\int_0^t V_Z \tag{38}$$

Substituting V_Z from Eq. (36) and using flux relation given by Eqs. (1), (38) can be modified as:

$$V_{B3} = -\frac{\gamma G_{m1}}{(C_{0-} + C_B + C_2)} \frac{\alpha\beta}{(C_1 + C_Z)(R_1 + R_X)} \bullet \frac{Z_{Y1}(R_1 + R_X)}{(Z_{Y1} + R_S)(R_1 + R_X) - \alpha\beta\gamma G_{m2}R_S Z_Z Z_{Y1}}\rho(t) \tag{39}$$

Performing routine analysis at node 'Y_1', it can be analysed that:

$$I_{O2+} = \frac{\alpha\beta\gamma G_{m2}V_{Y1}}{Z_Z} \tag{40}$$

Carrying out simple mathematical analysis on Eqs. (30) and (40), yields:

$$I_{in} = -\gamma \frac{\alpha\beta}{(C_1 + C_Z)(R_1 + R_X)} \bullet \frac{Z_{Y1}(R_1 + R_X)}{(Z_{Y1} + R_S)(R_1 + R_X) - \alpha\beta\gamma G_{m2}R_S Z_Z Z_{Y1}} \left\{1 - \frac{1}{\frac{\alpha\beta\gamma G_{m2}Z_{Y1}}{Z_Z}}\right\} G_{m2}\phi(t) \tag{41}$$

Using Eq. (7), I_{in} and M_L^{-1} of proposed meminductor while considering parasitics and non-idealities are expressed by Eq. (42) and (43) respectively.

$$I_{in} = K\gamma\eta\left\{1 - \frac{1}{\delta Z_{Y1}}\right\}\left[\frac{\gamma\eta G_{m1}}{C_{02eq}}\rho(t) + V_{SS} + 2V_{th}\right]\phi(t) \tag{42}$$

$$M_L^{-1} = K\gamma\eta\left\{1 - \frac{1}{\delta Z_{Y1}}\right\}\left[\frac{\gamma\eta G_{m1}}{C_{02eq}}\rho(t) + V_{SS} + 2V_{th}\right] \tag{43}$$

here,

$$\eta = \frac{\alpha\beta}{(C_1 + C_Z)(R_1 + R_X)} \cdot \frac{Z_{Y1}(R_1 + R_X)}{(Z_{Y1} + R_S)(R_1 + R_X) - \alpha\beta\gamma G_{m2}R_S Z_Z Z_{Y1}},$$
$$\delta = \frac{\alpha\beta\gamma G_{m2}}{Z_Z}, and C_{02eq} = (C_{0-} + C_B + C_2) \tag{44}$$

Analysis of Eqs. (42), (43), and (44) reveals that the parasitic elements, namely R_X, C_Z, C_0, and C_B, can be effectively disregarded by consolidating them with R_1, C_1, and C_2, respectively. Additionally, assuming R_{0+} and R_{Y1} to be significantly large, and C_{Y1} and C_{0+} to be extremely small, enables the neglect of the minor current I_{ZY1} in comparison to I_{in}. These considerations collectively contribute to the robust and practically stable behavior of the proposed meminductor.

6 Applications of proposed meminductor

In this section, to demonstrate the viability of the suggested meminductor emulator, two applications—chaotic oscillator and adaptive learning circuit—have been implemented.

6.1 Chaotic oscillator

Since the previous three decades, the chaos phenomena has been extensively explored in a variety of scientific fields, including physics, ecology, biology, optics, etc. An intriguing and straightforward tool for researching and creating chaos in electronic and communication systems is Chua's chaotic oscillator. This circuit exhibits rich dynamics, is simply built, and is tractable mathematically. These features have made Chua's oscillator a popular choice for producing chaotic signals for real-world applications, including: music, secure communications, neural networks, nonlinear waves, and visual sensing [67, 68]. This oscillator's architecture is mostly built around Chua's diode, an active three-segment nonlinear resistor. In Fig. 20, a simple fourth-order chaotic oscillator is displayed [18]. In this circuit, Chua's diode has been replaced with the proposed meminductor emulator. The negative resistance required in the circuit has been implemented using OPAMP based negative impedance converter (NIC). The four state variables of this circuit are: voltage across capacitor C_1 (V_{C1}), voltage across capacitor C_2 (V_{C2}), current through inductor L (I_L), and current through meminductor M_L (I_{ML}).

The state-equations representing first-order dynamics of this circuit are given as:

$$C_1\frac{dV_{C1}}{dt}+I_L=\frac{V_{C1}}{R_2};C_2\frac{dV_{C2}}{dt}+I_{ML}=I_L;$$
$$L\frac{dI_L}{dt}+I_L\cdot R_1=V_{C1}-V_{C2};M_L\frac{dI_{ML}}{dt}=V_{C2} \quad (45)$$

here C_1, C_2, L, M_L, R_1 and R_2 denote the values (capacitance, inductance, meminductance or resistance) of the corresponding element. The suitable values of these component parameters have been chosen in order to obtain chaotic response across state variables of the circuit. For the chaotic circuit depicted in Fig. 20, various projection plots generated in LTspice have been plotted in Fig. 21. These plots have been observed with the parameter's values chosen as $C_1=65$nF, $C_2=10$nF, $L_1=60$mH, $R_1=100\Omega$, and $R_2=-2k\Omega$. The required value of R_2 has been obtained with $Ra=2k\Omega$ and $Rb=2k\Omega$. Here, M_L has been replaced by proposed MDVCCTA based meminductor.

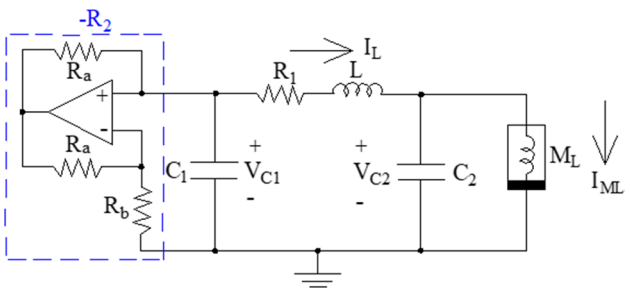

Fig. 20 A third-order Chua's chaotic oscillator

6.2 Adaptive learning circuit

The neuromorphic circuit using proposed meminductor emulator is presented in Fig. 22. The meminductors are found to be more suitable for neuromorphic applications as compared to memristors [69]. The proposed meminductor emulator circuit has been used in adaptive learning circuit to demonstrate how it adjusts its meminductance to achieve the appropriate resonance frequency of the circuit according to the applied input voltage (V_{in}). The response of the circuit mimics the behaviour of amoeba that is one of the simplest creatures on earth having brain-like behaviours in terms of controlling their actions based on the past events. The amoeba's locomotive speed is influenced by its surrounding temperature. Amoeba reduces its locomotive speed when temperature falls. The adaptive learning circuit shown in Fig. 22 behaves the similar way. The input pulse (V_{in}) represents the surrounding temperature, and the output voltage (V_{out}) represents the locomotive speed of amoeba. The amplitude of output voltage (amoeba's locomotive speed) gets reduced when the input voltage (temperature) drops. The pattern of input voltage follows the three cases: drops in voltage (reduced temperature), rise in voltage (increased temperature), and the constant voltage (no change in temperature) as shown in Fig. 23. Initially, voltage is maintained constant, and it gets reduced after some time to a particular level. Thereafter, the voltage is increased to achieve the same level from where it started. The same process is repeated thrice initially and thereafter maintains the constant voltage for a specific time and again follows the same pattern for one period. This pattern is applied to provide all scenarios that amoeba faces in terms of temperature. The amoeba locomotive speed gets reduced, increased, and maintained constant for reduction, increment, and constant temperature, respectively. In the similar way, the output response (V_{out}) of the circuit closely follows the behaviour of input pulse due to inherent ability of remembrance of meminductor as can be seen from Fig. 23. Therefore, the adaptive learning circuit is made to anticipate the amoeba's behaviour in response to changes temperature in the environment. Three steps can be used to define the amoeba's learning process: storage of previous occurrences, future forecasting, and comprehension of the timing of recurrent events [70, 71]. An element with memory retention capabilities can be employed to simulate an adaptive learning circuit with amoeba-like behavioural responses. Therefore, the proposed meminductor emulator circuit is

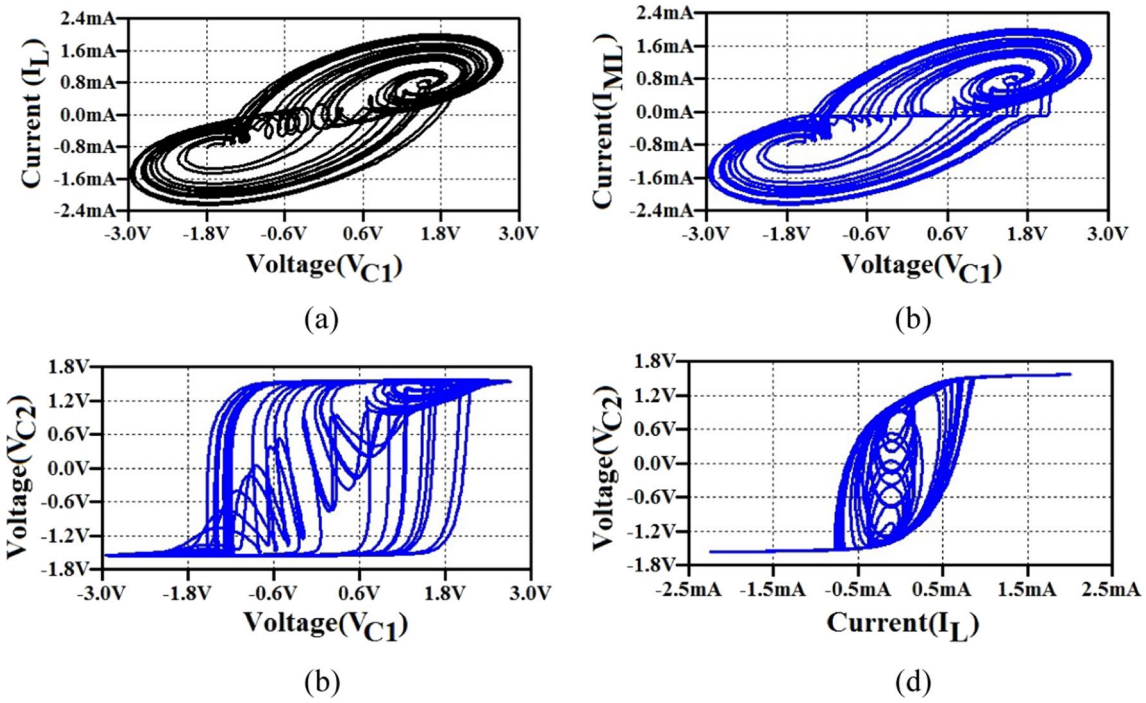

Fig. 21 Projection plots of chaotic oscillator observed between space variables (**a**) I_L & V_{C1} (**b**) I_{ML} & V_{C1} (**c**) V_{C2} & V_{C1} (**d**) V_{C2} & I_L

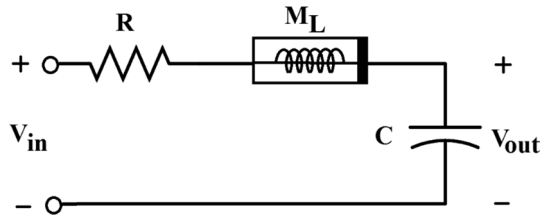

Fig. 22 Electrical model of adaptive learning circuit using proposed meminductor

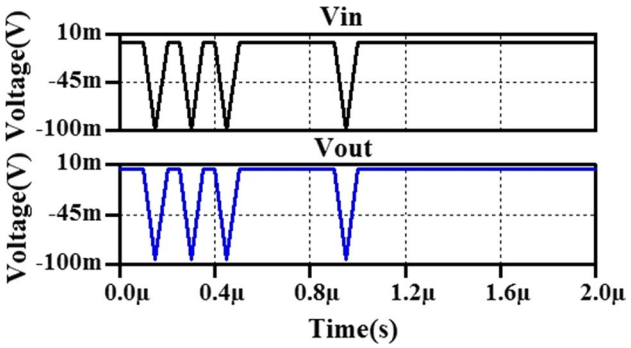

Fig. 23 Locomotive response against temperature fluctuations as seen by adaptive learning circuit of Fig. 22

employed to realize an adaptive learning circuit. This circuit is implemented with the help of a resistor (R), a capacitor (C), and the suggested meminductor (M_L).

7 Conclusion

The possibility of designing a single active block-based floating meminductor has been explored. The modified differential voltage current conveyor transconductance amplifier has been chosen due to its simple structure along with differential and in-built tuning features. The proposed circuit's appropriate operation has been confirmed by looking at the essential meminductor fingerprints, pinched hysteresis loops with zero-crossing and non-volatility tests. Through a simple switch connected at the input terminals, it has been demonstrated that the suggested circuit can operate in both incremental and decremental modes. The simulation results obtained in LTspice show the workability of the proposed circuit till 80 MHz while consuming 3.82mW power. The pinched hysteresis loops observed with temperature variations from −55 °C to + 125 °C, variations in resistance from 10 to 30kΩ, and ± 10% variations in supply voltage confirm the suitability of the proposed circuit in a practical environment. Additionally, Monte Carlo and corner analyses demonstrate the suggested meminductor's robustness. Furthermore, the successful design of a chaotic oscillator and an adaptive learning circuit utilizing the suggested meminductor has been illustrated.

Author's contribution Dr. SKR and Dr. RD contributed to the conception of ideas and circuit design. Material preparation and data collection were performed by Dr. RD and Dr. SKR. Simulations and analyses

were performed by Dr. RD and Dr. BA. All authors have contributed to writing the manuscript and approved the final manuscript.

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Code availability The code is available with corresponding author. It can be provided on reasonable request.

Declarations

Conflict of interest There is no conflict of interest.

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