



Schmitt trigger-based single-ended stable 7T SRAM cell

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Abstract

In this paper, a schmitt trigger-based single-sided 7T stable SRAM is proposed for ultra-low energy and near-threshold operation, which supports a bit interleaving scheme. The proposed ST-7T SRAM design improves the WSNM (Write Static Noise Margin) and RSNM (Read Static Noise Margin) and consumes less energy. Moreover, obtain high read strength by utilizing a single-sided ST (schmitt trigger) inverter. Furthermore, write ability is also enhanced by applying an ST inverter write assist scheme (Negative V_{WWL} technique), which can limit the tripping voltage of the ST inverter circuit. The PST-7T (Proposed ST-7T) circuit minimizes the read power by 49.96%, write power by 39.27%, and leakage power by 39.17% compared to conventional-6T SRAM. The RSNM and WSNM of the proposed SRAM circuit are enhanced by 66.28% and 18.97% compared to conventional-6T SRAM. The write energy and read energy utilization are also lowered by 14.87% and 14.19% compared to the SE7T SRAM cell.

Keywords Near threshold · SRAM (Static Random Access Memory) · Schmitt trigger · Bit interleaving scheme · Ultra-low energy

1 Introduction

Growing demand for low-power portable devices such as, energy harvesting devices, bio-implants, self-driven wireless sensors, etc., a low power system-on-chip (SoC) design has become more significant because of limited battery life. Since a significant portion of SoC is occupied by SRAM, reducing SRAM's energy utilization is a principal way to minimize the overall energy utilization of the chip [1]. Therefore, the design of robust ultra-low energy SRAM has become significant and draws the attention of researchers. However, such a low-power SRAM cell design encounters a lot of performance-related and process challenges [2]. Because in the deep nanometer region, the operation is very difficult due to enlarged device alterations. Reduction of power by supply voltage (VDD) scaling is the best way to minimize energy utilization [3]. As the VDD is scaling down power consumption decreases quadratically but soft error

rate, delay, and yield will be degraded. In the subthreshold region, the delay increases exponentially, where VDD is less than the threshold voltage. So, the operation in the near-threshold region where the supply voltage is slightly larger than the V_{th} (threshold voltage) can accomplish a large reduction in power and enhancement in delay compared to the sub- V_{th} operation [4]. But, the problem in the near-threshold region is soft error induced by alpha particles. These high-energy α -particles can strike the cell and damage the memory cell or interrupt the operation. Bit interleaving structure is applied in the near- V_{th} region to sort out the enhanced soft error rate [5]. In bit-interleaving structure fragments(bits) of the word are interleaved spatially. So, one-bit errors occurred and they can be removed by easy error correction circuits (ECC).

Conventional 6T SRAM suffers from reading disturbance-induced static noise margin degradation with VDD scaling. So, it is hard to get enough read and write stability at a time. To achieve adequate read and write stability in near-threshold operation, various SRAM cell configurations have been proposed [6–11]. However, these cells have some drawbacks such as large cell size, energy consumption, etc. Here, we propose a single-sided ST-7T SRAM cell, which consumes low energy and occupies a smaller area while ensuring near-threshold stability. To operate SRAM under

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PVT variations successfully, the cross-connected inverter's stability is significant [7]. Furthermore, PST-7T SRAM provides a high read static noise margin, lower power consumption, and robustness to PVT variations.

The arrangement of this paper is done as follows. Section II discusses the earlier reported SRAM cells. The proposed design is introduced in Section III. The Comparison of simulated results is described in section IV. Finally concluded in Section V.

2 Earlier reported SRAM cells

2.1 Conventional-6T SRAM

The conventional-6T SRAM cell is depicted in Fig. 1a [8]. However, this cell faces read and write stability issues at lower supply voltage. By using minimum-size access transistors, the read stability can be improved, but it will degrade

the write ability. Since write ability and read stability are the main design constraints. Thus, it is challenging to operate 6T SRAM in the sub-threshold region. Another challenge in 6T-SRAM is the small ON-OFF current ratio of access transistors, which does not allow the incorporation of a greater number of cells in every vertical column of a memory array. To overcome these problems, researchers have implemented different SRAM cell configurations.

2.2 ST-10T SRAM cell

The ST-10T SRAM cell depicted in Fig. 1b uses two cross-connected schmitt trigger-based inverters [9]. It also experiences reading disturbance, but the data stored is not inverted due to the improved read stability of the schmitt trigger inverter. However, this cell faces the issue of energy utilization and area overheads due to the differential bit line structure and a greater number of transistors.

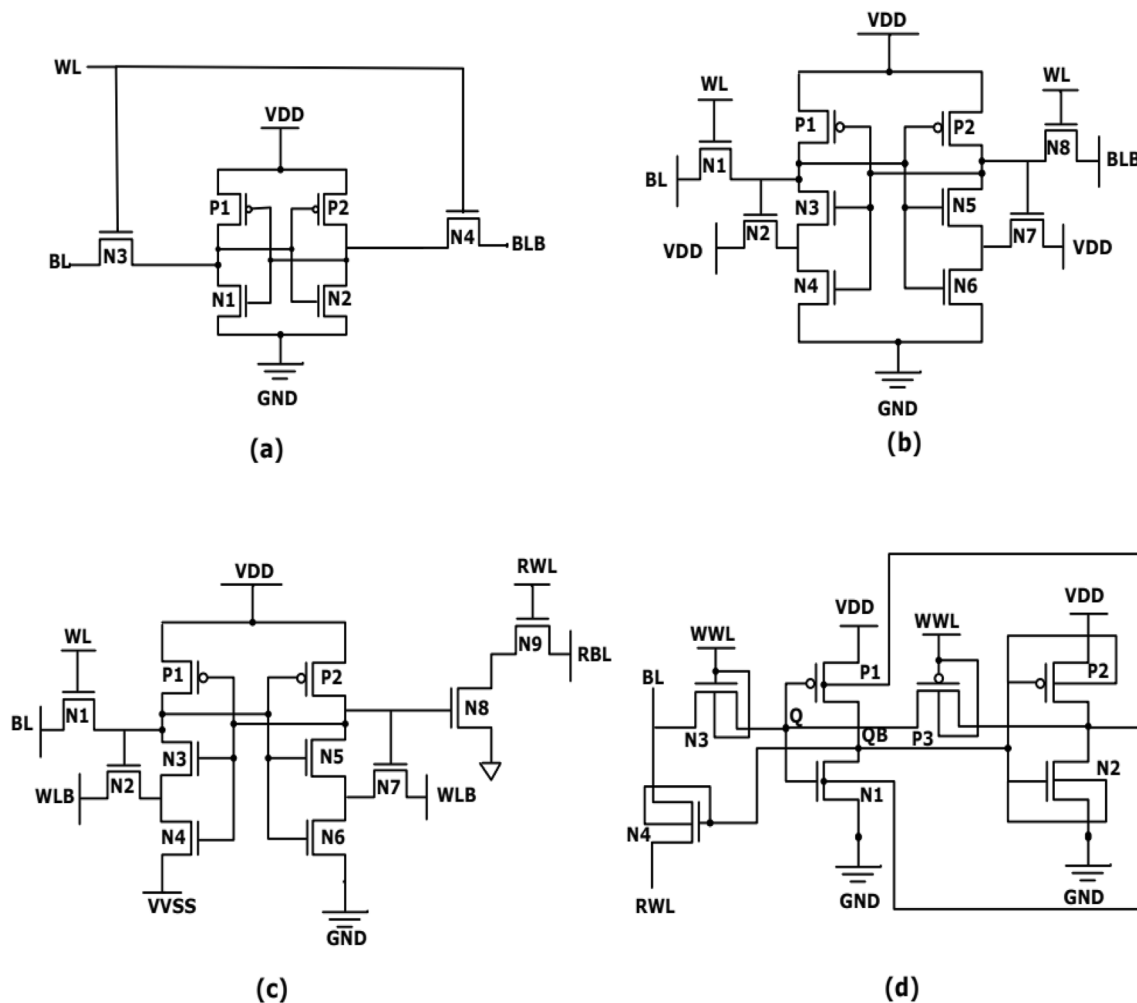


Fig. 1 Earlier reported SRAM cells **a** Conventional-6T SRAM, **b** ST-10T SRAM, **c** ST-11T SRAM, and **d** SE-7T SRAM cell

2.3 ST-11T SRAM cell

The ST-11T SRAM cell is depicted in Fig. 1c. In this cell, cross-coupled Schmitt trigger-based inverters along with a reading buffer are used [10]. Read stability is enhanced by the read buffer circuit, and hold stability is enhanced by schmitt trigger inverters. The write-1 ability is improved by row based floating VVSS scheme, but this improvement is not significant. Due to the increased number of transistors, this cell has a wide area. The write-1 operation is performed by only one cell and the remaining all perform the write-0 action. So, the write-0 cells can drive the VVSS. Hence, write-1 ability improvement is insignificant.

2.4 SE-7T SRAM cell

Figure 1d depicts the SE-7T SRAM cell. It uses an ST circuit with a built-in body bias feedback mechanism within the cell core [11]. RSNM is improved by a separate read path and minimizes read delay. Feedback cutting transistor is used to improve WSNM. But, the drawback of this circuit is write delay is increased, and also power consumption is more compared to other cells considered in the work. However, it shows better performance in terms of read and write energy.

3 Proposed ST-7T SRAM cell

The connection drawing of the Proposed ST-7T (PST7T) SRAM is depicted in Fig. 2 and its timing diagram is depicted in Fig. 3. The proposed design comprises a cross-connected standard inverter and schmitt trigger inverter and one NMOS access transistor. It has a row-based WL signal, and a column-based write word line (WWL). The source terminal of the ST inverter’s feedback transistor is connected with WWL.

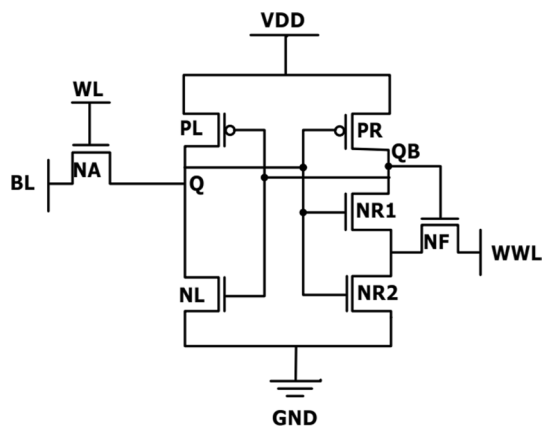


Fig. 2 Proposed ST-7T SRAM cell

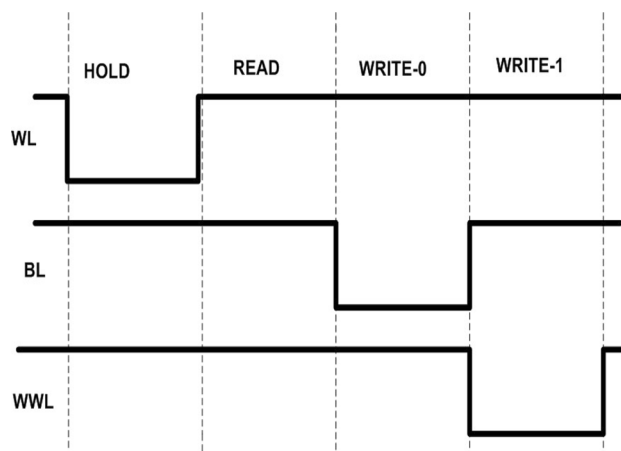


Fig. 3 Timing diagram of PST7T

3.1 Hold, read and write operation

In hold operation, WL is disabled and WWL is kept high and BL is pre-charged. Hence, the cross-connected standard and ST inverter pair is disconnected from the bit line, further hold capacity is improved due to the feedback structure. In read mode, BL is pre-charged, and WL is enabled. So, the access transistor turned ON. Consequently, the bit line may be discharged depending on the storage node Q. Generally, failure in reading occurs due to read disturbance from the bit line (BL). The PST7T circuit in the hold, read and write mode is depicted in Fig. 4a, b and c respectively. When read disturbance occurs at the storage node, its voltage overshoots the inverter trip voltage, and the storage node data can be inverted. But in the proposed design, we use an ST inverter and its trip voltage is high compared to the normal inverter. Hence, the data cannot be inverted. Therefore, the PST7T SRAM cell mitigates the problem of reading failure by the use of a cross-coupled ST inverter and standard inverter.

During the write operation, WL is activated to activate the access transistor. So, the data from BL can be transferred to the storage node. Based on data at BL the cell will write either write-0 or write-1. For the write-0 operation, WWL remains “1” and BL made “0” by the write driver. For the write-1 operation, BL made “1” by the write driver, and column-based WWL is changed to “0”. Hence, the feedback is removed from the ST inverter and its trip voltage becomes identical with respect to the normal inverter. The storage node Q is being pushed to “1” via the access transistor and the schmitt-trigger inverter output QB is now changed to “0”. Thereafter column-based WWL reset to “1” after QB is flipped. However, due to the weak drivability of the NMOS access transistor, there is no sufficient improvement in write ability. The negative VWW L technique is used to enhance the write-1 capacity of the PST7T design. When WWL is applied with negative voltage, the node Vx

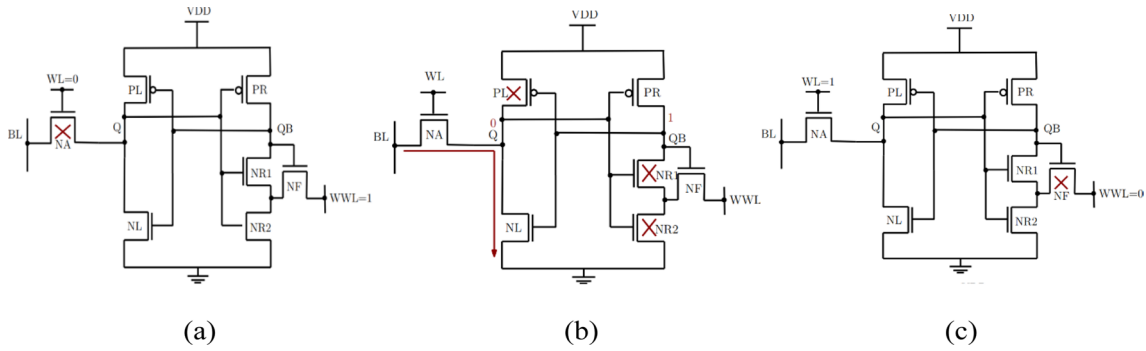


Fig. 4 Proposed ST-7T SRAM in a hold, b read and c write modes

immediately becomes negative due to the activated feedback transistor. The reduction in V_x can increase the robustness of PR1, which decreases the schmitt trigger inverter’s trip voltage. Thus, the write-1 operation becomes easy. During the write-1 operation when WWL made “0”, the feedback is removed and the trip voltage is minimized by 21.9%. When WWL is applied with a negative value of -0.2 V, the reduction in trip voltage is 52.4% percent. Therefore, the write-1 ability is significantly improved by the negative V_{WWL} assist technique.

3.2 Half-select stability

Due to the scale down of the technology, the disturbance in the data stored is raised throughout the write mode in half select SRAM cells, due to its word lines are energized. As an outcome, memory cells are written unintentionally [12]. During half-select, the SRAM cells must have been secured. Otherwise, during the write mode, the memory cell may lose the data. This half-select issue can cause multi-bit soft errors. Furthermore, the disturbance of heavy ions, alpha

particles, and protons is raised [13, 14]. To minimize bit errors error correction code (ECC) technique is needed in a memory cell, but conventional ECC techniques are not sufficient. A bit-interleaving architecture is needed to ignore multiple-bit errors. In bit-interleaving architecture, bits are arranged by providing column signals and words [15]. Based on WL and column-based WWL control signals, the desired cell can be selected in the PST-7T SRAM. Hence, the half-selection issue is solved in this manner.

The half-selected cell’s data must be stable during read and write operations. Hence, these cell’s hold stability must be taken into account in the design of SRAM [16]. The row half-selected cell’s hold stability in all modes must be ensured in order to use a bit-interleaving structure [20]. The row half-selected cells in read and write operations are disturbed by BL, which acts as selected cell in the read operation. In row of half-selected cells, there is no stability issue because the selected cell’s read stability is ensured sufficiently. Figure 5 illustrates the write-0 and write-1 mode column half -selected cells. As the NL and PL transistors are turned off in write-0 and write-1 modes respectively in

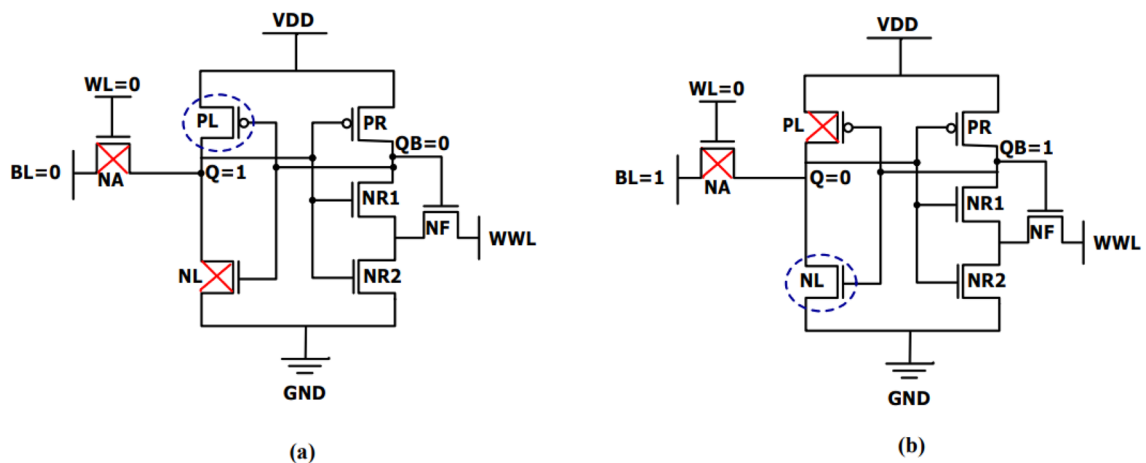


Fig. 5 Column half-selected cells in a write-0 and b write-1 operations

column half-selected cell, the storage node Q is stable, and the column half-selected cell’s hold stability is ensured. As an outcome, the proposed ST 7T SRAM cell’s, the hold stability is ensured in half-selected cells.

4 Simulation results analysis and comparison

In this section, comparative simulation results with existing SRAM cells are discussed using FinFET-18 nm technology. The performance parameters considered for the comparison are area, static noise margin, delay, power, energy, and leakage power. All the performance metrics of PST7T SRAM are analyzed at 27°C temperature and compared with SE-7T SRAM, ST-11T SRAM, ST-10T SRAM, and conventional-6T SRAM cells. Transistor sizing is the major task in maintaining read and write stabilities. The factors which affect the SRAM cell’s stability are attentively considered for design. Typically, the β ratio should be between 1.2 and 3 for better RSNM [17]. The γ ratio should be less than 1.2 for better WSNM [18]. The comparison of different features of SRAM cells, considered in this design is represented in Table 1.

4.1 Static noise margin

Figure 6 shows comparison results of HSNM, RSNM, and WSNM of proposed ST7T SRAM cell with conventional-6T, ST-10T, ST-11T, and SE-7T SRAM cells. The proposed cell achieves the HSNM of 329 mV at 0.6 V (Fig. 7). Figure 8 shows the butterfly diagram of 6T, SE-7T, and PST-7T SRAM cells in hold operation. The RSNM can be verified using butterfly curves of bit cell read operation as shown in Fig. 9. Due to BL being decoupled in read mode, the RSNM is almost equal to HSNM. The magnitude of SNM is indicated by the size of the square which can be suited into the butterfly plot [19]. As HSNM is high for ST-inverter SRAM read stability is improved. The write ability of PST7T SRAM is enhanced due to the negative V_{WVWL} technique. Hence the PST7T SRAM achieves 1.2× higher

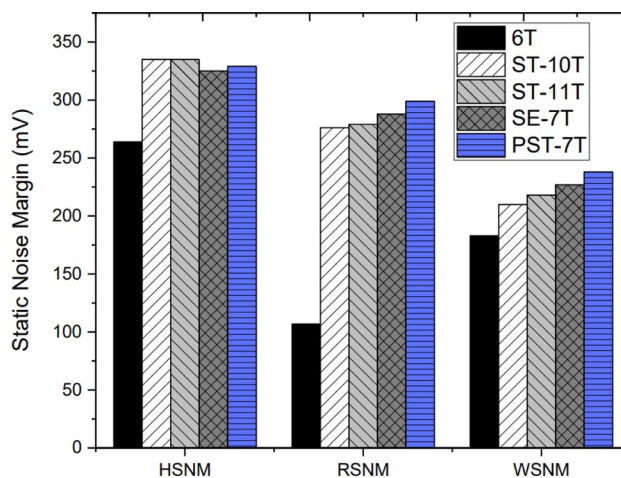


Fig. 6 Comparison of HSNM, RSNM, and WSNM of proposed ST-7T SRAM with previous SRAM cells

WSNM compared to the ST-11T SRAM cell, illustrated in Fig. 6. Variation of noise margin for different VDD values is also observed and it is illustrated in Fig. 7. Figure 7a illustrates the HSNM variation with respect to VDD, Fig. 7b illustrates the RSNM variation with respect to VDD, and Fig. 7c indicates the WSNM variation with respect to VDD.

4.2 Read and write delay

For differential circuits, read delay can be measured as the duration between the moment when WL is activated to the moment when the difference between BL and BLB is 50mV [20]. For single-ended circuits, read delay can be measured as the duration between the moment when WL is activated to the moment when BL is discharged to VDD-50mV. [21, 22]. Write delay can be defined as the duration between the moment when WL is activated to the moment when the data at the storage node reached 90% of VDD. Figure 10 shows the read delay comparison of PST7T SRAM with 6T, ST10T, ST11T, and SE7T SRAM cells at different process corners. Figure 11 illustrates the write delay comparison of PST7T SRAM with 6T, ST10T, ST11T, and SE7T

Table 1 Proposed ST-7T SRAM feature comparison

Cell feature	Traditional-6T [8]	ST-10T [9]	ST-11T [10]	SE-7T [11]	Proposed ST-7T
Bitlines	2	2	2	1	1
Control signals	1-Word line	1-Word line	1-Wordline + 1-RWL	1-RWL + 1 WWL	1-Word line + 1-WWL
Read/write	Differential	Differential	Differential	Single-ended	Single-ended
NMOS transistors in Read path	2	3	3	2	2
Half-selection resolved or not	No	Yes	Yes	Yes	Yes

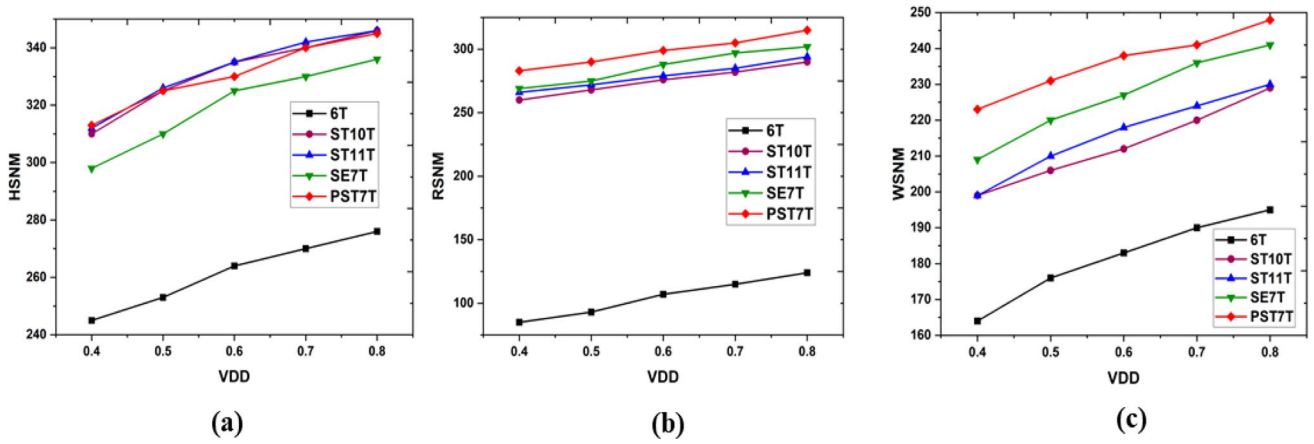


Fig. 7 Variation of noise margin with respect to VDD a HSNM variation with VDD, b RSNM variation with VDD, and c WSNM variation with VDD.

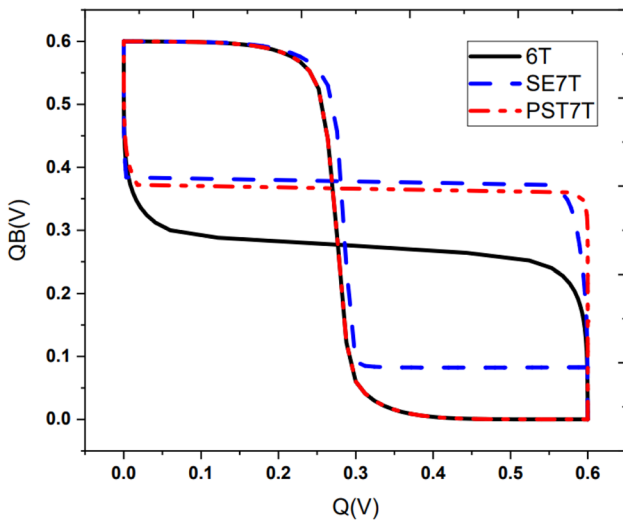


Fig. 8 Comparison of HSNM of proposed ST-7T SRAM with SE7T and conventional 6T SRAM cells

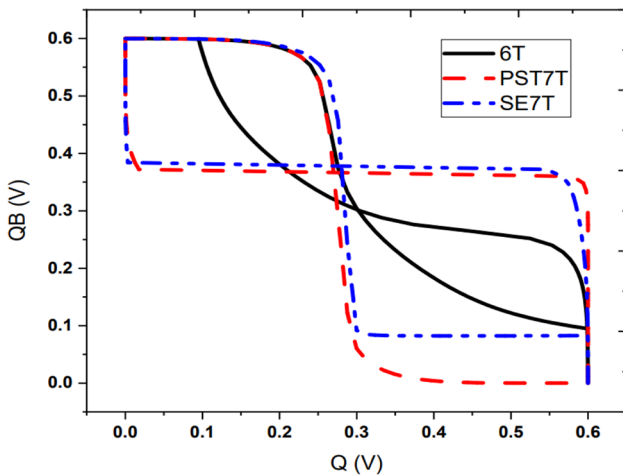


Fig. 9 Comparison of RSNM of proposed ST-7T SRAM with SE7T and conventional 6T SRAM cells

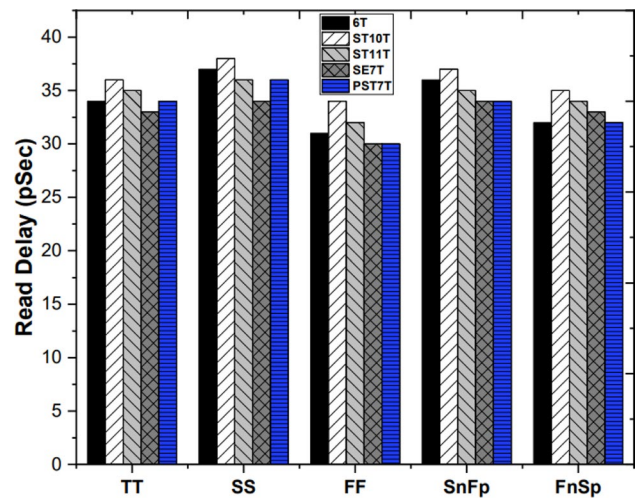


Fig. 10 Read delay comparison of PST7T SRAM cell at different process corners

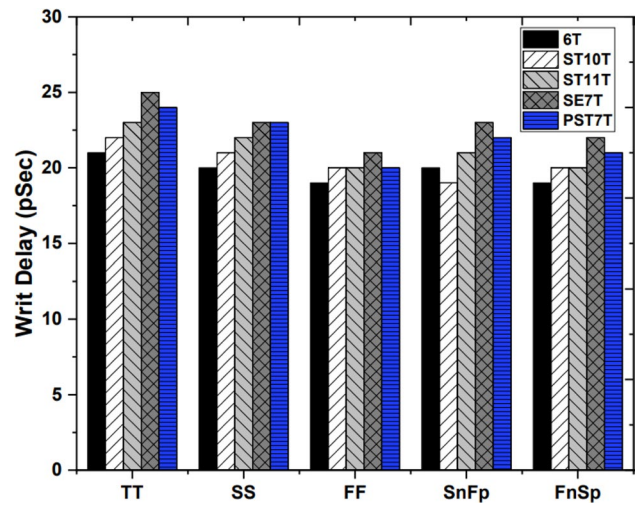


Fig. 11 Write delay comparison of PST7T SRAM cell at different process corners

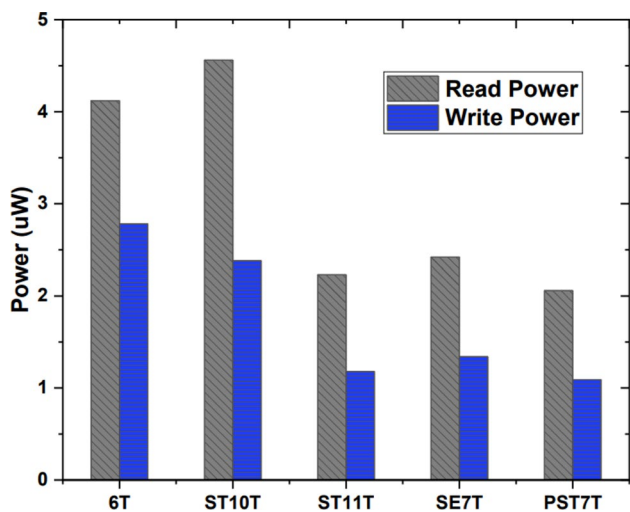


Fig. 12 Read and write power comparison of PST-7T SRAM cell

SRAM cells at different process corners. In the proposed cell write delay is longer compared to other differential bit line structures, because of the single-bit line write operation. Therefore ST-11T and ST-10T cells have less delay. But, the write delay of PST7T SRAM cell is less compared to SE7T SRAM cell. The proposed ST-7T cell at TT (typical-typical) process corner, has a read delay of 34ps and write delay of 24ps.

4.3 Read and write power

In single-bit line architectures, power utilization is diminished because of the low switching activity of BL [23]. The discharging and charging of the bit line take less power, compared to differential bit line structures [24, 25]. Hence the read and write power utilization of PST-7T SRAM cell is less than ST-11T SRAM and ST-10T SRAM cells as it uses a single bit line and also less compared to SE-7T SRAM cell. The write power of conventional-6T SRAM is maximum among all other cells. In PST-7T SRAM cell, write power is lowered by 39.27% compared to conventional-6T SRAM cell. Moreover, the read power of ST-10T and ST-11T SRAM cells is high due to more transistor count in the reading path. The read power of PST-7T SRAM is diminished by 49.96% compared to traditional-6T SRAM. The comparison of read and write power consumption of PST7T SRAM with previous SRAM cells is depicted in Fig. 12. Monte Carlo simulations are performed for 500 samples to observe the read-and-write power distribution plots, mean and standard deviation which are shown in Figs. 13 and 14.

4.4 Read and write energy

The comparison results of write energy consumption of PST7T SRAM with conventional-6T SRAM, ST-10T SRAM, ST-11T SRAM, and SE-7T SRAM is shown in

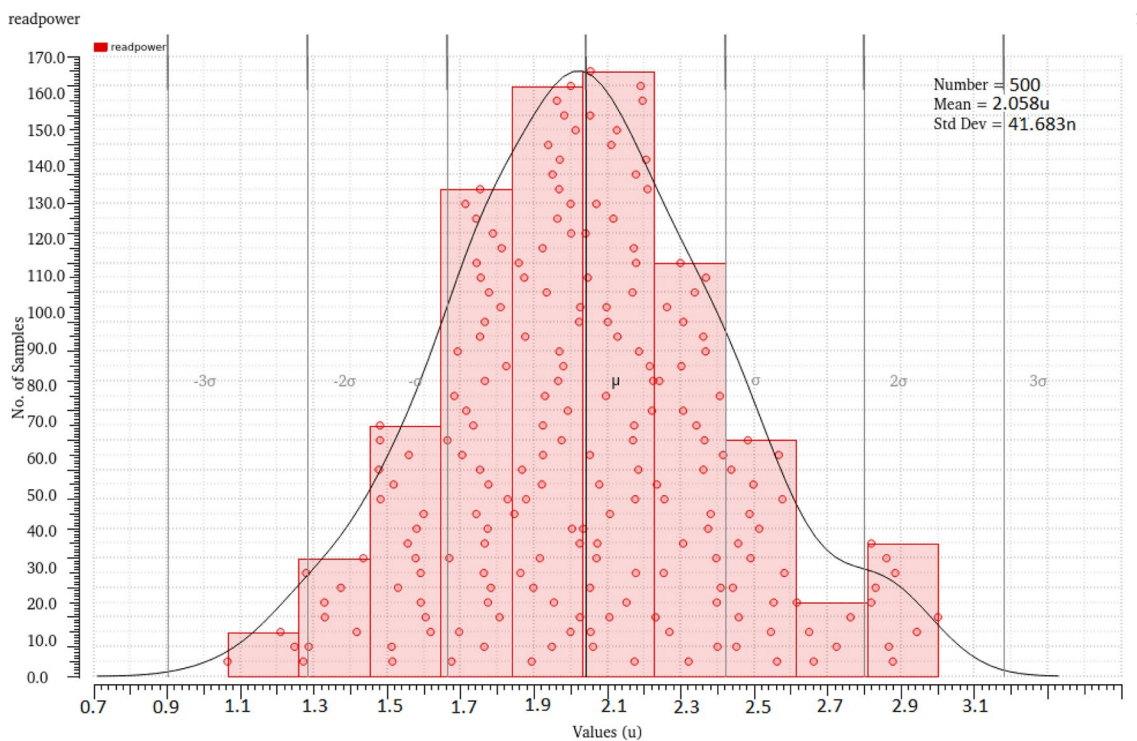


Fig. 13 Read power distribution of PST-7T SRAM cell

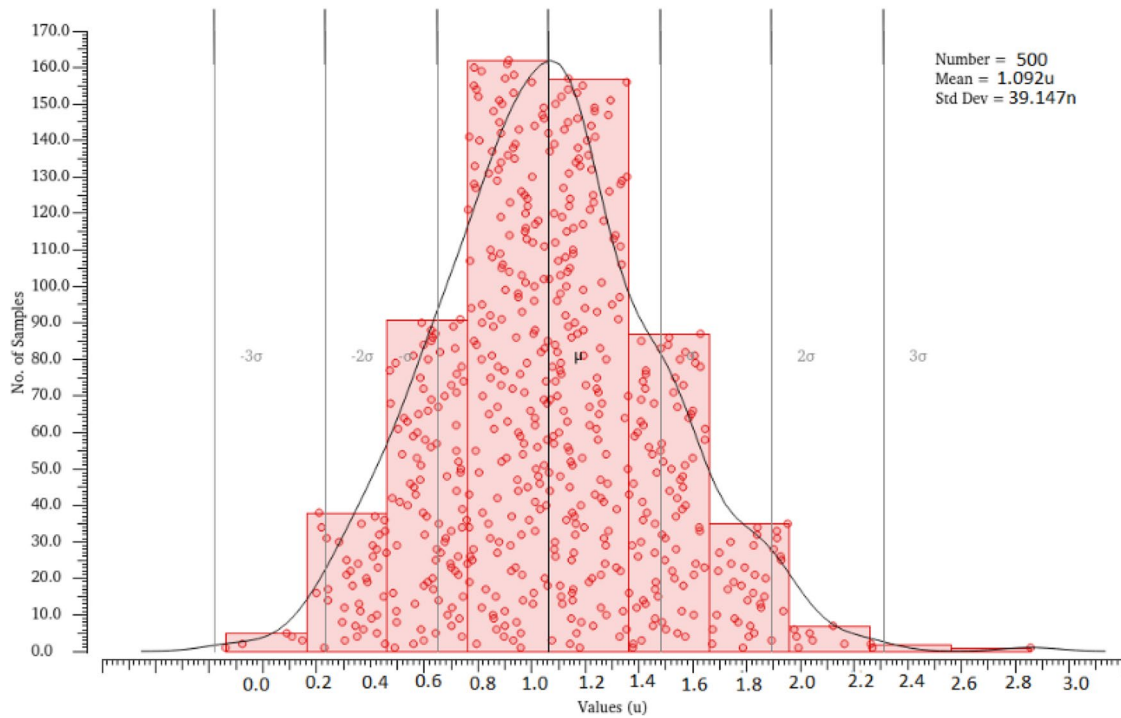


Fig. 14 Write power distribution of PST-7T SRAM cell

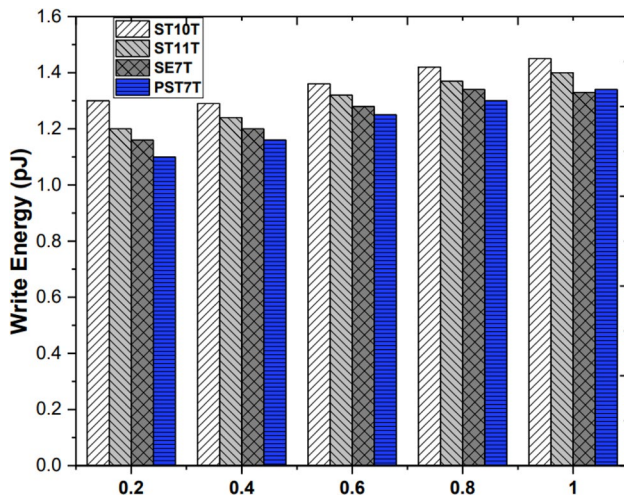


Fig. 15 Write energy comparison of PST7T SRAM cell at different power supply

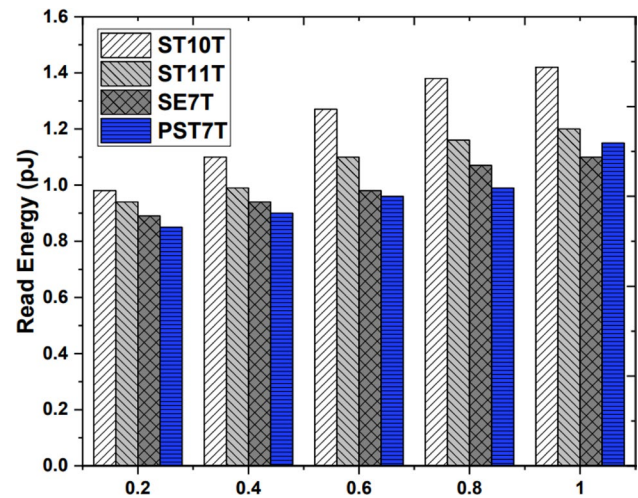


Fig. 16 Read energy comparison of PST7T SRAM cell at different power supply

Fig. 15. Write energy consumption is mainly because of column-based signals [26, 27]. In ST11T SRAM column-based shared VVSS signal toggles a large capacitance which leads to consuming less energy [10]. In PST7T SRAM cell, WL is a row-based control signal and WWL is a column-based control signal. Thus, it is the second least compared to other SRAMs. Hence write assist technique is used to reduce the energy utilization in write mode. Write energy

utilization is minimized by 14.87% compared to SE-7T SRAM cell. Figure 16 illustrates the comparison of reading energy utilization of PST-7T SRAM with ST-11T, ST-10T, and SE-7T SRAM cells. Compared to all, 6T and ST-10T SRAM has the maximum reading energy utilization due to raised capacitance in differential sensing. The read energy of PST7T SRAM cell is lowered by 14.19% compared to SE-7T SRAM cell.

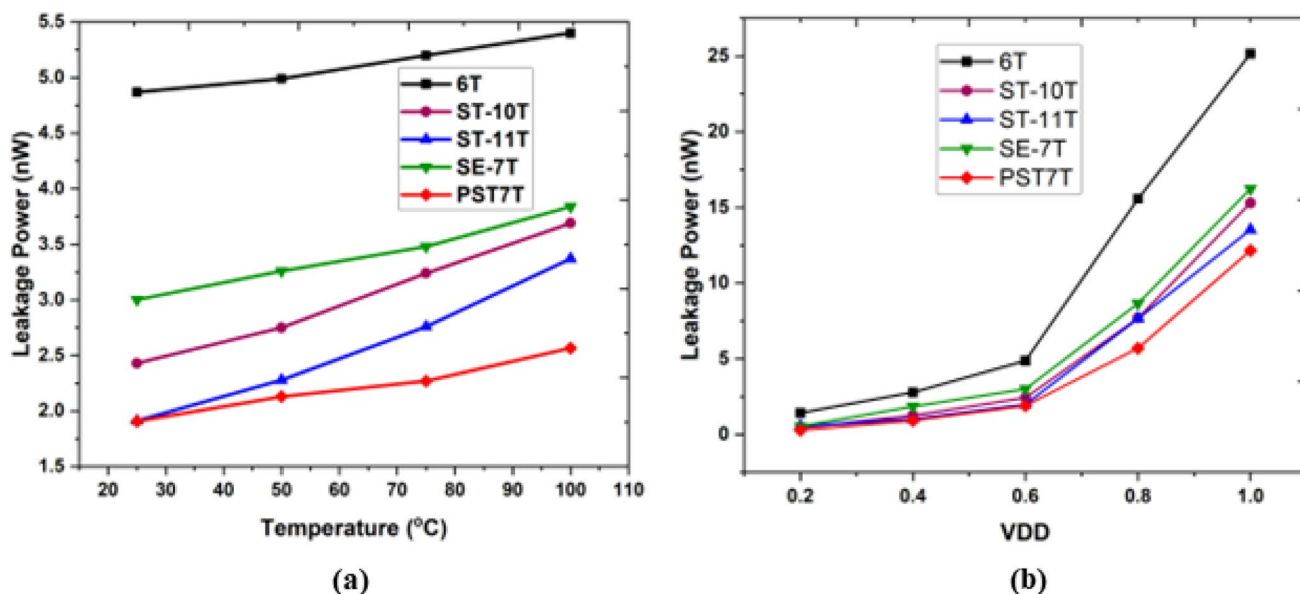


Fig. 17 Leakage power comparison of PST7T SRAM cell a At different temperatures, b For different VDD values

4.5 Leakage Power

Figure 17 shows the comparison of leakage power of PST-7T SRAM. Figure 17a indicates leakage comparison at various temperatures, and Fig. 17b indicates leakage comparison for different VDD values. The proposed ST-7T SRAM cell utilizes less leakage power because all leakage paths are removed during HOLD operation from BL and VDD to the ground [28, 29]. It is clear from the results that, the PST7T SRAM achieves low leakage power. The leakage power utilization of PST-7T SRAM is 39.17%, 14.35%, 13.23%, and 15.72% less than conventional-6T SRAM, ST-10T SRAM, ST-11T SRAM, and SE-7T SRAM cells respectively. Montecarlo simulations are performed for 500 samples to observe the leakage distribution plot, mean and standard deviation which are shown in Fig. 18. The leakage power variation at different technology node is also observed and it is depicted in Table 2.

Table 2 Leakage power comparison at different technology node

Technology	Leakage power				
	6T	ST10T	ST11T	SE7T	PST7T
45 nm	18.092 pW	13.438 pW	11.17 pW	12.251 pW	8.025 pW
32 nm	1.136 nW	0.229 nW	0.253 nW	0.694 nW	0.137 nW
18 nm	4.87 nW	2.83 nW	1.978 nW	3.001 nW	1.908 nW
16 nm	7.682 nW	4.967 nW	2.731 nW	5.376 nW	2.546 nW

4.6 Write assist technique

In ST10T and ST11T SRAM cells boosted V_{WL} technique is used to improve the write ability. Because of NMOS’s weak drivability in write-1 operation, the proposed design must use the write-1 assist technique. ST10T SRAM cell uses boosted V_{WL} and negative V_{BL} write assist techniques. Whereas, the negative V_{WWL} technique depicted in Fig. 19 is used in the proposed ST7T SRAM cell. In the write-1 operation when WWL made “0”, the feedback is removed and the trip voltage is reduced by 21.9%. When WWL is applied with a negative value of -0.2 V, the reduction in trip voltage is 52.4% percent. Therefore, the write-1 ability is significantly improved by the negative V_{WWL} assist technique.

4.7 Cell area

The layouts of PST-7T SRAM and earlier reported SRAM cells are depicted in Fig. 20. From this layout comparison we observe that the PST-7T SRAM cell has 1.40× area overhead compared to conventional-6T SRAM. The comparative result of PST-7T SRAM with existing SRAM cells is shown in Fig. 21. Because of less transistor count, the area of PST7T SRAM is small. The proposed SRAM cell showed an overhead in area of 1.4× compared to traditional-6T SRAM cell, but 37% and 41% smaller area compared to ST-10T and ST-11T SRAM cells.

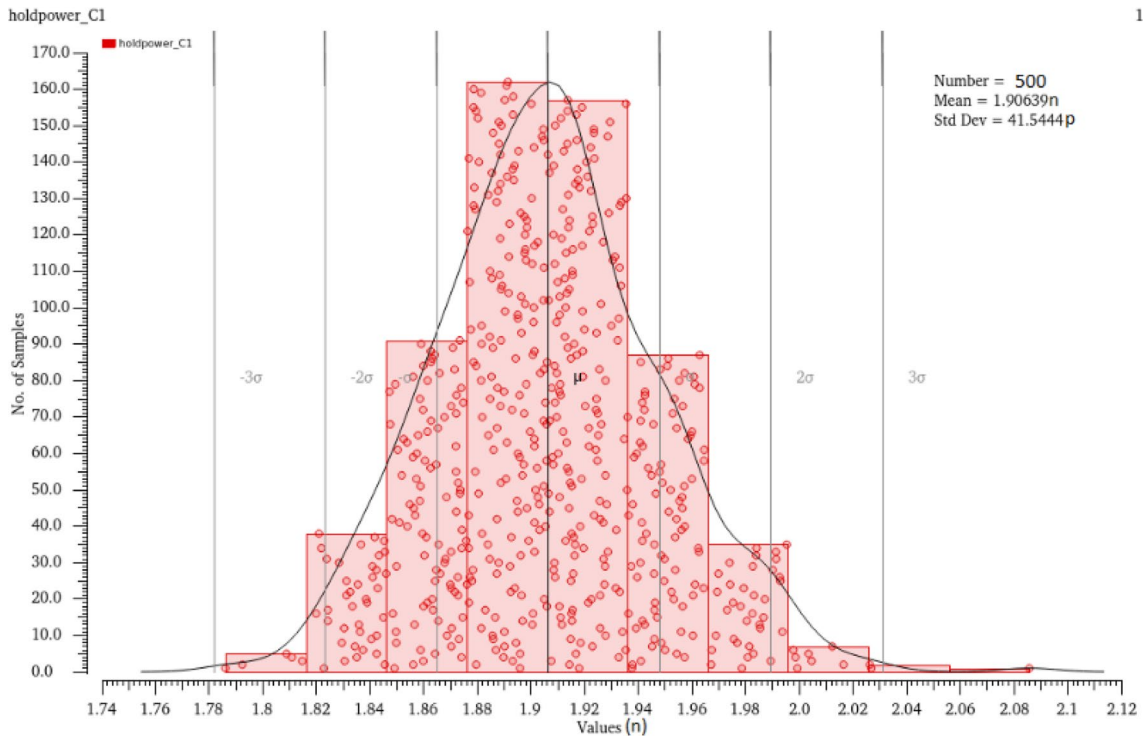


Fig. 18 Leakage power distribution of PST7T SRAM cell

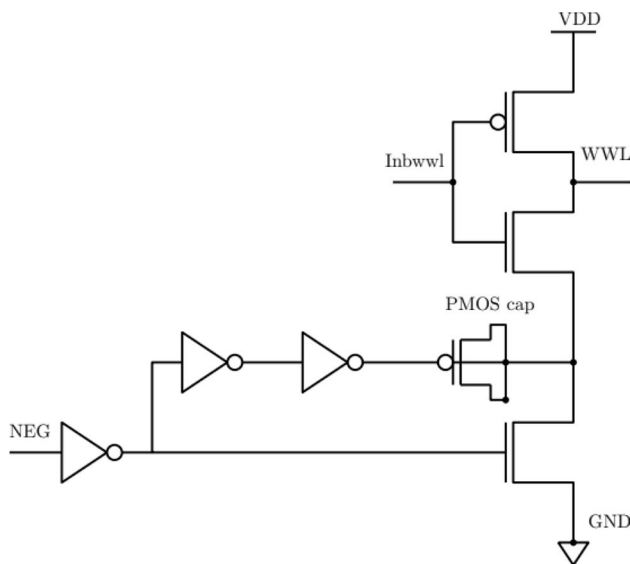


Fig. 19 Negative V_{WWL} technique

4.8 Electric quality metric

The performance of an SRAM cell can be measured using the electric quality metric (EQM) [30], shown in Eq. (1).

$$EQM = \frac{RSNM \times HSNM \times WSNM}{P_{leak} \times T_{RA} \times P_{read} \times P_{write} \times Area} \tag{1}$$

Where, RSNM is the read static noise margin, HSNM means hold static noise margin, WSNM is the write static noise margin in mV, P_{leak} is the leakage power, P_{read} denotes the read power, P_{write} denotes the write power in μW , T_{RA} indicates the read delay is in ns, and the area is in $(\mu m)^2$.

Figure 22 represents the comparison of EQM of PST7T SRAM with previous SRAM cells considered for this work. The metric of the PST7T SRAM cell is enhanced by 73.62%, 18.53%, 16.65%, and 12.24% comparing to traditional-6T, ST-10T, ST-11T, and SE-7T SRAM cells respectively. From Table 3, it can be observed that the PST7T SRAM cell works better in parameters when compared to other considered cells in the design.

5 Conclusion

This paper discusses a new single-sided schmitt-trigger 7T-SRAM, to mitigate energy utilization and to operate SRAM in the near-threshold region. The proposed design significantly improved read and write stability in the

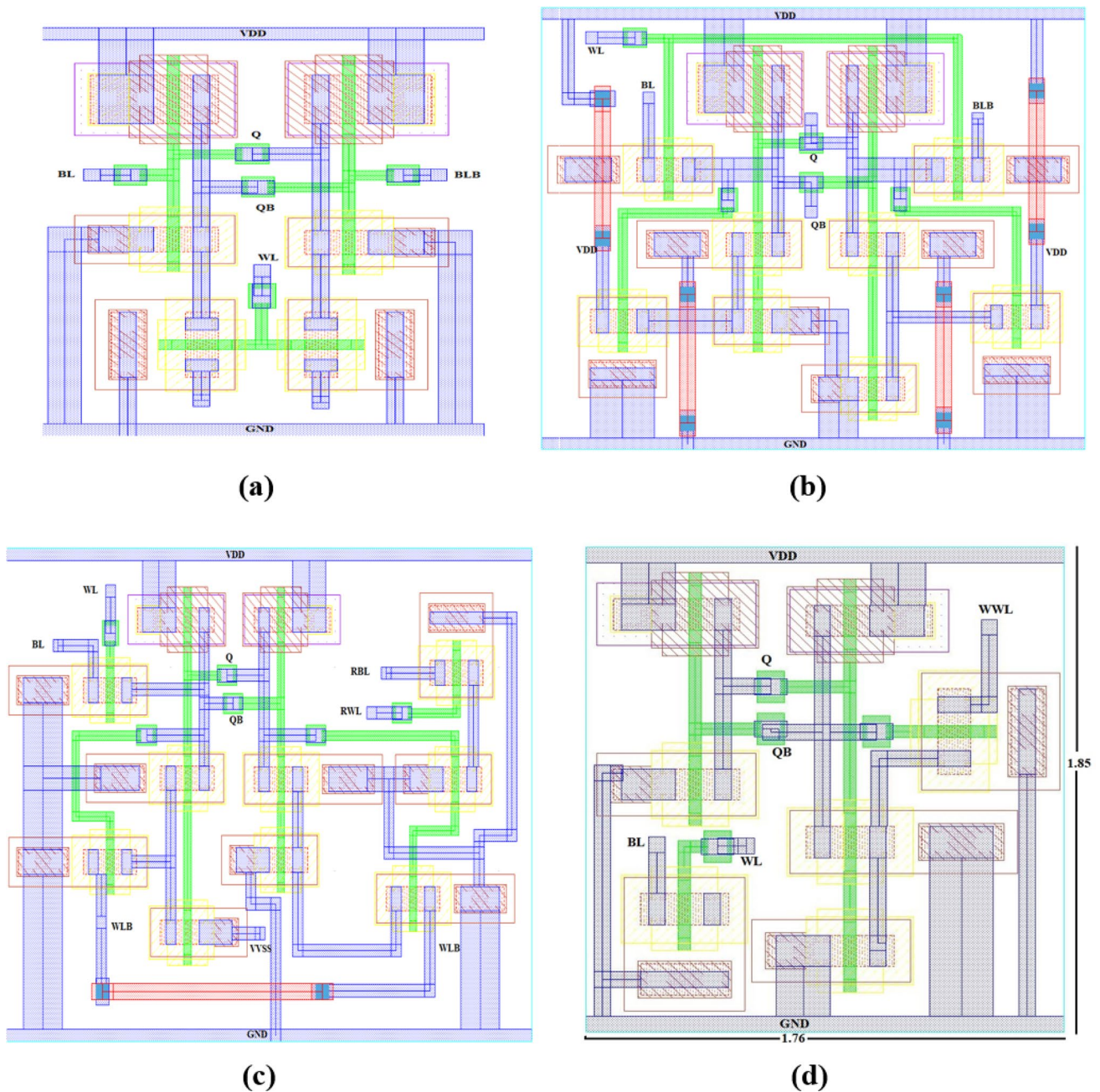


Fig. 20 Layouts of proposed and earlier reported SRAM cells **a** 6T SRAM, **b** ST10T SRAM, **c** ST11T SRAM, and **d** PST7T SRAM

near-threshold region. The proposed design is analyzed for energy, power, stability, delay, and area. Read stability was improved by using the cross-connected standard inverter and ST inverter. The write ability was improved by using the negative V_{WWL} write assist scheme, which can control

the ST inverter trip voltage. The PST7T SRAM utilizes low power compared to ST-10T SRAM and ST-11T SRAM. The RSNM and WSNM also improved by 66.28% and 18.97% compared to conventional-6T SRAM. The write energy and read energy utilization also lowered by 14.87% and 14.19%

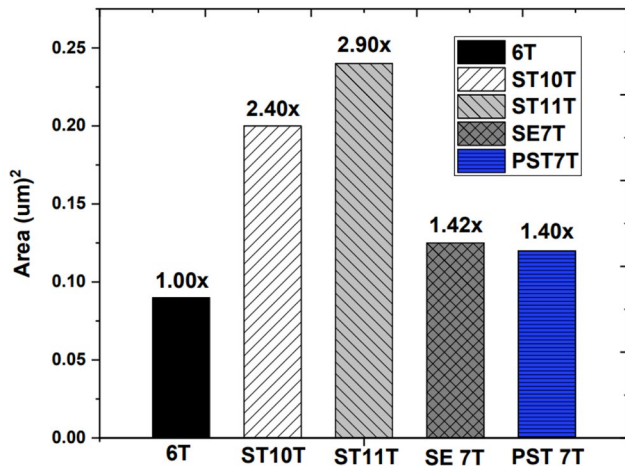


Fig. 21 Area comparison

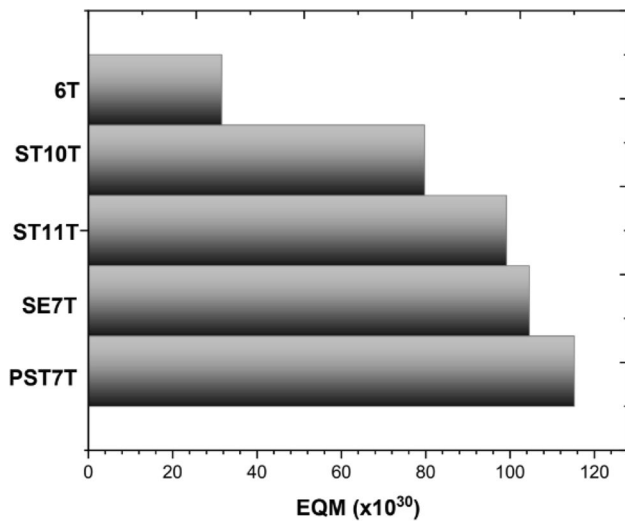


Fig. 22 Electric quality metric comparison of PST-7T SRAM cell

compared to ST10T and ST11T SRAM cells respectively. In addition, from all simulation results, it is observed that PST-7T SRAM cell exhibits better operation in terms of stability, speed, and power. Hence it is a good choice for low-power applications.

Table 3 Comparison of various performance parameters of PST7T SRAM with other SRAM cells

Name of cell	HSNM (mV)	RSNM (mV)	WSNM (mV)	Leakage power (nW)	Read power (uW)	Write power (uW)	Read delay (nS)	Write delay (nS)
Conventional-6T	264	107	183	4.87	4.12	2.78	34	21
ST-10T SRAM	335	276	210	2.43	4.56	2.38	36	22
ST-11T SRAM	335	279	218	1.978	2.23	1.18	35	23
SE-7T SRAM	325	288	227	3.001	2.42	1.34	33	25
PST-7T SRAM	329	299	238	1.908	2.058	1.09	34	24

Author contributions APK Conceptualization, methodology, simulation; RL Investigation, reviewing and editing, overall correction.

Data availability The authors confirm that the data supporting the findings of this study are available within the article or below mentioned references.

Declarations

Conflict of interest The authors declared there is no conflict of interest in this work.

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