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A low power single bit-line configuration dependent 7T SRAM bit cell with process-variation-tolerant enhanced read performance

Bhawna Rawat[1] · **Poornima Mittal**[1]

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Abstract
Cache memory is a key component for most microprocessors in embedded system. The increasing processing load has resulted in an upsurge in the demand for low power, high performance SRAM bit cells. Consequently, in this paper a 7T bit cell is designed for feature size 32 nm and 300 mV supply voltage. The improvement in the performance of the proposed cell is validated against the results obtained for pre-existing 6T, 7T, 8T, 9T, and 10T cells. The read and hold noise margin for the cell is obtained to be 96 and 68 mV respectively, whereas the static margin for the write operation is 170 mV. To perform a successful write operation, a pulse-width of 30 ns is utilized. The power analysis reveals that the proposed cell has minimal read/write power consumption. The leakage power for the cell is 8.4 pW and 1.2 pW for Q = '0' and '1' respectively. Tolerance analysis justifies that the cell maintains its functionality and yields credible outputs under process-voltage-temperature variations for static performance metrics. The layout for the proposed 7T cell occupies 0.584 μm^2 area. This is 5.55% smaller than a single ended 6T. The area for other 7T counterparts, 8T, 9T, and 10T cells is larger than the proposed cell.

Keywords Low voltage · Single port · Leakage power · Write margin · Layout analysis

1 Introduction

The increase in demand for round the clock digital connectivity, and the explosion of everyday personal data has increased the processing demand for embedded systems. A major component of efficient embedded system is Static Random Access Memory (SRAM); formed by bit cells organized in an array. The bit cell stores the data, whereas reading and writing into the cell is facilitated by peripheral circuitry; it is composed of decoders, bit-lines, and sense amplifiers [1]. The memory core along with the peripheral circuit consumes about 30% of the total power for the system and 50% chip area [2, 3]. Two factors—static and dynamic, combine to form the total power consumed by an SRAM cell. Static power has a linear dependence on supply voltage (V_{DD}), whereas, the latter has a quadratic dependence on V_{DD} [4]. The increasing demand for portable devices with longer battery life has made power consumption reduction a key design objective. The most trivial method to lower power consumption is to lower the operational V_{DD} for the cell [5]. But this is limited by the variations caused by process-voltage-temperature (PVT) in the nanometer vicinity [6]. Also, the declining trends for V_{DD} have resulted in standby power dominating dynamic power [7]. Reduction in V_{DD} also limits the speed of operation [8]. As V_{DD} decreases, the V_{DD}–V_{TH} factor diminishes. Thereby diminishing the operational frequency for the bit cell [9]. Therefore, the power consumption per instruction increase, even though the total power consumed by the cell decreases [10]. Consequently, hampering the overall performance for the SRAM based memory. Other reasons that result in the degradation of performance include—drain induced barrier lower (DIBL), geometry defects, electro migration, oxide breakdown, hot carrier injection, and electrostatic discharge [11–13]. Thus, designing a digital circuit operational at low levels of V_{DD} is a mammoth task for designers [14].

Another aspect that limits the performance of SRAM is the slow-fast corner; here if an NMOS and PMOS transistors are equally sized the performance for the CMOS circuit is skewed. This is caused by vast gap between the mobility for the NMOS and PMOS transistors, which

✉ Poornima Mittal
poornimamittal@dtu.ac.in

Bhawna Rawat
bhawnarawat12@gmail.com

[1] Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India

gets extenuated because of the skewed corner. The collective influence of the aforementioned factors increases the vulnerability [15] of the cell towards read, write, and access time failures. Besides, embedded cache memories with larger area are more prone to such failures [16]. In this paper a seven-transistor (7T) cell based on a single bit-line architecture is proposed. The presence of a single bit-line abets in limiting the dynamic power consumed by the cell. Another reason for choice of single ended configuration over differential ended cell is its ability to withstand reduction in V_{DD} [17, 18]. It also provides the added advantage of reduced silicon overhead, thereby increasing its economic feasibility.

In this paper, different SRAM bit cells are designed at 32 nm technology node to analyze the performance of the bit cell to identify their shortcomings. The learning of that are then utilized to design a modified 7T SRAM bit cell with improved performance. Along with this introduction section, the paper is organized into the following ten sections. Section II gives a schematic review of existing SRAM bit cells. Further, Section III defines the architecture and modes of operation for the proposed 7T cell. In Section IV, the simulation results for static analysis are presented and in section V, the cell ratio analysis is detailed. Further, in section VI the dynamic write ability is elaborated, while the power analysis is given in section VII. Section VIII justifies the tolerance analysis for the cell. The layout and area comparison of the bit cells are detailed in section IX. Finally, Section X recapitulates the findings of the paper.

2 Review of pre-existing bit cells in literature

Diverse architectures for SRAM cell are reported in literature to accomplish different design objectives—low area footprint, operational at low V_{DD}, reduced power consumption, faster operation, and high bit density. Figure 1 illustrates the circuit diagram for SRAM cells that were reported in the previous decade for different applications. The conventional SRAM cell is a six transistor (6TC) bit cell, as depicted in Fig. 1(a). Mutually connected inverter pairs (PUL-PDL & PUR-PDR) form the data core of the cell. The contents of the memory are retrieved using NMOS access transistors (ACL & ACR). Its speedy operation along with smaller area footprint make it the "de facto" model for implementation. However, the declining values for V_{DD} and shrinking technology node have made implementing 6TC cell fairly difficult. At lower technology nodes, the high leakage current increases the static power consumed by cell [19, 20]. The performance of conventional 6T cell suffers majorly because of the inherent read–write conflict in the cell. Also, due to common control signal for the read and write operation, it is also prone to half select disturbance, majorly causing a miswriting operation in the half selected cell. Also, due to V_{DD} scaling, the impact of process, voltage and temperature variations on the read and write operation becomes dominant.

For SRAM memory, maximum power is consumed during charging and discharging of bit-lines [17]. To reduce the discharging event, a single ended, dual port 6T (6TS) cell was described in 2019 [21]. The transistor based diagram

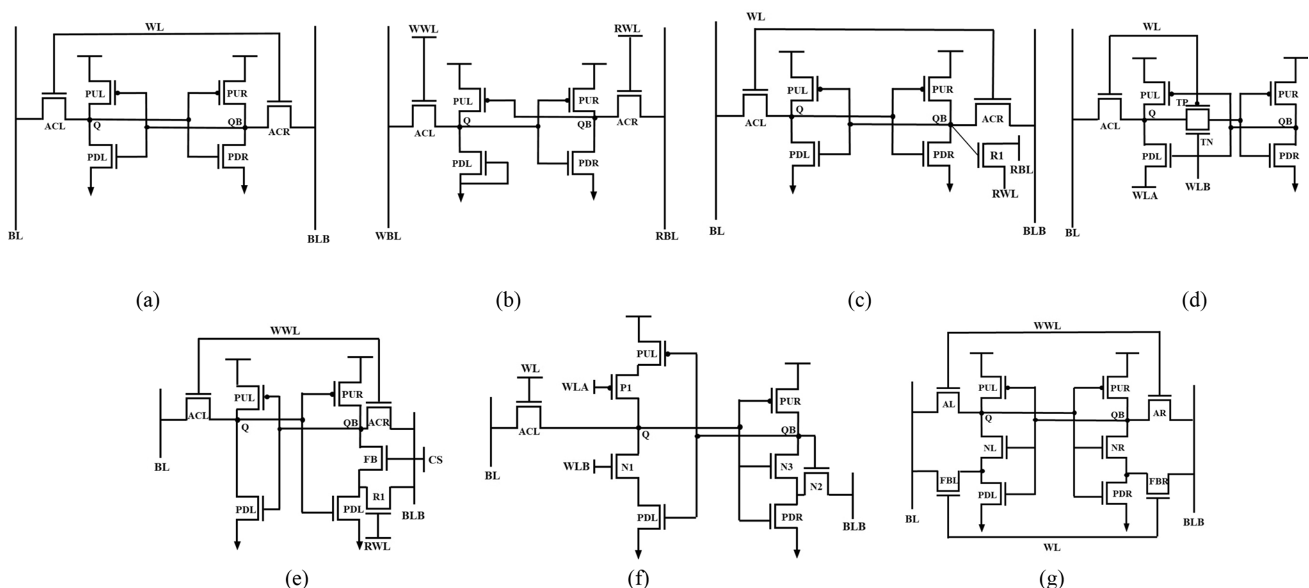


Fig. 1 Transistor based Circuit diagram for **a** 6TC, **b** 6TS, **c** 7TL, **d** 7TY, **e** 8TS, **f** 9TC, and **g** 10TK SRAM bit cells

for the cell is presented in Fig. 1(b). The memory element in 6TS consists of an inverter pair (PUR-PDR). The second inverter (PUL-PDL), is modified such that the gate and source for PDL are shorted to ground, thus it always operates in cutoff region. But, this degrade the Q = '0' margin, so a low V_{TH} transistor (LVT) is used to restore its performance. NMOS transistors (ACR & ACL) are used to access the contents of the data during the read/write operations. But in doing so, the number of control signals have increased leading to an increment in the overall capacitance of the memory. As bit cells are joined to form an array that acts as the memory core for the cache memory, a small increment in the capacitance for a bit cell has a multi-fold impact on the capacitance of the entire column. This results in increase in dynamic power for the memory and also increases designing complexity for the sense amplifier (and other peripheral circuitry). Increment in capacitance of the bit cell also deteriorates its dynamic write ability. Consequently, this has a radical effect on the dynamic performance and power consumed by the bit cell. This cell though outperforms the 6TC bit cell in terms of leakage, the overall energy consumption and area for the embedded memory is quite large.

Another method to uplift the performance of an SRAM cell is to combine 6TC cell with an independent read port to isolate the read and write operation. A similar 7T bit cell architecture (7TL) was reported by researchers in 2017 [22]. The circuit schematic for the same is illustrated in Fig. 1(c). An additional NMOS transistor (R1) is used to perform the read function; R1 is controlled by node QB. Read bit-line (RBL) via R1 to read word-line (RWL) form the read discharge path for the cell. As the gate of R1 is connected to the QB node of the memory core, it conducts only when Q = '0'. Thus reducing the read activity factor for the bit cell to 0.5. The only shortcoming for this cell is that the additional read port reduces the write drive current for the cell thereby resulting in a poor write performance.

Yet another 7T (7TY) cell configuration was suggested in 2016 [23]. The schematic for the same is depicted in Fig. 1(d). 7TY has a single-ended, single port architecture. Transmission gate (TN-TP) is used for disconnecting the feedback between the inverter pair. The cell is accessed via NMOS transistor (ACL). Four control signals are used to navigate the bit cell according to its modes of operation. These control signals are, WL, WLA, WLB and BL. But, its dual pulse based write operation reduces the speed for the bit cell. Also, the increased count of control signals; WLA and WLB results in additional peripheral circuitry for the bit cell. Consequently, having a substantial increase in the layout footprint and power consumption for the memory array.

A stable and low voltage enabled SRAM bit cell was reported in 2017 [24]. The bit cell is formed by eight transistors (8TS) and relies on a single bit-line enabled read and a dual bit-line enabled write operation. An NMOS transistor (FB) is used to disconnect the V_{DD} from ground rails; this is done to boost the single ended read stability for the cell. The transistor based diagram of the 8TS is presented in Fig. 1(e). The stacked transistor configuration also aids in reducing the leakage current for the cell. This cell has reported an improved performance but for its efficient working relies on an XOR gate common to a row. A dedicated XOR gates for each row has multifold impact on the area footprint and the overall power consumption for the memory array.

A 9T (9TC) single ended SRAM bit cell using Schmitt Trigger (ST) based inverter was reported in 2020 [25]. ST based inverter has the ability to manipulate its switching voltage subject to the direction of input transition [26]. The circuit diagram for the 9TC is illustrated in Fig. 1(f). The data storage in the cell is facilitated by a stacked inverter (PUL-P1- N1-PDL), plus a ST inverter (PUR-N2-PDL). The word-line (WL) control signal is used to access the data storage node for the bit cell. While the signal WLA and WLB are used to control P1 and N1 respectively. The WLA/WLB signals for the read and write operation are 0/1 and 1/1 respectively.

Another ST based cell was described by Kulkarni and Roy in 2012 [27]. This cell was an improved version of the cell described in 2007 [28]. This cell has a ten transistor (10TK) structure and the circuit schematic for the same is presented in Fig. 1(g). The write-word-line (WWL) control signal is used to access the data core formed by mutually connected ST inverter pair (PUL-NL-PDL & PUR-NR-PDR). While, the WL signal controls the feedback for the bit cell. This cell has an improved hold stability but due to its differential read operation the read stability for the cell suffers. While, the increased transistor count increases the power consumed by the cell [29]. Moreover, the increased area footprint makes the cell less economically efficient. A major limitation of various bit cells is that they often concentrate on enhancing only one of the performance parameters. And, usually the improvement in one comes at the cost of another. But it is imperative to design and propose a bit cell that balances the performance for all modes of operations simultaneously. The aforementioned cell are used to validating the performance of the proposed bit.

It can be concluded from the aforementioned review that the performance for SRAM bit cell has suffered drastically due to technology node scaling and supply voltage reduction. The 6TC cell is unable to perform for lower technology node due to the inherent read–write conflict, so the 6TS cell was reported. It eliminated the inherent read–write conflict, but resulted in high power requirement, thereby making it unfit for low power application. Consequently, the 7TL cell was reported to isolate the read and write port, while maintaining a low operational voltage requirement. To lower the power consumption for the bit cell, a single ended, single port cell—7TY was reported. But, it is dependent on two

additional control signals thereby increasing the interconnect load for the circuit. Increase in control signal count also increases the effective capacitance for the memory, thereby, increasing delay in the circuit. Another bit cell that resolves the read–write conflict is the 8TS cell. But, it leads to floating condition in the circuit, thereby increasing its vulnerability to error. While, to limit the power consumption for the bit cell, 9TC and 10TK cell were reported with Schmitt Trigger topology to improve the performance of the bit cell. But the area penalty for the 9 T and 10 T SRAM bit cell is extremely high, thus making them economically unfeasible. This mandates the requirement for an SRAM bit cell that efficiently resolves the read–write conflict; it operates at low values of supply voltage, and has lower layout area.

3 Proposed structure

The proposed SRAM is a seven transistor (7TP) bit cell that utilizes a single bit-line configuration. The data core of the cell comprises of mutually connected inverter pairs; inv1 (PUL-PDL) and inv2 (PUR-PDR). Unlike a conventional 6TC which relies on the mutual feedback connection between inverter pair, the 7TP SRAM bit cell disconnects the feedback via an additional LVT NMOS transistor (FB). NMOS transistors (WA and RA) facilitate the read/write operations for the cell. The transistor based circuit for 7TP cell is shown in Fig. 2. The read and write functions are controlled by signal read-line (RL) and word-line (WL) respectively. The operating conditions of the three control signals; W, WL, and RL are given in Table 1.

3.1 Hold operation

Throughout the hold operation, the effective functioning of the cell is limited to the coupled inverter pair. To maintain the cross coupled connection the feedback NMOS transistor (FB) is in conducting state for the entire duration of the hold operation.

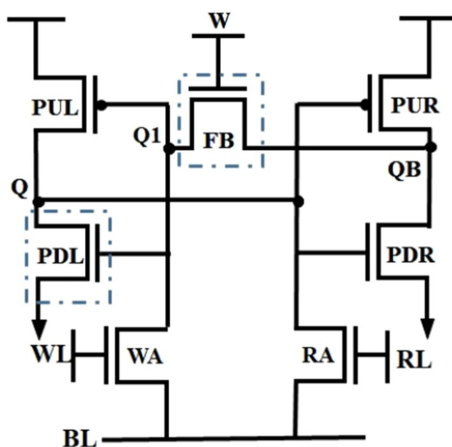


Fig. 2 The transistor based circuit diagram of the 7TP bit cell

3.2 Read operation

The 7TP cell relies on RA, controlled by RL, for the read operation. To additionally reduce the read vulnerability, the cell relies only on inv2 (PUR-PDR) for read operation. Thus, when the bit cell stores Q = ‘1’, there is no discharge path for the bit line. This is an important aspect of the bit cell, as it reduces the activity factor for 7TP cell from 1 to 0.5. Thus assisting in limiting the dynamic power consumed by the cell when operating in read mode.

3.3 Write operation

The first step to steer the cell into write mode is to disconnect the mutually connected inverter pair. The same is done by exerting W = ‘0’. This effectively reduces the coupled inverter pair to a cascaded configuration dependent on BL. Firstly, the complement of the data to be stored at Q is set on BL. Then, WL signal is exerted to activate WA transistor. Thus, the data on BL is transferred to node Q1, which drives inv1 to produce the desired bit value at Q. Then Q drives inv2 to write data at QB. The additional signal W is utilized by the circuit to control the internal configuration of the bit cell. It enables the cell to convert the mutually coupled inverter pair configuration to a cascaded inverter configuration. But, this results in an increased control signal, resulting in increased interconnects in the circuits. But, it helps improve the write ability for the cell at optimal transistor sizing; therefore the area for the proposed 7T SRAM bit cell is lesser than its other counterparts (explained in Sect. 9). Therefore, the slightly increased overhead because of the extra control signal gets overshadowed by its benefits.

The RA transistor is cutoff when the cell is operating is write mode. To additionally assist the write operation, the voltage transfer characteristics for the inverters are adjusted. Also, the write operation for the cell relies on the swiftness of inv1; as the delay of a gate is inversely proportional to V_{DD}–V_{TH}. Thus, reducing the value of V_{TH} decreases the delay for the gate [30]. Therefore, PDL being an LVT NMOS ensure a swifter write operation. Optimally sized transistors along with the use of LVT NMOS for inv1 are step incorporated to build-up the write performance for the cell.

Table 1 Truth table for proposed 7 T SRAM bit cell

	W	WL	RL
Hold	1	0	0
Read	1	0	1
Write	0	1	0

4 Static analysis

The tool used for designing all the bit cells is Symica DE. The library files used for simulating the circuits is 32 nm technology node by Predictive Technology Models. The results obtained for the 7TP cell are compared against 6TC, 6TS, 7TL 7TY, 8TS, 9TC, and 10TK for validation. Each of these bit cell has already been discussed in Section II. The environment temperature is set to 27 °C for the complete study. The dimensions for all the cells are mentioned in Table 2. An important parameter that determines the stability of bit cell is the retention of stored data in standby as well as read access mode. The conventional method to measure the former is static noise margin (SNM); it is the maximum DC noise level a cell may withstand before an erroneous flip in the data of the bit cell is registered [28]. It is used to quantify the cell's stability and its immunity to noise [31]. It is obtained by graphically superimposing the transfer characteristics of the inverter core resulting in a two lobe based curve [32], called the butterfly curve. The SNM is the measure of side of the biggest square that perfectly fits inside the smaller lobes of the butterfly curve [33].

4.1 Hold noise margin

An SRAM cell for most part of its functioning remains in the hold mode. Therefore, the first parameter under analysis is the hold SNM (HSNM). The SNM for each bit cell is calculated as the side of the largest square that completely fits inside the smaller lobe of the butterfly curve. For a symmetrical butterfly curve, either of the lobes may be considered for calculation of SNM. To demonstrate the calculation of SNM, a square is embedded in the HSNM and RSNM curve for the butterfly curve. The same is depicted in Fig. 3(h). The HSNM for the 7TP cell is calculated as difference between the x-axis (y-axis) coordinates for red square embedded in the hold butterfly curve (123–27 or 279–183 = 96 mV). The RSNM for the 7TP cell is calculated as difference between the x-axis (y-axis) coordinates for blue square embedded in the read butterfly curve (133–65 or 289–221 = 68 mV). The values for HSNM of all the cells detailed in the schematic survey along with the proposed cell are presented in the Fig. 3; along with the read butterfly curve (explained in the subsequent sub-section) for each cell. All the obtained HSNM values are tabulated in Table 3. The values suggest that 7TP cell has a moderate hold performance with respect to other bit cells. The proposed cell performs better with respect to 6TC, 6TS, 7TL, and 7TY, while the HSNM of the 10TK cell is equivalent to the HSNM of the 7TP cell

Table 2 Cell Dimensions (in nm) for various SRAM bit cells

	6TC	6TS	7TL	7TY	7TP	8TS	9TC	10TK
PUL	72	120	64	64	64	160	64	200
PUR	72	180	64	64	64	160	64	200
PDL	72	180	166	96	166	160	96	200
PDR	72	180	96	96	96	160	96	200
ACL	144	120	128	96	96	160	64	200
ACR	144	120	128	96	96	160	64	200
R1	–	–	128	–	–	160		–
R2	–	–	128	–	–	160		–
TN	–	–	–	64	–	–		–
TP	–	–	–	64	–	–		–
DL	–	–		–	64	160		–
FB	–	–		–	64	160		–
WA					96			
RA					96			
P1							96	
N1							96	
N2							96	
N3							96	
FBL	–	–	–		–	–		200
FBR	–	–	–		–	–		200
NL	–	–	–		–	–		200
NR	–	–	–		–	–		200

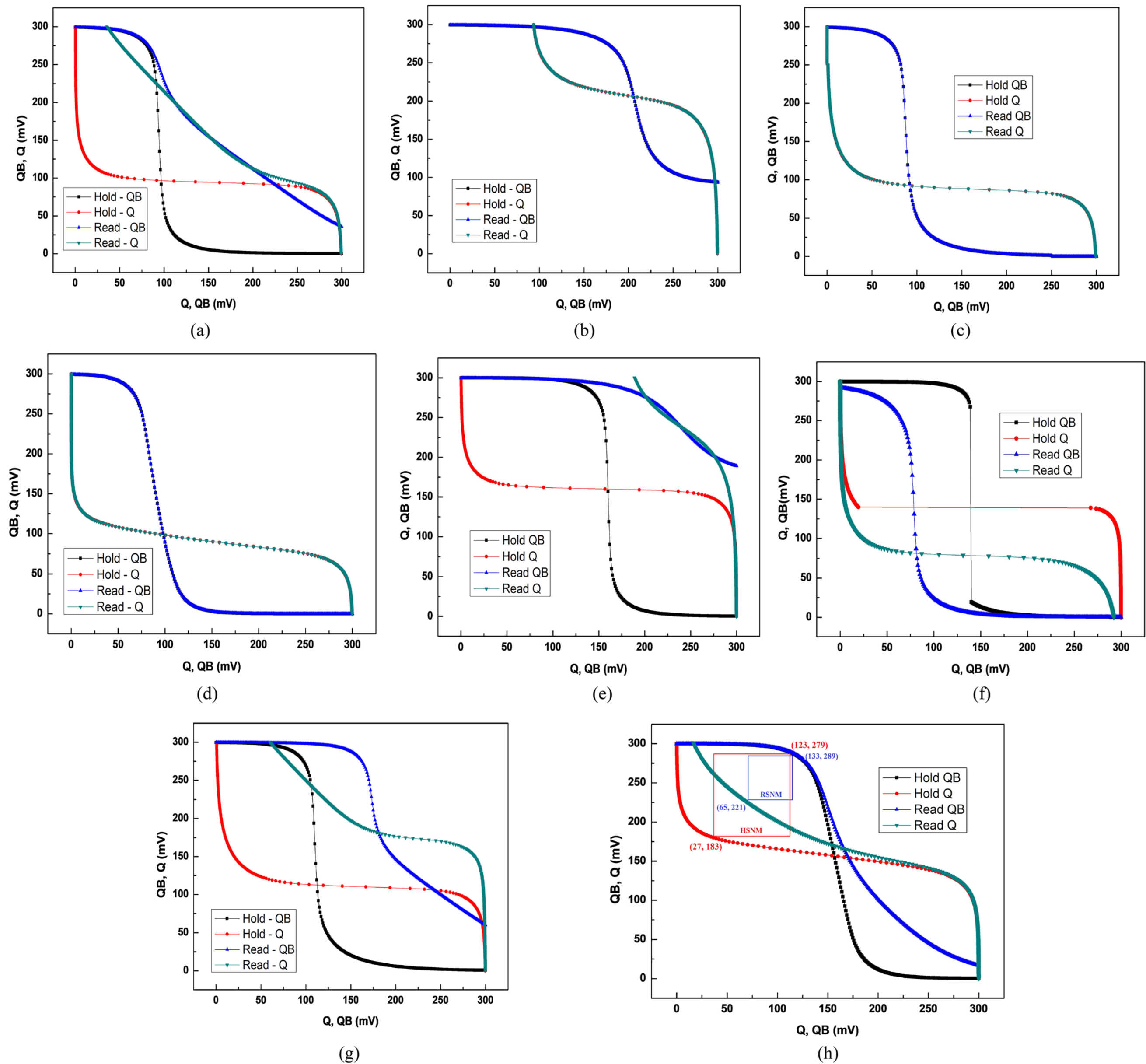


Fig. 3 Combined butterfly curves for HSNM and RSNM for **a** 6TC, **b** 6TS, **c** 7TL, **d** 7TY, **e** 8TS, **f** 9TC, **g** 10TK, and **h** 7TP SRAM cells

at 96 mV. But the 8TS and 9TC cells have a higher HSNM value compared to the 7TP cell.

4.2 Read noise margin

For the duration of the read mode, the bit value stored in the cell is retrieved using access transistors. For 6TC cell, the word-line is set high to cause conduction through the read access transistors. Thus, subjecting the bit cell to vulnerability, as there is a possibility of undesired flipping of data stored in the memory core. Therefore, it is important to measure the resilience of the cell during read mode; it is quantified as read SNM (RSNM). A differential read

Table 3 The performance of SRAM cells for static parameter (HSNM, RSNM, and WM)

Cells	HSNM (mV)	RSNM (mV)	WM (mV)
6TC	80	17	145
6TS	37	37	105
7TL	74	74	189
7TY	74	74	-
7TP	96	68	170
8TS	104	0	111
9TC	117	80	195
10TK	96	57	145

operation always has poor performance as the cell becomes more prone to noise [34] for both ‘0’ and ‘1’, as the cell discharges for both. This problem is more intensified by decreasing V_{DD}. Whereas, during a single ended read operation, the cell discharges for either ‘1’ or ‘0’, thereby reducing the possibility of error by half. Additionally, to boost the read discharge current vulnerability for the bit cell, the voltage transfer characteristics for the 7TP bit cell is modified to make it less vulnerable during the read operation. Consequently, the RSNM for the 7TP is higher in comparison to the other bit cells with a differential read configuration; the same can be inferred from Fig. 3. The HSNM and RSNM for all the bit cells are depicted in Fig. 3.

Another aspect vital for differential bit line sensing is the minimum required voltage of 50 mV [27]. The complementary bit lines of the bit cell should develop a 50 mV [27] minimum difference to sense the output. But the results show that the RSNM for 6TC is 17 mV which is way below the permissible limit. Therefore, it can be said that 6TC bit cells will fail to perform effective read operation at V_{DD} as low as 300 mV. On the other end, the cells 6TS, 7TL, 7TY, 9TC, and 10TK show RSNM of 37, 74, 74, 80, and 57 mV respectively. The proposed cell registers a RSNM of 68 mV even with a single ended port; hence it will perform a valid read operation.

4.3 Write stability

The robustness of a cell during write mode is measured as its ability to alter the stored data. Write margin (WM) is a reliable parameter for a cell’s write ability [35]. By definition, WM is estimated as the difference between the voltage level of V_{DD} and WL when the bit stored in the cell flips [36]. A balanced WM is essential to ensure a successful write operation. A very low value for WM makes it challenging to perform the write operation, while a high WM escalates its vulnerability to noise. WM is measured using the methodology recommended by Islam and Hasan [37]. The WM values for all bit cells except 7TY are tabulated in Table 3. The write operation for 7TY is divided into two pulses, while, all the other cells in this study utilize a single pulse to perform the write operation therefore, its evaluation is not included, to avoid projecting it as pseudo poor.

The WM values obtained for 6TC/6TS/7TL/8TS/9TC/10TK cells register a WM of 145/105/189/111/195/145 mV respectively. Table 3 collectively summarizes the static performance data for all bit cells. The graphical comparison for the same is presented in Fig. 4. All the cells have a commendable performance during the hold operation but their RSNM value acts as the differentiator. The RSNM butterfly curve of 8TS cell collapse; thereby making it highly susceptible to read noise. Another cells with considerably low RSNM value is 6TC at 17 mV. This cell is also susceptible to read noise. The other bit cells have reliable values for RSNM metric (Table 4).

The 9TC cell has a good performance for both HSNM and RSNM but its WM is extremely high, making its write operation highly susceptible to noise. The 10TK cell has a commendable performance for the three parameters but its high layout area (explained in section IX) make it a less viable. Thus, after analyzing the static performance of the 7TP cell, it can be stated that this cell has achieved a balance between the three modes of functioning—hold, read and write.

5 Cell ratio analysis

Cell ratio for a cell is the proportion between the aspect ratio of the access transistor and the corresponding pull-down network. For a conventional cell it determines the

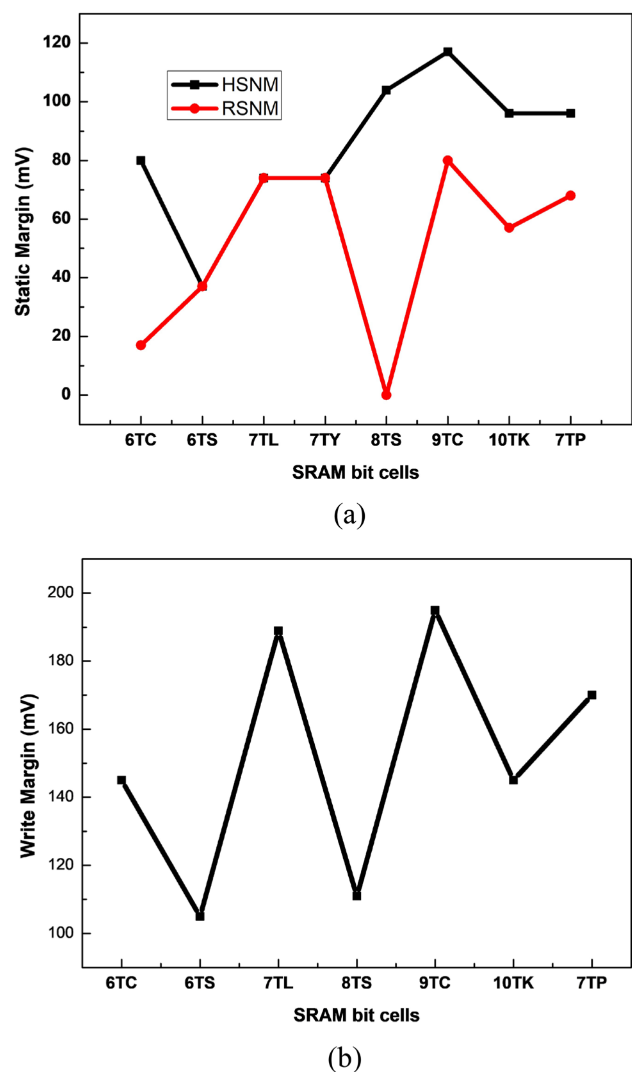


Fig. 4 Graphical representation of the static analysis for **a** HSNM and RSNM, **b** WM for various SRAM bit cells

Table 4 Performance of the 7TP cell in terms of Saturation voltage, delay, and SNM with varying cell ratio

Cell ratio	Saturation voltage (mV)	Time delay (ps)	SNM (mV)
1.5	91	59	63.6
2	76	71	87.36
2.5	70	90	90
3	62	101	84.56
3.5	56	129	78.43
4	53	156	70.56
4.5	49	180	67.2
5	46	245	61.26
5.5	43	280	56.58
6	40	330	52.8

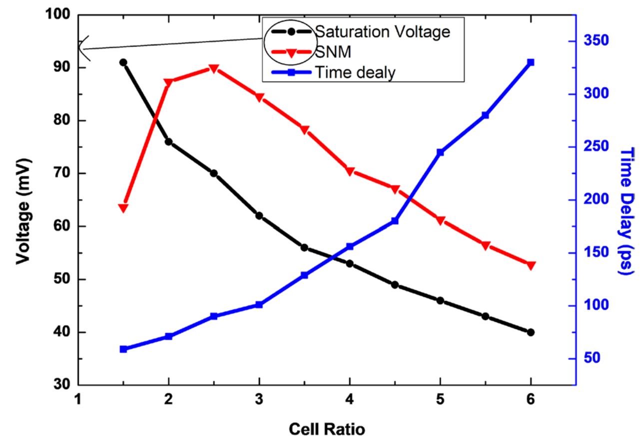


Fig. 5 Performance of the 7TP SRAM cell for varying cell ratios

optimum sizing for the best RSNM value for the cell. For this analysis the cell ratio of the 7TP bit cell is increased from 1 to 6 in steps of 0.5. The parameters that are measured with respect to the cell ratio are the HSNM, saturation voltage and the delay in attaining 40 mV (the minimum saturation voltage attained by all bit cells).

$$\text{Cell Ratio} = \frac{Aspect\ Ratio\ of\ Access\ Transistors}{Aspect\ Ratio\ of\ Pull\ Down\ Network} \quad (1)$$

The single-ended read port for the 7TP cell it carefully designed to not register a destructive read operation. For each cell ratio, there is a corresponding maximum voltage the BL rises to and it is referred to as saturation voltage. While, the delay in the cell is calculated as the time consumed by the cell to raise the bit-line voltage to 40 mV. The corresponding data is plotted on a double Y axis plot as shown in Fig. 5. An increase in the delay and saturation voltage is observed with an increment in the cell ratio for the proposed bit cell. While RSNM vs. cell ratio trend line attains peak corresponding to cell ratio of 2.5. The saturation voltage is sufficiently high, while the delay is fairly low for the same cell ratio. Therefore, 2.5 is considered as the most optimum cell ratio for the 7TP SRAM bit cell.

6 Dynamic write analysis

During static analysis, the pulse width for WL is assumed to be infinite. While, for real time operations the pulse width for write operation is finite. Thus, to characterize the real time write ability for a cell, it is primal to measure the write pulse width. It is defined as the least possible pulse width required to alter the bit stored in the cell. If it is less than that then the data in the cell will not change, causing a write failure. Figure 6 depicts the write operation for two consecutive pulse. The initial conditional for the 7TP is Q = ‘0’ and QB = ‘1’. The pulse-width for the 7TP cell is found to be 30 ns.

To analyze the dynamic write ability of SRAM bit cell with increment in values of V_{DD}, the plot for V_{DD} vs pulse width is presented in Fig. 7. The plot is split for V_{DD} varying from (a) 0.3 to 0.6 V and (b) for 0.7 to 1 V. This is done for the ease of comparison as well as to demonstrate commendable dynamic write ability for the proposed cell for low as well as high V_{DD}. Figure 7(a) validates that the 7TP cell operates at the lowest pulse width of 30 ns at 300 mV. The highest dynamic pulse width is utilized by 6TS bit cell at 100 ns for V_{DD} at 300 mV. While, the performance of 6TC, 7TL, 8TS, and 10TK cell is better in comparison to 6TS but slightly higher than the 7TP cell. But these aforementioned cells have a differential ended write operation and it is an accepted notion that in comparison to the former a single ended write is more challenging. Thereby, establishing the improvement in the performance of the 7TP cell. The 9TC cell also has a single ended operation but its pulse width requirements are slightly higher than the 7TP cell.

Therefore, for lower values of V_{DD} it can be deduced that 7TP cell requires a shorter pulse width with respect to other cells. The proposed SRAM bit cell is able to maintain its credibility for V_{DD} in the range of 0.7 to 1 V. The cell displays successful write operation for least value of pulse width for all values of V_{DD}. The SRAM bit cells that have comparable performance to 7TP bit cell are the 6TC, 7TL, and 10TK SRAM bit cells but they are differential in nature so that automatically makes it easier to write into them. Therefore, it is appropriate to infer that 7TP cell has an improved performance in comparison to other cells.

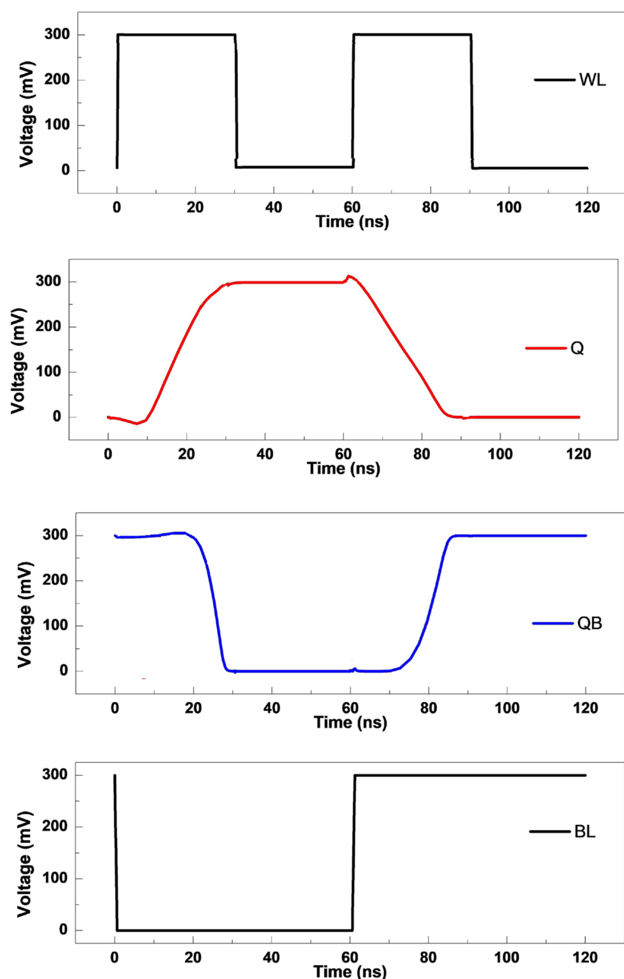
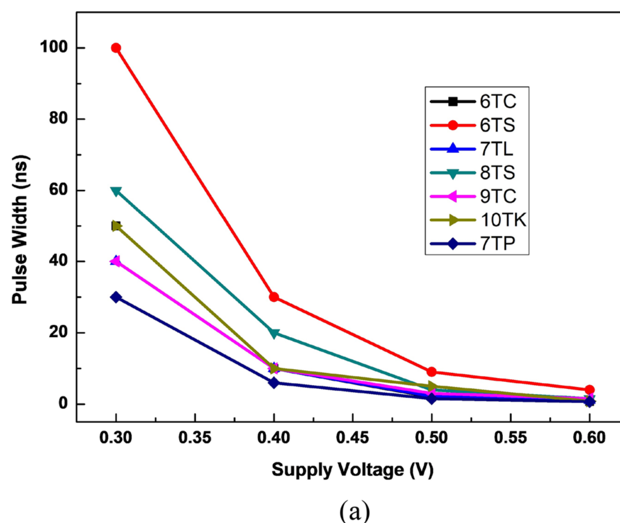
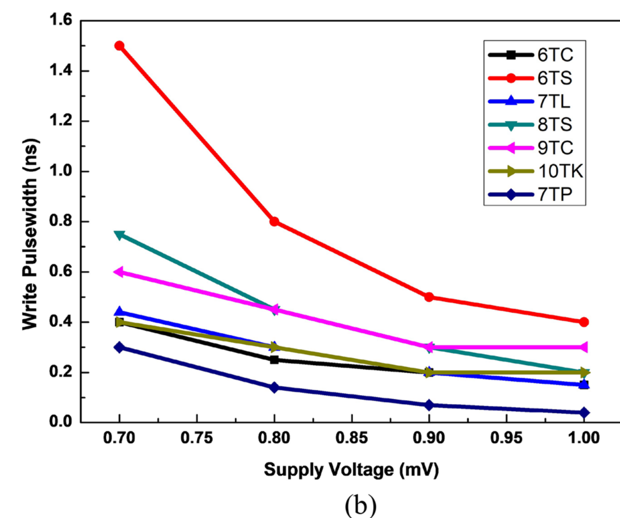


Fig. 6 Two consecutive write operation for the 7TP cell performed at pulse width of 30 ns



(a)



(b)

Fig. 7 Characteristic plots of pulse width as a function of V_{DD} **a** 0.3 to 0.6 V and **b** 0.7 to 1 V for SRAM cells

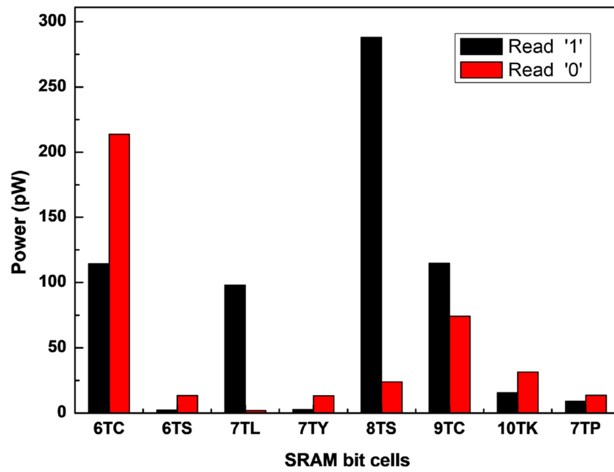
7 Power analysis

7.1 Read and write power analysis

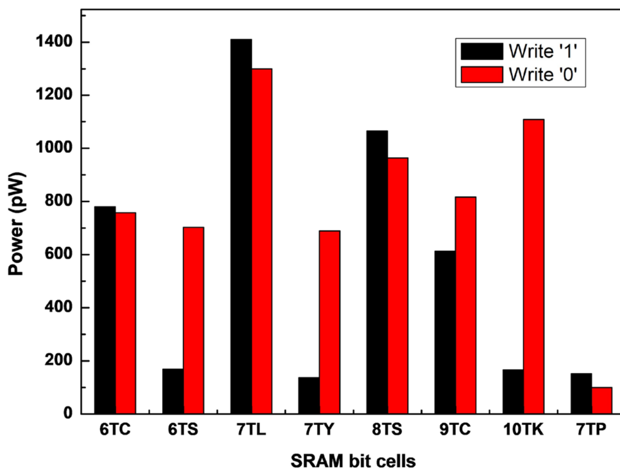
A cell consumes most power during the phase it is being accessed. This can be either read or write operation. But of the two, more power is consumed during the write operation. This same conclusion can also be drawn from the Fig. 8, which gives a graphical comparison for power consumed by the cell in (a) read and (b) write mode.

For a differential read operation the power consumed is evaluated over the time required to drop the bit-line voltage to 50 mV. While, for single ended cell the pulse width is taken to be time needed for data to reach the vicinity of switching voltage. The power consumption during the read operation is highest for 8TS cell for data value '1'. The read cell though has a single ended operation the stacking configuration increases the read drive current. The device dimensions are also large for the cell, thereby increasing the power dissipation for the cell. 6TC cell also experiences a high read power for both '0' and '1', due to its differential nature. Though 10TK cell is also differential in nature, its read power is low owing to the shortened discharged path and ST inverter configuration. The remaining SRAM bit cells—6TS, 7TY, are single ended in nature and have read power for Q = '1' less than 7TP due to no discharge path for the operation. The power consumption for Q = '0' is comparable for the three cells.

During the write operation a longer pulse-width is needed to deliberately modify the data present in the cell. By default, it is assumed that the data stored inside the cell is Q = '0' and QB = '1'. For the first cycle, the input data exerted into the cell via BL is '0'. This results in '0' at node Q1, thus the node Q develops '1' and the node QB becomes '0'. Then, for



(a)



(b)

Fig. 8 Power consumption by the different SRAM cell when operating in **a** read and **b** write mode

the next cycle, the BL signal is exerted high, to develop ‘0’ and ‘1’ at node Q and QB respectively. So for write power analysis the operation is performed and the power consumed during the process is recorded. The power dissipated during a differential write operation is higher with respect to a single ended cell [38]. The same can be inferred from Fig. 8, as the power consumption for 6TC, 7TL, 8TS, and 10TK is considerably high. Single ended cells are generally biased towards either ‘0’ or ‘1’, resulting in high power consumption for the other value. This characteristic of a single-ended SRAM cell is attributed to its coupled inverter based memory core. But the write operation for the 7TP cell modifies the inverter core to form a cascaded inverter configuration. Also, the use of LVT MOS reduces the power requirement for the cell. Thereby making it more power efficient.

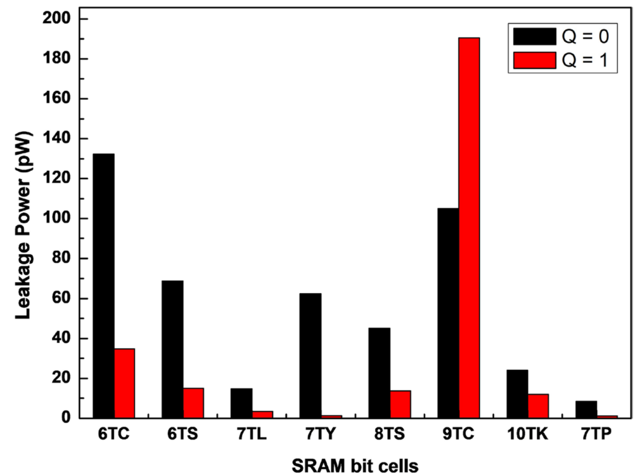


Fig. 9 Graphical comparison for power consumed during the hold state for SRAM bit cells

7.2 Leakage power analysis

Most cells in the SRAM array are maintained in hold state. Hence, leakage power consumed by a cell during the hold mode forms a key component of total power consumption for a cell [37]. Additionally, in submicron technologies, the increase in leakage is attributed to nanometer feature size for the device. Therefore, it is essential to study the leakage power for a cell. To identify the leakage power for the bit cell, the leakage current is simulated and the standby power is calculated as V_{DD} times of leakage current [39]. A graphical comparison of power consumed because of leakage in the cell is depicted in Fig. 9. It is inferred from Fig. 9 that the leakage power recorded for the 7TP cell is very low. The leakage power recorded for 7TP cell is 8.4 pW and 1.2 pW for Q = ‘0’ and ‘1’ respectively. The only other cell with comparable leakage power is 7TL, as it also has a single-ended nature. The highest leakage power is registered for 9TC; this is a consequence of its additional control signals being ON during the hold state as well, causing a high current to flow through the circuit to keep the inverter core intact.

The high values for leakage of 6TC is attributed to its differential nature and for 6TS is due to PDL being always in ON state. For 10TK cell, though differential in nature has low leakage due to its stacked inverter configuration along with the disable control signals help reduce the leakage power consumption for the cell [40].

8 Tolerance analysis

8.1 Process variation tolerance

SRAM bit cell have observed a very sharp decline in technology node resulting in serious variability issue at the circuit level [41]. Additionally, the increasing size of cache memory has resulted in upsurge in process variations among cells. This causes degradation in performance of adjacent bit cell due to asymmetrical characteristics [15]. Therefore, statistical methods are utilized to detect this degree of variation in the performance all the cells. Inter-die V_{TH} mismatch is taken as the main statistical parameter for evaluation. To ensure reliability, a failure probability of $P_{fail} < 10^{-10}$ is required [41]. The probability is Gaussian in nature and is calculated based on μ-6σ parameter. Here, μ is the mean value of V_{TH} and σ is its standard deviation. The factors responsible for process variation are line edge roughness, chemical–mechanical polishing, random dopant fluctuation, and lithography effects [42]. Most of these parameters are neither predictable nor can they be controlled. But the location and distribution of these factors influences the V_{TH} [42]. Therefore, in this work, V_{TH} is used as the primary source to predict the variability tolerance of the 7TP cell.

The Monte Carlo simulations for static parameters of 7TP are performed for 10,000 data point. The results for the same are depicted in Fig. 10. The process variation results yield the least value for HSNM and RSNM to be 87 and 48 mV respectively. While the WM obtained for maximum variation is 195 mV. The Monte Carlo simulation of the 7TP bit cell for 10,000 data points is compared with respect to other cells. The result for each cell deteriorate in keeping with 6σ global variations, the worst case value attained for the cells are demonstrated in Fig. 10(d). The 6TC, 6TS, and 8TS cell register a drop in HNSM, while their RSNM curve collapses. Thus, certifying a high read failure probabilty for the cells. Whereas, the 7TL and 9TC cells experience increases in WM to 200 and 210 mV respectively, which is considerabily high, making them highly susceptible to noise. The

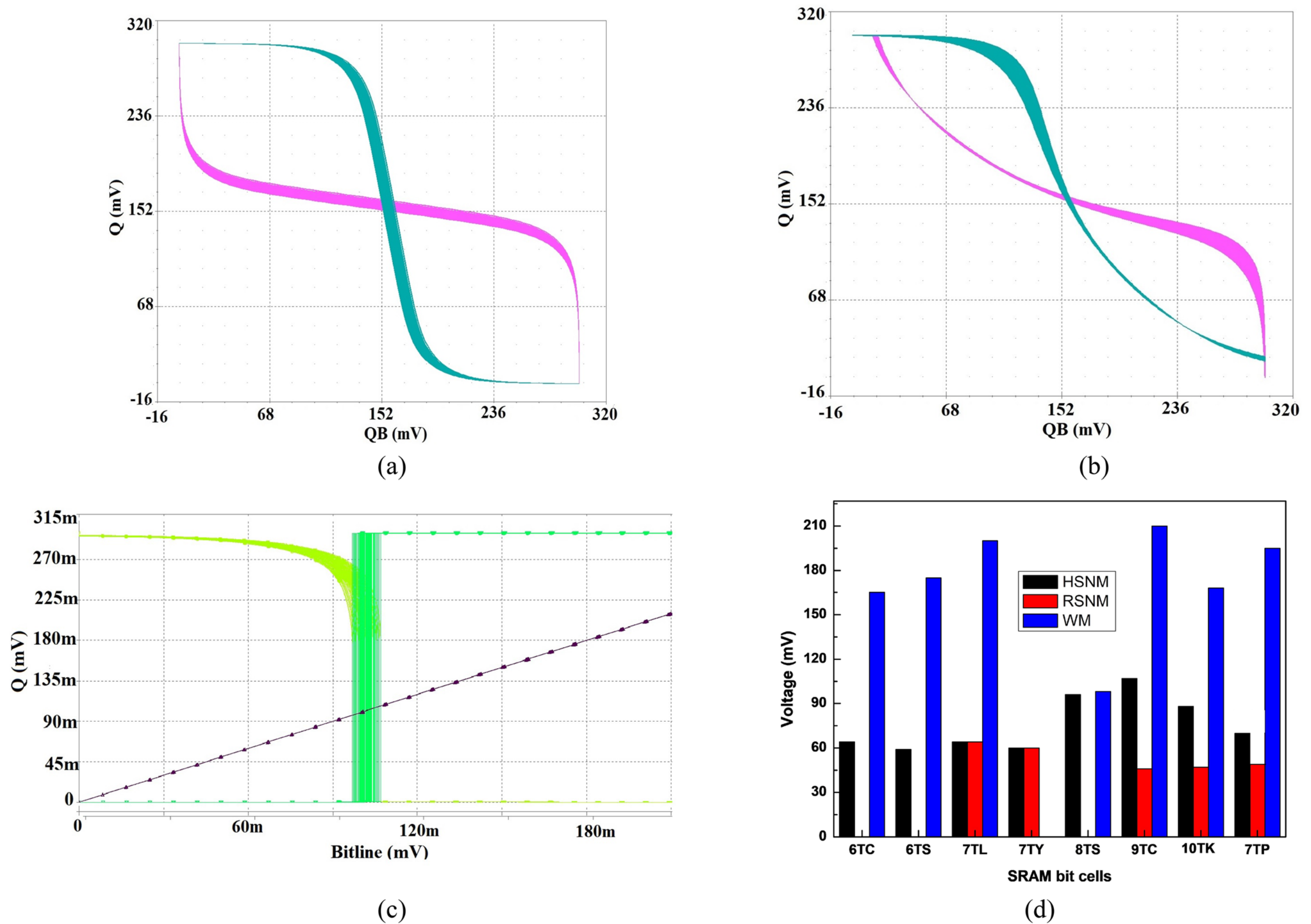


Fig. 10 Effect of process variation on **a** Hold SNM, **b** Read SNM, **c** WM for 7TP cell, and **d** graphical comparison for minimum values obtained at 10,000 Monte Carlo simulations for bit cells

6TC, 6TS and 10TK cells have a reliable WM in the vicinity of 165 mV but their poor RSNM values make them highly prone to read failure.

The MonteCarlo simulations reveal the cells vulnerability to failure subject to 6σ global variations. So it can be deduced from the analysis that all cells register a decline in their perfromance but the 7TP SRAM bit cell maintain reliable perfromance.

8.2 Voltage tolerance

The static analysis is included for the proposed cell for voltage levels lower than 0.3 V up to 0.14 V. The values as depicted in the Fig. 11 reflect that the cell is unable to perform write operation at 0.16 V or lower voltages. The least voltage at which the cell is able to maintain its functionality is 0.18 V.

However, the static performance at this voltage is so low that sensing the read for single ended cell would become highly difficult. Therefore, in keeping with stable performance for all the modes of operation, 0.3 V is taken as the least voltage for operation for the bit cell.

8.3 Temperature tolerance

SRAM circuits are required to function under a wide range of temperature. A device temperature may surge due to relentless operation or environmental circumstances. Therefore, to account for the temperature variation encountered by the cache memory, a temperature variation analysis is performed for the proposed cell. This is accomplished to ensure the performance reliability of the cell. The analysis is performed for temperature varying from 25 to 85 °C.

The results for the analysis is presented in Fig. 12. With the variation in temperature a deviation in performance of static parameters for the cell is observed. The cell maintains

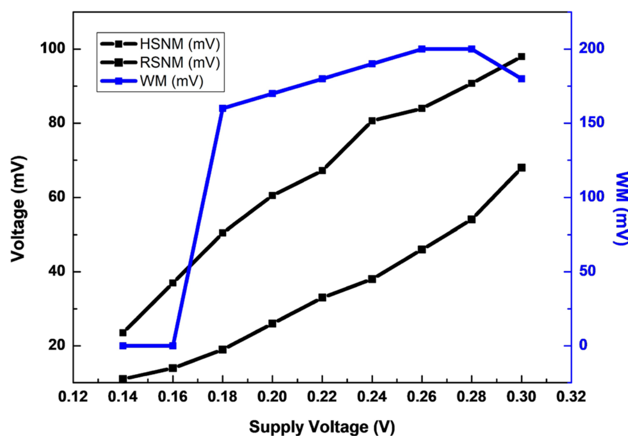
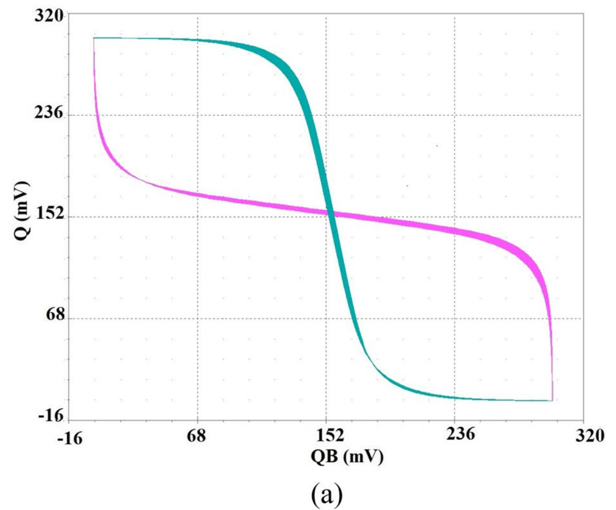
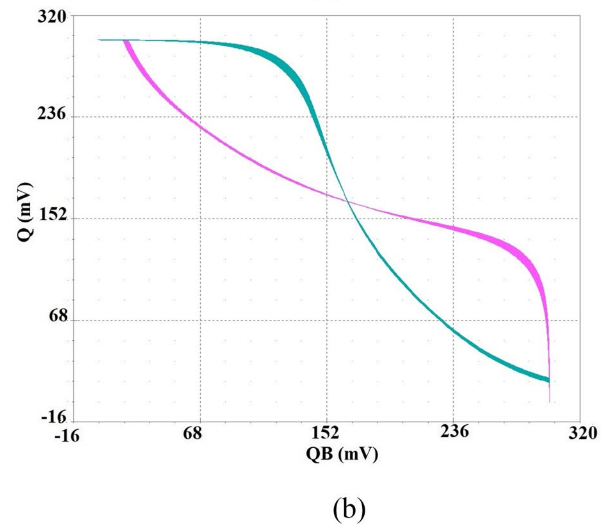


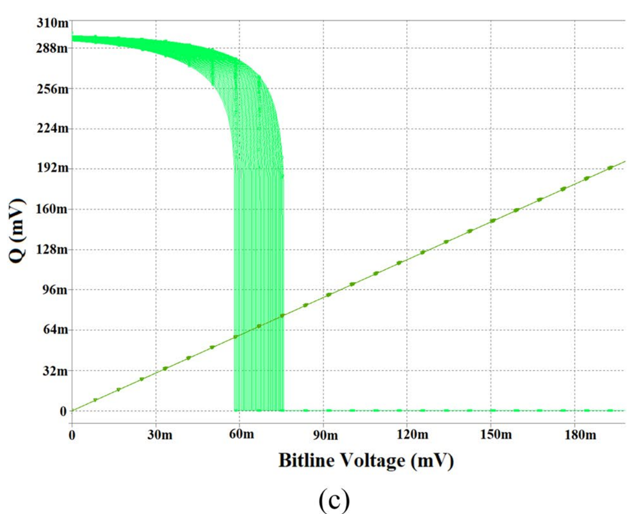
Fig. 11 Variation in RSNM and WM for 7TP cell with varying V_{DD}



(a)



(b)



(c)

Fig. 12 Deviation in performance of **a** HSNM, **b** RSNM, and WM for 7TP cell due to temperature variation

HSNM and RSNM margins at 90 and 58 mV respectively; which is a decline of 0.1 and 0.16 mV/°C from its hold and read static performance respectively. While, the WM increases to 230 mV. This data justifies the performance of 7TP bit cell as reliable with variation in temperature.

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9 Layout and area

SRAM cells are arranged into large arrays to form cache memory. Thus, in order to integrate large number of bit cells into the cache memory of the SoC, it is imperative to have minimal area for a bit cell. The layout design for the bit cells are given in Fig. 13. The dimensions of each cell are mentioned alongside the layout. Also, the length (μm), width (μm) and area (μm^2) for each cell are plotted in Fig. 15 for an easy comparison.

The layout for the 4×4 array for the 7TP cell is depicted in Fig. 14. The layout is designed to demonstrate the routing directions for supply lines and control signals for the cell. The V_{DD}, ground potential, W and RL1 signal are routed vertically, while the BL and WL signal for the cell are routed horizontally. The write operation for the bit cell is controlled via control signals WL and W, which form independent row and column based signals respectively. While, the read operation is controlled by the RL signal. The 4×4 array based layout for the bit cell helps understand the array based implementation for the SRAM memory. For ease of comparison the bit cell area along with the cell dimension (length and width) are plotted in Fig. 15.

The SRAM bit cell with the least area of 0.456 μm^2 is 6TC cell. This is a key factor that makes 6TC the most

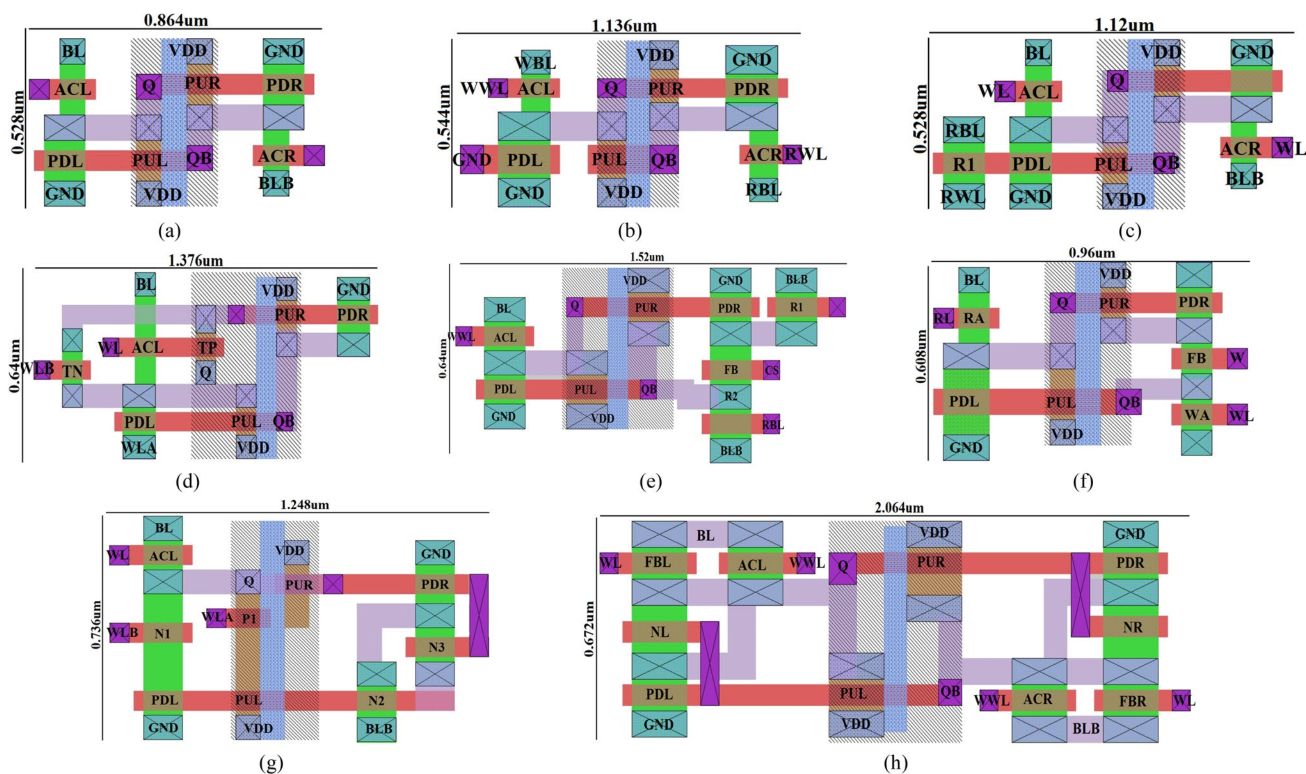

Fig. 13 Layout for the **a** 6TC, **b** 6TS, **c** 7TL, **d** 7TY, **e** 8TS, **f** 7TP, **g** 9TC, and **h** 10 T SRAM bit cells

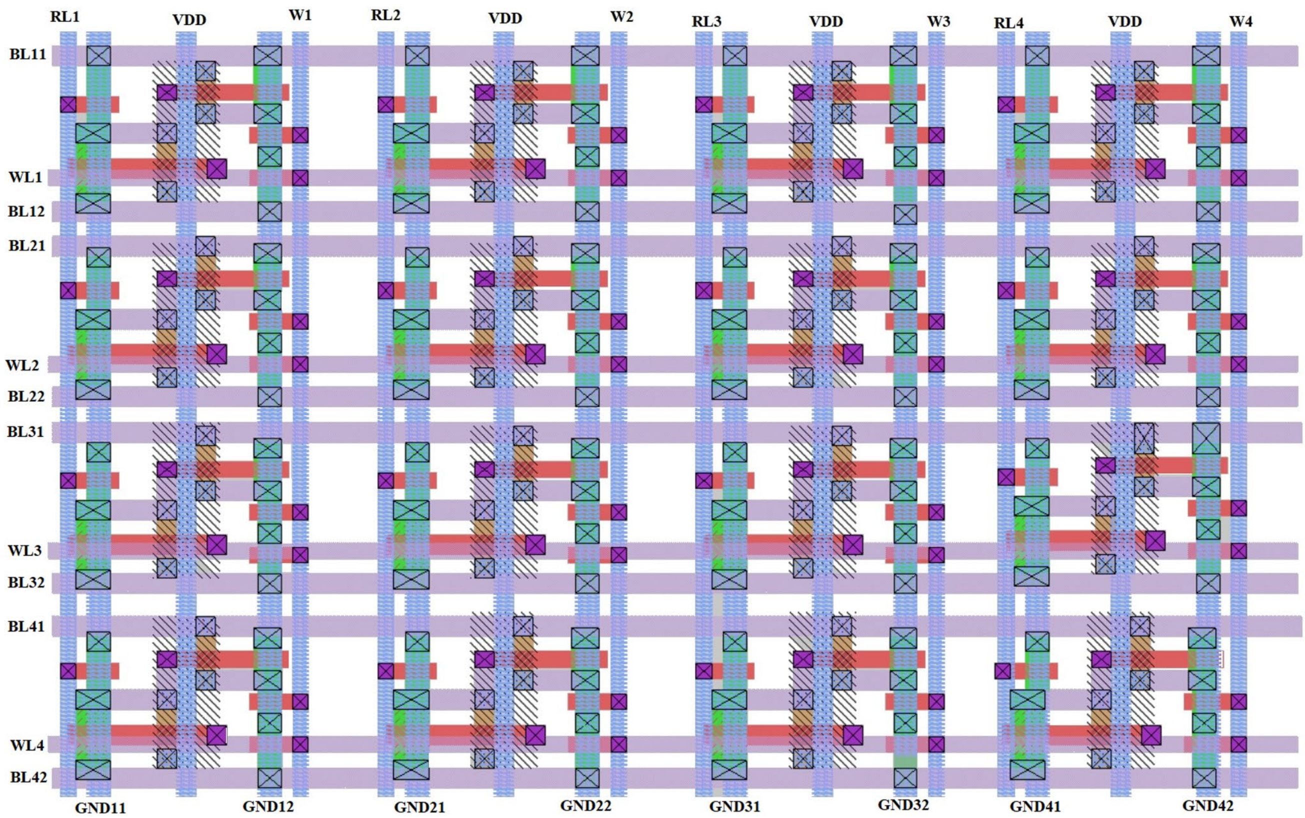

Fig. 14 A 4×4 block of the proposed 7TSE SRAM bit cell showcasing the direction of control signal and supply line routing

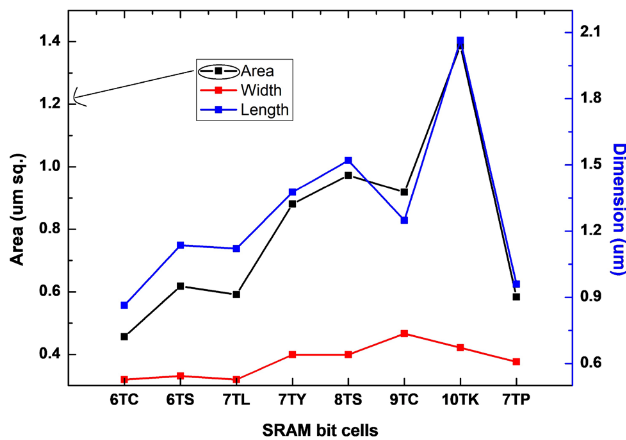

Fig. 15 Graphical comparison for area and dimensions of SRAM cells

preferred memory cell for the industry. But this is only the case for 6TC, the 6TS bit cell though has the same transistor count, but its area is significantly higher at 0.618 μm^2. The 7TP bit cell on the other hand occupies on 0.584 μm^2 which is 27.8% more than 6TC but is 5.55% less than the 6TS cell. Also, it is the smallest SRAM bit cell in terms of area after 6TC. The area for the other bit cells; 6TS, 7TL, 7TY, 8TS, 9TC and 10TK is greater as compared to 7TP cell by 5.87%, 1.31%, 50.8%, 66.67%, 57.36%, and 137.63% respectively.

10 Conclusion

In this work, a single bit-line enabled, single port 7T bit cell is proposed. The feature size for the cell is 32 nm and is simulated at 300 mV supply voltage. The single bit-line architecture of the proposed cell decreases its switching activity factor. The performance of the proposed 7T cell is validated against its 6T, 7T, 8T, 9T, and 10T pre-existing counterparts. The comparison yields that the static performance for the 7TP cell for hold operation is higher than its 6T, 7T, and 10T counterparts, while the read operation is better than all except other 7T cells. Whereas, the write margin for the cell 170 mV, which is fairly balanced and is near the ideal value of $V_{DD}/2$. The cell requires a pulse-width of 30 ns to register a successful write operation, which is fastest amongst the other pre-existing cells in the paper. All the aforementioned merits for the 7TP SRAM bit cell are obtained for minimal power consumption. The tolerance analysis validates that the cell maintains a reliable performance under PVT variations. The aforementioned merits are achieved for area footprint of 0.584 μm^2. This is 27.8% greater than 6TC cell but is

significantly smaller than other counterparts studied. The area for 6TS, 7TL, 7TY, 8TS, 9TC, and 10TK is greater by 5.87%, 1.31%, 50.8%, 66.67%, 57.36%, and 137.63% respectively as compared to 7TP. Thus, it is confirmed that the single port, single bit-line enabled proposed cell is viable when compared to other bit cells.

Data availability Data sharing not applicable to this article as no datasets were generated or analyzed during the current study.

References

1. Gavaskar, K., Narayanan, M. S., Nachammal, M. S., & Vignesh, K. (2021). Design and comparative analysis of SRAM array using low leakage controlled transistor techniques with improved delay. *Journal of Ambient Intelligence and Humanized Computing*. https://doi.org/10.1007/s12652-021-03353-z
2. Prasad, G., & Anand, A. (2015). Statistical analysis of low-power SRAM cell structure. *Analog Integrated Circuits and Signal Processing, 82*, 349–358.
3. Mukherjee, R., Saha, P., Chakrabarti, I., Dutta, P. K., & Ray, A. K. (2018). Fast adaptive motion estimation algorithm and its efficient VLSI system for high definition videos. *Expert Systems with Applications, 101*, 159–175.
4. Gavaskar, K., Ragupathy, U. S., & Malini, V. (2019). Design of novel SRAM cell using hybrid VLSI techniques for low leakage and high speed in embedded memories. *Wireless Personal Communications, 108*(4), 2311–2339.
5. Gavaskar, K., & Ragupathy, U. S. (2014). An efficient design and comparative analysis of low power memory cell structures. In *2014 International Conference on Green Computing Communication and Electrical Engineering (ICGCCEE)* (pp. 1–5). IEEE.
6. Lorenzo, R., & Pailly, R. (2020). Single bit-line 11T SRAM cell for low power and improved stability. *IET Computers and Digital Techniques, 14*(3), 114–121.
7. Rathod, A. P. S., Lakhera, P., Baliga, A. K., Mittal, P., Kumar, B. (2015). Performance comparison of pass transistor and CMOS logic configuration based de-multiplexers. In *International Conference on Computing, Communication & Automation* (pp. 1433–1437)
8. Lorenzo, R., & Chaudhury, S. (2017). A novel 9T SRAM architecture for low leakage and high performance. *Analog Integrated Circuits and Signal Processing, 92*, 315–325.
9. Boley, J., Wang, J., & Calhoun, B. H. (2012). Analyzing subthreshold bitcell topologies and the effects of assist methods on SRAM VMIN. *Journal of Low Power Electronics and Applications, 2*, 143–154.
10. Nayak, D., Acharya, D. P., & Mahapatra, K. (2016). An improved energy efficient SRAM cell for access over a wide frequency range. *Solid State Electronics, 126*, 14–22.
11. Kranti, A., & Armstrong, G. A. (2008). 6-T SRAM cell design with nanoscale double-gate SOI MOSFETs: impact of source/drain engineering and circuit topology. *Semiconductor Science and Technology, 23*, 075049.
12. Mittal, P., Negi, Y. S., & Singh, R. K. (2016). A depth analysis for different structures of organic thin film transistors: modeling of performance limiting issues. *Microelectronics Engineering, 150*, 7.
13. Gavaskar, K., Ragupathy, U. S., & Malini, V. (2019). Proposed design of 1 kb memory array structure for cache memories. *Wireless Personal Communications, 109*(2), 823–847.
14. Raj, K., Kumar, B., & Mittal, P. (2009). FPGA implementation of mask level CMOS layout design of redundant binary signed digit comparator. *International Journal of Computer Science and Network Security, 9*(9), 107–115.
15. Kumar, T. S., & Tripathi, S. L. (2021). Process evaluation in FinFET based 7T SRAM cell. *Analog Integrated Circuits and Signal Processing, 109*, 545–551.
16. Lorenzo, R., & Chaudhury, S. (2017). A novel SRAM cell design with a body-bias controller circuit for low leakage, high speed and improved stability. *Wireless Personal Communications, 94*, 3513–3529.
17. Tu, M. H., Lin, J. Y., Tsai, M. C., Jou, S. J., & Chuang, C. T. (2011). Single-ended subthreshold SRAM with asymmetrical write/read assist. *IEEE Transactions on Circuits Systems I: Regular Papers, 57*(2011), 3039–3047.
18. Kumar, B., Kaushik, B. K., Negi, Y. S., Mittal, P., & Mandal, A. (2011). Organic thin film transistors characteristics parameters, structures and their applications. *IEEE Recent Advances in Intelligent Computational Systems, 2011*, 706–711.
19. Anitha, D., Manjunathachari, K., Kumar, P. S., & Prasad, G. (2017). Design of low leakage process tolerant SRAM cell. *Analog Integrated Circuits and Signal Processing, 93*, 531–538.
20. Mittal, P., & Kumar, N. (2020). Comparative analysis of 90nm MOSFET and 18nm FinFET based different multiplexers for low power digital circuits. *International Journal of Advanced Science and Technology, 29*, 4089–4096.
21. Surana, N., & Mekie, J. (2019). Energy efficient single-ended 6-T SRAM for multimedia applications. *IEEE Transactions on Circuits and Systems II: Express Briefs, 66*, 1023.
22. Liu, J. S., Clavel, M. B., & Hudait, M. K. (2017). An energy-efficient tensile strained Ge/InGaAs TFET 7T SRAM cell architecture for ultra-low voltage applications. *IEEE Transactions on Electron Devices, 64*, 2193–2200.
23. Yang, Y., Jeong, H., Song, S. C., Wang, J., Yeap, G., & Jung, S. O. (2016). Single bit-line 7T SRAM cell for near-threshold voltage operation with enhanced performance and energy in 14 nm FinFET technology. *IEEE Transactions on Circuits and Systems I: Regular Papers, 63*, 1023.
24. Singh, P., & Vishvakarma, S. K. (2017). Ultra-low power high stability 8T SRAM for application in object tracking system. *IEEE Access, 6*, 2279–2290.
25. Cho, K., Park, J., Oh, T. W., & Jung, O. K. (2020). One sided Schmitt-Trigger Based 9T SRAM cell for near threshold operation. *IEEE Transactions on Circuits and Systems I: Regular Papers, 67*, 1551.
26. Kulkarni, J. P., & Roy, K. (2012). Ultralow-voltage process-variation-tolerant schmitt-trigger-based SRAM design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 20*, 319.
27. Kulkarni, J. P., Kim, K., & Roy, K. (2007). A 160 mV robust schmitt trigger based subthreshold SRAM. *IEEE Journal of Solid-State Circuits, 42*, 2303–2313.
28. Negi, S., Rana, A., Baliga, A.K., Mittal, P., Kumar, B. (2015). Performance analysis of dual gate organic thin film transistor and organic SR latch application. In: *International Conference on Computing, Communication & Automation*, pp. 1427–1432.
29. Rawat, B., & Mittal, P. (2020). Analysis of varied architectural configuration for 7T SRAM bit cell. In: *4th International Conference on Recent Trend in Communication & Electronics*.
30. Kang, S., Leblebici, Y., & Kim, C. (2015). *CMOS digital integrated circuits*, 3rd ed. New York; McGraw-Hill, pp.204, 422.
31. Krishna, R., & Duraiswamy, P. (2021). Low leakage 10T SRAM cell with improved data stability in deep sub-micron technologies. *Analog Integrated Circuits and Signal Processing, 109*, 153–163.

32. Mann, R. W., Wang, J., Nalam, S., Khanna, S., Braceras, G., Pilo, H., & Calhoun, B. H. (2010). Impact of circuit assist method on margin and performance in 6T SRAM. *Solid State Electronics, 54*, 1398–1407.
33. Reddy, B. K. N., Ramalingaswamy, C., Nagulapalli, R., & Ramesh, D. (2019). A novel 8T SRAM with improved cell density. *Analog Integrated Circuits and Signal Processing, 98*, 357–366.
34. Rawat, B., & Mittal, P. (2021). A 32 nm single ended single port 7T SRAM for low power utilization. *Semiconductor Science and Technology, 36*, 095006.
35. Singh, J., Mohanty, S. P., & Pradhan, D. K. (2013). *Robust SRAM designs and analysis*. Springer.
36. Ahmad, S., Gupta, M. K., Alam, N., & Hasan, M. (2016). Single-ended Schmitt trigger based robust low power SRAM cell. *IEEE Transaction on Very Large Scale Integration (VLSI) Systems, 20*, 2634.
37. Islam, A., & Hasan, M. (2012). Leakage characterization of 10T SRAM cell. *IEEE Transactions on Electron Devices, 59*, 631–638.
38. Islam, A., & Hasan, M. (2011). Single-ended 6T SRAM cell to improve dynamic power dissipation by decreasing activity factor. *The Mediterranain Journal of Electronics and Communication, 7*, 172–181.
39. Gavaskar, K., & Ragupathy, U. S. (2019). Low power self-controllable voltage level and low swing logic based 11T SRAM cell for high speed CMOS circuits. *Analog Integrated Circuits and Signal Processing, 100*(1), 61–77.
40. Lin, S., Kim, Y.B., & Lombardi, F. (2008). A highly-stable nanometer memory for low power design. *Proc. IEEE International Workshop Design Test of Nano Devices, Circuits Systems* 17.
41. Doorn, T., Maten, E.T., Croon, J., Bucchianico, J.D., & Wittich, O. (2008). Importance sampling Monte Carlo simulations for accurate estimation of SRAM yield. In *ESSCIRC 2008 - 34th European Solid-State Circuits Conference*.
42. Ding, J., & Asenov, A. (2020). The analysis of static random access memory stability under the influence of statistical variability and bias temperature instability-induced ageing. *Semiconductor Science and Technology, 36*, 025008.

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Bhawna Rawat was born in Delhi, India in 1993. She received her B. Tech Degree in Electronics and Communication Engineering from Shiv Nadar University, Greater Noida, India in 2015. She received M.Tech degree in VLSI Design from Indira Gandhi Delhi Technical University for Women, Delhi, India. She is presently pursuing Ph.D. at Delhi Technological University, New Delhi, India. Her research interests include low power circuit design, memory circuits in emerging technologies.

Poornima Mittal (Ph.D, M.Tech(H), B.Tech), Member IEEE has published 140 + research papers in international journals and conferences of repute. Her research interest includes design/modeling of flexible electronic devices, memory and low power VLSI circuits. She has published two patents on novel TFT structure and memory design. Also, she has published a Text Book titled "Organic Thin-Film-Transistor Applications: Materials to Circuits" by CRC Press, Taylor & Francis in 2016. She is the reviewer of IEEE transactions and other reputed international journals of IEEE, IET, Elsevier, IOP, Wiley and Taylor & Francis. She has received the research awards in 2012 and 2015 for her dedicated research at Graphic Era University, Dehradun. Also, she has received Commendable Research Awards in 2019, 2020, 2021 and 2022 at Delhi Technological University, Delhi. She is the recipient of Innovator of the Year Award at Uttarakhand State Science and Technology Congress in 2016. She has delivered many expert talks and chaired sessions in the reputed international conferences. She is the life member of many professional societies. She has more than 16 years of academic and research experience. Presently, she is working as Professor in the Department of Electronics and Communication Engineering at Delhi Technological University, Delhi, India..