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SBCCI'2021 Guest Editorial

Fernando Gehm Moraes[1] · Bernardo Leite[2]

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The Symposium on Integrated Circuits and Systems Design (SBCCI) is an international forum dedicated to Integrated Circuits and Systems Design, Test and Electronic Design automation (EDA), held annually in Brazil. The SBCCI has established itself as an important international forum for the presentation of advanced research results on leading-edge aspects of integrated circuits and systems design, such as Analog circuits, mixed-signal and Digital Integrated Circuits Design, dedicated and reconfigurable architectures, EDA tools, design methods, embedded Systems, System-on-chip, and Nanoarchitectures, as well as Verification and Test Methods. This 34th SBCCI edition was planned to take place in Campinas, 100 km from São Paulo, but transformed into a virtual event due to the Convid-19 pandemic

This special section contains extended versions of the best papers presented at the SBCCI'2021. The papers have been again refereed along the usual refereeing process in force at the Analog Integrated Circuits and Signal Processing Journal. We are proud to offer these papers to the readers of this journal now. Seven papers have been finally selected, covering a variety of topics related to the event, including:

- Low-power circuits: (1) "***An Ultra-Low-Power CMOS Smart Temperature Sensor based on Frequency to Digital Conversion***" – This work presents an integrated smart temperature sensor implemented in a 180 nm CMOS technology suitable for low voltage and ultra-low power electronic applications. The designed circuit uses a frequency to digital conversion topology, in which the frequency of an internal signal is linearly dependent on the room temperature. (2) "***An Ultra Low Power Analog Integrated Radial Basis Function Classifier for Smart IoT Systems***" – The authors propose an analog classification system, combining Analog Feature Extraction with an Analog Classifier, eliminating most digital circuits, appropriate for battery-operated systems, as IoT devices.
- Bio-medical applications: (1) "***Auricular vagus nerve stimulator for closed-loop biofeedback-based operation***" – The Authors propose an Auricular vagus nerve stimulation (aVNS) hardware for closed-loop application, which utilizes cardiorespiratory sensing using embedded sensors (and/or external sensors), processes and analyzes the acquired data in real-time, and directly governs settings of the aVNS. (2) "***Design of a Low Power and Robust VLSI Power Line Interference Canceler with Optimized Arithmetic Operators***" – This work proposes a low power dissipation VLSI hardware architecture for a robust power line interference canceling (PLIC) in biopotential signals. The designed circuit effectively suppresses interferences in ECG (Electrocardiogram), EEG (Electroencephalogram), EMG (Electromyogram), and EOG (Electrooculogram) signals.
- Computer Architecture. (1) "***Sharing SIMD Execution Units with Decoupled Offloader in Asymmetric Multicores***" – This work proposes a decoupled offloading mechanism for asymmetric multicore architectures (e.g., ARM big.LITTLE), allowing the big core to use such power-efficient Execution Units (EU) in the little core while its own can be power-gated, maintaining the original migration transparency of the architecture. Results show that, on average, the proposed approach provides 16.9% in energy and 16.4% Energy-Delay Product (EDP) improvements at the cost of 0.6% in time overhead for Mibench benchmarks.

✉ Fernando Gehm Moraes
fernando.moraes@pucrs.br

Bernardo Leite
leite@ufpr.br

[1] Pontifical Catholic University of Rio Grande do Sul - PUCRS, Viamão, Brazil

[2] Federal University of Paraná, Curitiba, Brazil

- Test, verification, and fault-tolerance. (1) "***Automatic Tool for Test Set Generation and DfT Assessment in Analog Circuits***" – This work presents a low-cost automatic test generation tool for structural analog testing. With the spice netlist and technology models of the circuit to be tested, a fault list is generated, considering a defect modeling provided by the user. (2) "***A Current Limiter for Satellite Power Protection***"– The paper presents the design of Latching Current Limiters (LCL) used in DC power distribution systems to isolate faults and protect satellite payloads. The presented LCL topology is a PMOS Power Transistor (PT) associated with a control circuit, which allows the adjustment of the limiting current and sets the trip-off time.

We hope that you enjoy these contributions as much as we did.

Fernando Gehm Moraes SBCCI Program Chair, Leading Guest Editor. Received the Electrical Engineering and M.Sc. degrees from the Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, in 1987 and 1990, respectively. In 1994 he received the Ph.D. degree from the Laboratoire d´Informatique, Robotique et Microélectronique de Montpellier (LIRMM), France. He is currently at PUCRS, where he has been an Associate Professor from 1996 to 2002 and Professor since 2002. From 1998 to 2000, he joined the LIRMM as an Invited Professor for three months each year. He has authored and co-authored 49 peer-refereed journal articles in the field of VLSI design, including the development of networks-on-chip and telecommunication circuits. He has also authored and co-authored more than 200 conference papers on these topics. He advised 30 MSc, and 16 Ph.D. works. His primary research interests include Microelectronics, reconfigurable architectures, NoCs and MPSoCs (multiprocessor system on chip), and security. IEEE Senior Member.

Bernardo Leite SBCCI Publication Chair, Guest Editor. Received the electrical engineering degree at Universidade Federal do Paraná (UFPR) in Curitiba, Brazil, the M. Sc. degree in electronic engineering at ENSEIRB, in Talence, France, and the Ph.D. degree in electronics at the University of Bordeaux, France. From 2007 to 2012, he was a researcher within the STMicroelectronics-IMS Bordeaux joint laboratory and, since 2012, Bernardo Leite has been a professor at UFPR and a member of the Group of Integrated Circuits and Systems (GICS). His research activities focus on the design of radiofrequency and millimeter-wave CMOS power amplifiers and on-chip transformers.