# A CMOS RF energy harvester with high PCE over a wide range of input power

Keyvan Farhang Razi[1] · Mohsen Moezzi[1]

## Abstract

In this Paper, an RF energy harvesting system in 0.18 $\mu$m CMOS Technology is proposed in which a novel adjustable rectifier has been employed. Due to the fact that the optimum number of stages in a multi-stage rectifier structure of a harvester largely relies upon the power of incident RF signal, the presented rectifier is capable of tuning its number of stages with respect to input power variation so as to prevent power conversion efficiency (PCE) degradation. Therefore, the harvester's rectifier is of optimum number of stages incessantly which leads to a PCE close to maximum over a wide input power range. The number of rectifier's stages in the proposed circuit, which operates at 915 MHz ISM-band, alters from three to seven stages when input power variation takes place. The maximum PCE of the circuit is 28.9% at input power of − 20 dBm when it drives 1 M$\Omega$ load. The outstanding specification of the proposed circuit is the ability of maintaining its PCE over 80% of maximum PCE in 10.5 dB input RF power range. In addition, the sensitivity of the designed circuit − 24 dBm which demonstrates superiority over previous works.

**Keywords** RF energy harvesting · RF-DC power converter · Conversion efficiency · Adjustable rectifier · Wireless sensor networks · CMOS

## 1 Introduction

Nowadays, energy harvesting is getting remarkable attention due to a rapid growing need for non-stop operation of portable electronic devices and replacing traditional batteries in various applications. In addition, applying energy harvesting techniques to supply power for biomedical implanted systems and wireless sensor networks used in internet-of-things applications are considered as appealing goals for researchers [1]. When it comes to low-power and low-cost energy harvesting, RF energy harvesting exhibits its superiority over other available ambient sources such as thermal, vibration and solar energy [2–5].

The block diagram of a conventional RF energy harvesting system is depicted in Fig. 1. The first block is an antenna which receives the incident RF signal in particular frequency band. The second block is impedance matching network that is in charge of maximizing the power transferred from the antenna to power conversion unit. The next block is RF-DC power conversion unit which rectifies RF signals. This section includes a multi-stage rectifier which is formed by cascading multiple rectifier's units. Rectifiers can be classified into single-ended and differential rectifiers [6, 7]. Although differential rectifiers inherently have higher conversion efficiency compared to single-ended rectifiers, they impose using balun or differential antennas which are not desirable for many RF energy harvesting applications [8]. The energy storage part consists a large capacitor or rechargeable battery which is followed by the load.

Sensitivity, power conversion efficiency, generated output DC voltage and input power range, in which the harvester can operate properly, are regarded as critical parameters to evaluate the performance of RF energy harvesting circuits. The harvester's performance is affected by the low amplitude of input RF signal, the threshold voltage and reverse leakage current of rectifying devices as well as unexpected fluctuations in the amplitude of received RF signals.

Indeed, the strength of an electromagnetic wave is extremely attenuated as the distance between the wave's

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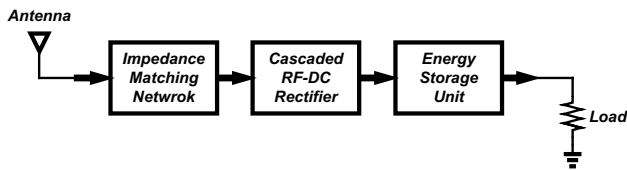
**Fig. 1** The block diagram of a conventional RF energy harvesting system

source and the receiver's antenna increases in both free space and indoor propagations [9]. Plus, the maximum allowed transmit output power fed into an antenna is 1 Watt in ISM band which is regulated by FCC rules. On the other hand, the amplitude of RF signal at the input of rectification stage must be sufficiently large to provide adequate overdrive voltage for the appropriate operation of MOS transistors in rectification chain. Hence, the threshold voltage of rectifying devices plays a pivotal role in the sensitivity of the energy harvesting system [10]. Extensive researches have been carried out to reduce or entirely cancel the threshold voltage of rectifying devices by employing technology-based [1, 9, 11, 12] or circuit-based approaches [10, 13–16].

The crucial issue which is not fully addressed in the literature is that the power of incident RF signal cannot be predicted accurately in practical applications and power variation of incident RF signal can contribute to unfavorable influences on the overall performance of the energy harvesting circuits. Single-ended rectifiers used in [10, 13, 16] can maintain their highest PCE within a narrow range of the incident RF power and the efficiency of the harvester will be drastically degraded when the input power varies from its optimum point. Reference [17] used auxiliary transistors to generate a relatively constant threshold compensation voltage for MOS transistors in rectification chain which is independent to input power variation and it leads to higher PCE over wider input power range. The drawback of the rectifier used in [17] is that the input range in which the PCE is higher than 80% of maximum PCE is not remarkably wide.

In this paper, an RF Energy harvesting system is proposed which includes an adjustable multi-stage rectifier with respect to input power level. The suggested rectifier is also able to modify the configuration of the last transistor connected to the load with respect to input power by changing its threshold voltage compensation level from one to zero so as to reduce the leakage loss and enhance the overall efficiency.

The paper is organized as follows. Section 2 presents the concept of rectification in energy harvesting systems by describing a full-wave Dickson rectifier as well as the constructive role of employing multi-stage Dickson-based CMOS rectifier to attain high output DC voltage. Furthermore, the self-threshold voltage compensation method and
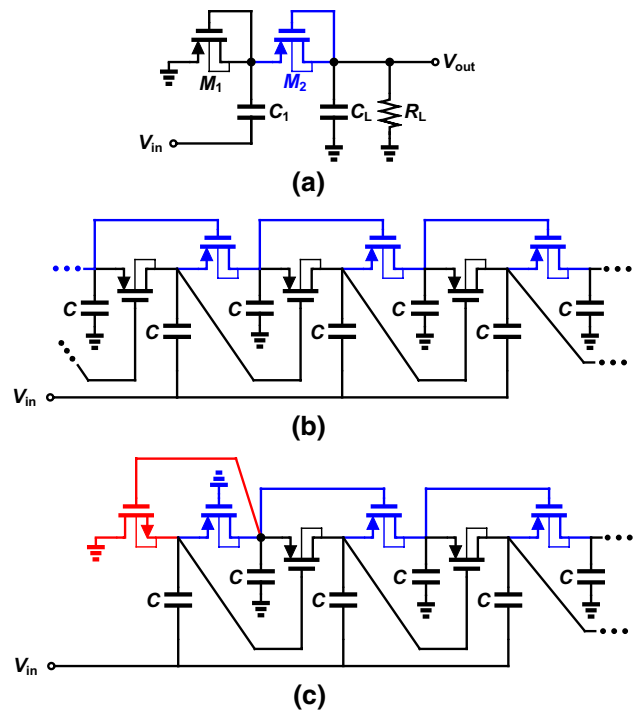


**Fig. 2** **a** PMOS Full-wave Dickson rectifier unit. **b** Multi stage rectifier with level-1 threshold compensation. **c** Multi stage Dickson rectifier with level-1 forward and backward threshold voltage compensation

harvester's loss are studied in this section. The proposed RF energy harvesting system which contains an efficient adjustable rectifier and exhibits high PCE over wide input power range is explained in Sect. 3, followed by demonstrating simulation outcomes of the proposed harvester in Sect. 4. Section 5 concludes the paper.

## 2 Basic concepts in RF energy harvesting

The ability of converting low-amplitude incident RF signals to a desirable DC voltage with high power conversion efficiency is of utmost importance in designing a RF energy harvester. In this section, the architecture of a basic Dickson rectifier along with the cascade configuration of multiple rectifiers, which are suitable for generating high DC voltage, is studied. Furthermore, the influence of body effect correspondence to power loss of rectification unit is briefly discussed in this section.

### 2.1 Analysis of rectifier unit

Fig. 2(a) shows the schematic of a full-wave rectifier using PMOS transistors. The output voltage of PMOS full-wave Dickson rectifier in steady state can be calculated as

$$V_{out} = 2V_P - |V_{th1}| - |V_{th2}| \tag{1}$$

where, $V_P$ is amplitude of input signal, $|V_{th1}|$ and $|V_{th2}|$ are threshold voltage of $M_1$ and $M_2$ transistors, respectively.

MOS transistors in full-wave rectifiers are turned on and off periodically. In order to reduce voltage drop and loss of rectifying devices, it is desirable to have low threshold voltage for transistors when they are conducting, and high threshold voltage when they are switched off. To actualize this target, the bulks of transistors are connected to drain terminal rather than source terminal and it is also shown in Fig. 2(a) [10].

In negative phase of input, $M_1$ is conducting and $M_2$ is in reverse leakage region. In this period, capacitor $C$ starts to be charged by the current flows through transistor $M_1$. In this condition, the bulk of $M_1$ is connected to the terminal which is of the lower voltage compared to the source terminal. Consequently, by increasing the source-body voltage of transistor, the threshold voltage is lowered when the PMOS transistor is conducting.

It is noteworthy that the aforementioned method for PCE enhancement by connecting bulk of transistors to the drain terminal imposes the constraint of employing PMOS transistors due to the fact that all NMOS transistors have a same p-type substrate and they cannot be individually biased in standard CMOS technology.

## 2.2 Cascaded RF-DC conversion unit

In order to obtain high output DC voltage, it is indispensable to employ a multi-stage rectifier since the incident RF power in energy harvesting applications is excessively low. PMOS Multi-stage rectifier topology is preferable on the grounds that its individual body biasing eliminates the undesirable impact of threshold voltage increment. The schematic of a PMOS multi-stage Dickson based rectifier is illustrated in Fig. 2(b).

Although applying the multi-stage approach enables designers to achieve higher output DC voltage in RF energy harvesting applications, the PCE of this method is still low and self-threshold voltage compensation technique must be used to improve PCE of the energy scavenger [13]. In this method, the gate of a PMOS transistor is connected to the output of previous stages in rectification chain instead of its drain terminal to provide negative compensation voltage. This is called backward threshold voltage compensation.

Fig. 2(c) exhibits a multi-stage rectifier with level-one forward and backward threshold voltage compensation. As it shown , in level-one threshold voltage compensation, the first transistors should be NMOS with forward threshold compensation; otherwise, the first PMOS transistor will be left uncompensated or a dummy stage must be added to the circuit which results in PCE degradation.

## 2.3 Power loss of transistors

Transistor in a full-wave Dickson rectifier operates in three operational regions; subthreshold, inversion and reverse leakage region. Loss in subthreshold region of transistors can be ignored due to its short time interval and rather low current amplitude which passes through transistors in this region. Hence, the loss of a transistor in a full-wave rectifier topology is derived as

$$P_{loss} = P_{inversion} + P_{leakage} \tag{2}$$

where, $P_{inversion}$ and $P_{leakage}$ are loss of a transistor in inversion and leakage region, respectively.

In a k-stage rectifier, 2k transistors are cascaded and total power loss of the circuit is expressed as

$$P_{loss-total} = 2kP_{loss} \tag{3}$$

The power conversion efficiency (PCE) of the circuit is defined as the ratio of DC power generated at load to the incident RF power and it is stated as

$$PCE = \frac{P_{load}}{P_{RF,in}} = \frac{P_{load}}{P_{load} + P_{loss-total}} \tag{4}$$

It should be noted that increasing level of compensation is not tantamount to PCE improvement due to the fact that reducing conduction loss of a transistor causes an increase in reverse leakage current and leakage loss. So, designers are encountered with a crucial trade-off finding the optimum level of compensation.

# 3 Proposed RF-DC power conversion circuit

## 3.1 Rectifier with adjustable number of stages

In conventional rectifiers which have a fixed number of rectifier's stages, the PCE is highly dependent to the input power. As a general trend, in low input power range, an increase in input power leads to higher output voltage and PCE of the rectifier with respect to the negligible amount of transistors' leakage. On the other hand, in high input power range, when the input power increases, the leakage current of transistors starts playing a critical role which brings about PCE degradation. As a result, the maximum PCE is obtained at the certain value of input power.

The PCE of rectifiers with fixed number of stages and hybrid threshold-voltage compensation versus input power is illustrated in Fig. 3(a). As it can be viewed, as input power increases, initially the PCE of a rectifier with a fixed number of stages increases until it reaches the maximum value; afterward, the adverse impact of increasing transistors' leakage loss will be dominated and results in PCE
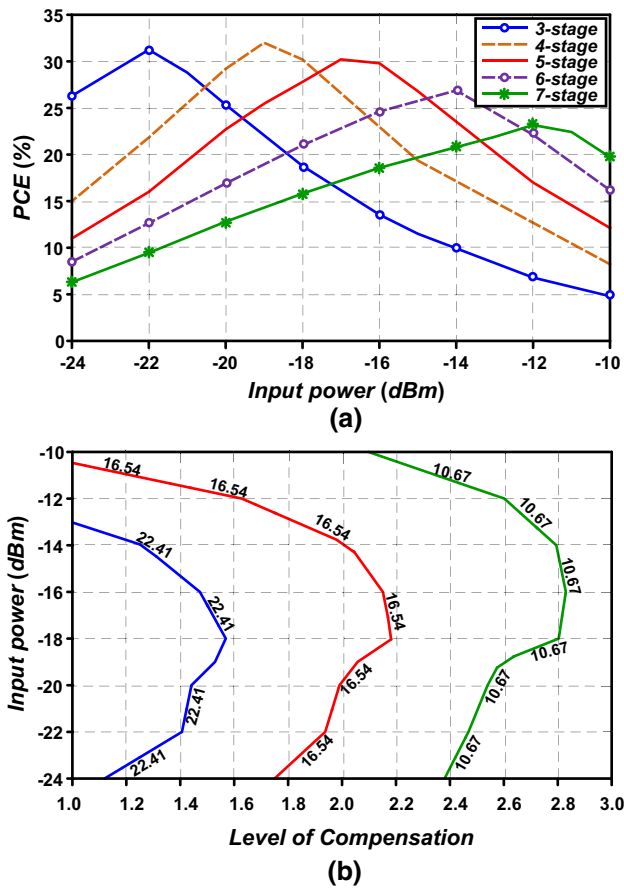
**Fig. 3** **a** Power conversion efficiency of multi-stage rectifiers versus input power. **b** Contour plot of constant PCE versus input power and level of compensation

degradation. Therefore, conventional multi-stage rectifiers are unable to maintain high PCE over a wide range of input power. Moreover, for each rectifier, the maximum PCE is obtained at different input power level. Thus, in practical RF energy harvesting applications where the available input power will experience unpredictable amplitude variation, the conventional RF-DC converters' performance are affected dramatically.

To address the aforementioned issue, a novel adjustable rectifier is presented and its architecture is shown in Fig. 4.
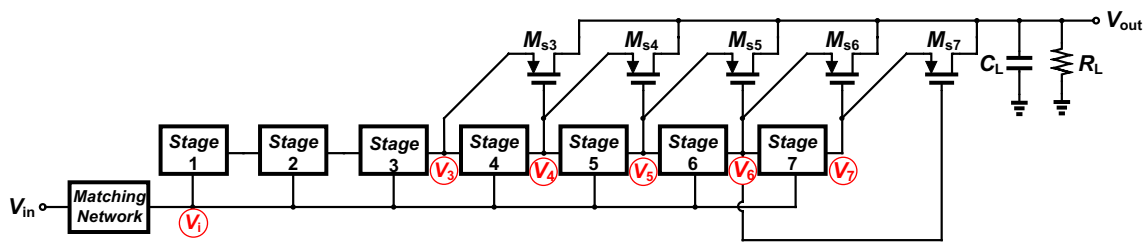
The proposed rectifier consists both fixed and variable stages. The first three stages are regarded as fixed stages and the next four stages are considered as variable stages. In this circuit, control switches denoted as $M_{s3}$-$M_{s7}$ are placed at the output of last five stages so as to adjust the number of rectifier's stages with respect to input power. These MOS switches are in charge of detecting the highest voltage among the output of the last five stages and adjust the number of the rectifier's stage with the aim of achieving the highest possible PCE.

As an illustration, it can be seen in Fig. 3(a) that when input power is − 22 dBm, the three-stage rectifier has the highest PCE. Furthermore, the simulation result shows that the output of the third stage ($V_3$) is the highest voltage among all stages' output voltage (i.e. $V_4$ to $V_7$). In the proposed architecture, the $M_{s3}$ switch, which its source is connected to $V_3$ and its drain is connected to $V_4$, will conduct and the output of the third stage is connected to the load. In this condition, the subsequent stages (stage-4 to stage-7) will be bypassed. It should be noted that, when $M_{s3}$ is ON, the voltage difference between the output of subsequent stages are not large enough to turn on the other switches.

Moreover, when the input power gets greater from − 22 to − 19 dBm, $V_4$ has the highest voltage among all nodes in the proposed circuit. Therefore, $M_{s3}$ will be turned off and $M_{s4}$ begins conducting and connecting the output of the fourth stage to the load and the succeeding stages will be bypassed. Likewise, the same procedure will occur for the other input power levels. As a consequence, the proposed RF-DC converter is capable of acquiring the optimum number of stages with respect to the input power so as to attain high RF-DC conversion efficiency over a wide range of input power. The proposed architecture is beneficial in powering sensors in wireless sensor networks in which the RF incident power is not fully foreseeable.

## 3.2 Change the last transistor configuration

It was indicated in the previous sections that the threshold voltage of transistors used in rectification chain plays a significant role in performance of RF energy harvesting systems. A critical compromise between harvester sensitivity
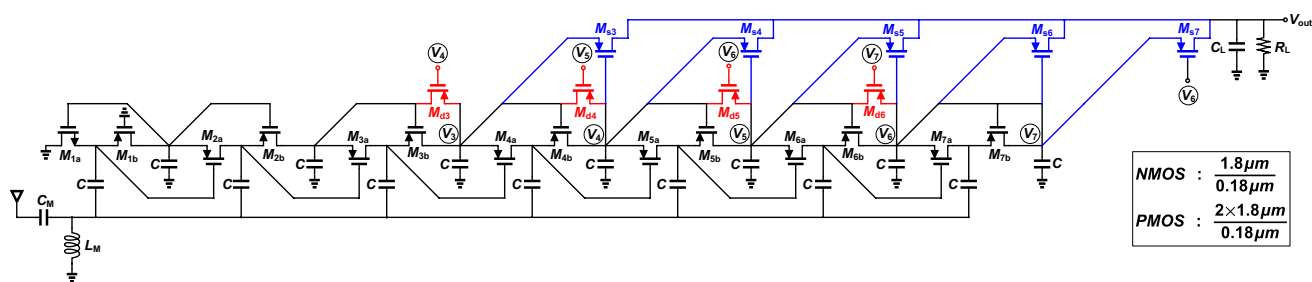


**Fig. 4** The structure of the proposed multi-stage adjustable rectifier

**Fig. 5** Circuit implementation of the proposed RF energy harvester system

and transistors' leakage loss exists when it comes to determining the level of threshold voltage compensation. A low threshold voltage is required for a better sensitivity, while the lower threshold voltage results in the higher reverse leakage current and higher loss in reverse operation region of transistors.

Thus, the contour plot of constant efficiency versus incident RF power and level of compensation is depicted in Fig. 3(b) with the aim of determining the optimum level of threshold voltage compensation. As it shown in Fig. 3(b), the level-1 compensation, which means connecting the gate of PMOS transistors to the source of one previous transistor instead of connecting to their own drain terminal, contributes to the better efficiency compared to the other threshold voltage compensation levels. In addition, provided that the last transistor of the rectifier is left uncompensated, the output capacitor charge leakage will be reduced [16].

As it described in Sect. 3.1, in the proposed novel adjustable rectifier, the number of stages varies dynamically when RF input power alters. Consequently, the last transistor of the rectification chain is changed. Hence, PMOS transistors $M_{d3}$ to $M_{d6}$ are employed to modify the compensation configuration of the last transistor from level-one to diode connected scheme. This approach is illustrated in Fig. 5.

For instance, when the RF input power is − 22 dBm, $V_3$ is higher than $V_4$. Hence, $M_{s3}$ will be turned on and the number of effective stages of the proposed rectifier is three. In this circumstance, $M_{d3}$ transforms the configuration of $M_{3b}$ from level-one back compensation to diode-connected configuration.

## 4 Simulation results

The proposed RF-DC converter, shown in Fig. 5 is implemented in standard 0.18 $\mu$m CMOS technology. The power conversion efficiency and output DC voltage of proposed rectifier in TT, FF and SS corner cases are depicted in Fig. 6. As it can be seen, the designed circuit is able to maintain its PCE relatively close to the maximum PCE of the circuit over wide range of input power thanks to the
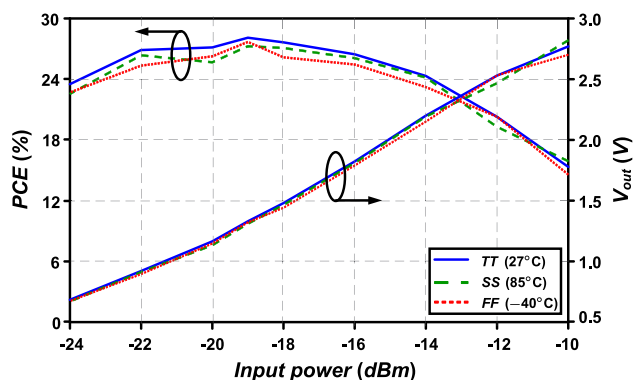


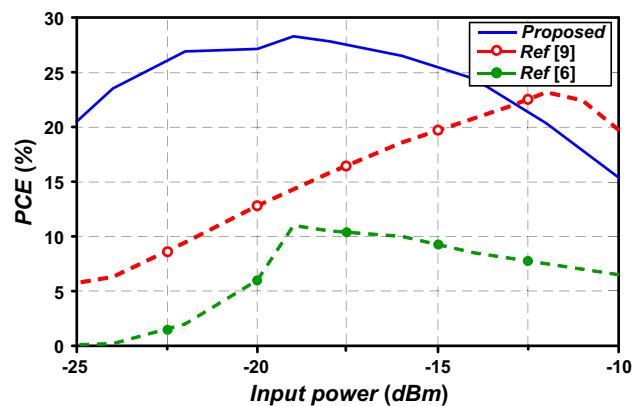**Fig. 6** PCE and output DC voltage of the proposed RF-DC convertor in corner cases



**Fig. 7** PCE comparison of the proposed and conventional RF-DC convertors

novel topology of rectifier in which the number of rectifier stages is dynamically adjusted with respect to the input RF power.

Fig. 7 compares the PCE of the proposed circuit with that of the structures reported in [13] and [16] in which threshold voltage compensation techniques have been utilized. As it can be seen , the proposed harvester exhibits higher PCE in a wide range of input power compared to those structures.

**Table 1** The effective number of stages of the proposed structure in terms of input power

| Input power (dBm) | − 10 | − 14 | − 16 | − 18 | − 22 | − 24 |
|---|---|---|---|---|---|---|
| Effective number of stages | 7 | 7 | 6 | 5 | 4 | 3 |
| Output voltage (V) | 2.77 | 2.2 | 1.823 | 1.48 | 0.921 | 0.684 |

Table 1 indicates that $M_{s3} - M_{s7}$ and $M_{d3} - M_{d7}$ can successfully modify the architecture of the proposed rectifier to dynamically adopt the optimum number of rectifier's stages as input power varies in a wide input power range.

It is noteworthy that the impedance matching circuit is designed in this work to ensure a full match between the input impedance of the proposed rectifier and the antenna's impedance. The impedance matching network in this circuit is a L-section matching network with an inductor and a capacitor which is shown in Fig. 5. The L-section impedance matching network is in charge of maximizing the power transfered from the antenna to the presented rectifier as well as providing a passive voltage amplification to enhance the voltage amplitude of the received signal at frequency of 915 MHz.

The performance of the proposed RF energy harvesting circuit is summarized and compared with previously published works in Table 2. The significant characteristic of the designed harvester is having PCE above 0.8PCE$_{max}$ in 10.5 dB input power range which outperforms all mentioned references in Table 2. Furthermore, in this work, a higher maximum PCE in addition to wider PCE range is also obtained in comparison with [13, 16, 18]. The performance of the proposed harvester in terms of sensitivity is better than all references which are mentioned in Table 2.

# 5 Conclusion

In this work, a wide-range power-efficient RF-DC power converter has been implemented to be utilized in RF energy scavenging applications. Auxiliary controlled transistors are employed in the proposed rectifier's topology to adjust the number of rectifier's stages and limit the output leakage current with respect to input power. In this approach, the number of rectifier's stages varies between three to seven which enables the harvester to have a rectifier with optimum number of stages in a wide range of input power. In other words, the harvester is protected against undesirable PCE degradation which originates from unwanted RF power variation that is commonplace in most of RF-powered devices.

Additionally, controlled PMOS transistors are used to identify and simultaneously transform the last transistor in rectification chain from level-1 compensation to diode-connected topology under different RF power conditions. As a result, the critical trade-off between threshold voltage compensation and reverse leakage current is successfully considered which enables the harvester to maintain its PCE higher than 80% of the PCE$_{max}$ in 10.5 dB input power range.

**Table 2** Performance summary of the proposed RF-DC converter

| Ref. | [10] | [13] | [16] | [18] | This work |
|---|---|---|---|---|---|
| Technology | 130 nm | 90 nm | 130 nm | 90 nm | 180 nm |
| Additional | Aux. | Tripple | – | Tripple | Aux. |
| Requirement | Transistors | Well | | Well | Transistors |
| Frequency (MHz) | 915 | 915 | 915 | 868 | 915 |
| Input Power Range (dB)[a] | 5.5 | 4 | 4.5 | 6.5 | 10.5 |
| Sensitivity (dBm) | − 20.5 | − 18.8 | − 21 | − 23 | − 24 |
| Maximum PCE | 32% | 11% | 22.6% | 24% | 28.9% |
| (@ P$_{in}$) | (− 15 dBm) | (− 19 dBm) | (− 17 dBm) | (− 21 dBm) | (− 22 dBm) |

[a] Input power range in which PCE ≥ 0.8 PCE$_{max}$

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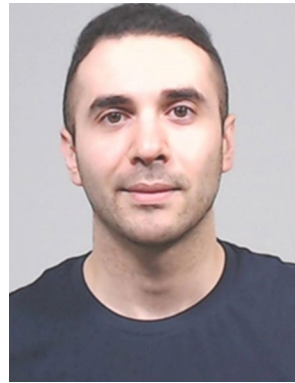
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