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An ultra-low-power CMOS smart temperature sensor based on frequency to digital conversion

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Abstract
The smart temperature sensor measures the room temperature and converts it to the digital domain, thus making it easier to process and store data. This work presents a fully integrated smart temperature sensor implemented in a 180 nm CMOS technology suitable for low voltage and ultra-low power electronic applications. The designed circuit uses a frequency to digital conversion topology, in which the frequency of an internal signal is linearly dependent on the room temperature. The minimum supply voltage for the designed circuit is only 0.5 V, while the occupied silicon area is 0.04 mm^2. By employing a simple frequency doubler circuit and proper circuit topologies, a very low power consumption of 19 nW for a sampling frequency of 100 Hz at 27 °C is achieved. Moreover, the sensor consumes nominally 190 pJ per conversion. The simulated inaccuracy using nominal (TT) transistor models is lower than 0.5 °C over a wide temperature range of − 30 °C to 100 °C. Preliminary silicon data shows the functionality of the design circuit. Additionally, the effects of the external clock signal temperature coefficient on the performance of the designed circuit were discussed, and a correction method was proposed.

Keywords Temperature sensor · Low-power · FDC · Wireless sensor node

1 Introduction

Temperature sensors (TS) are employed in numerous applications, for instance, environmental monitoring, transporting perishable goods, or precision agriculture. Even when other physical quantities are measured (*e.g.*, gas monitoring), the temperature measurement becomes necessary for compensating temperature-related errors.

When the TS is used in Wireless Sensor Networks (WSNs), as shown in Fig. 1, it is desirable to provide the output signal in a digital format to allow direct communication with the low power transmitter or the local low power microcontroller. In this case, the sensing capability and the electronic interface are combined in a single chip, and then, it is commonly referred as Smart Temperature Sensor (STS). Moderate accuracy of ± 1 °C is usually adequate for many of these applications, while low supply voltage and ultra-low power operation (*e.g.*, < 100 nW) may be mandatory. These systems commonly depend on limited battery size and/or energy harvesters, while operating for long periods.

For the above scenario, high precision, and power-hungry analog-to-digital converters (ADCs) are frequently avoided [1]. Thus, temperature sensors based on the time-domain approach are preferred over the voltage/current domain approach using ADCs. In the time-domain STS, the temperature information can be expressed in terms of the delay, duty cycle, or frequency before being converted to a digital code. The last one is called STS based on Frequency to Digital Conversion (FDC).

Several STS devices using an FDC topology have been proposed [1–5]. Although [1–4] present great performance, their minimum supply voltages, of around 1.1 V, make them impossible to be used in applications that require very low VDD. Work [5] operates with a minimum supply voltage of 0.5 V with a very low silicon area, but consumes 8.8 µW, which is too much for systems that need to operate with energy harvesting [6]. Moreover, its very low silicon area is achieved by using a switched capacitor current reference that requires a high-frequency signal of 10 MHz.

In [7], the authors presented a fully CMOS integrated STS with low supply voltage operation (< 1 V),

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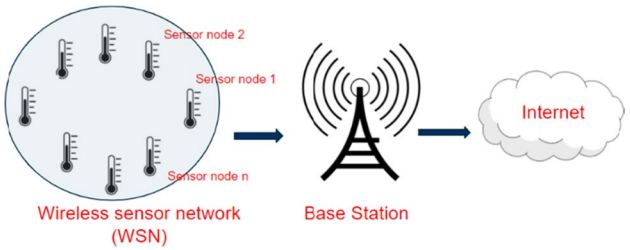

Fig. 1 Temperature sensors used in a wireless sensor network

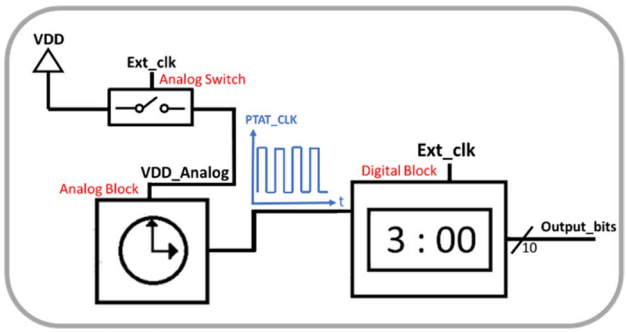

Fig. 2 A top-level view of the smart temperature sensor

ultra-low power consumption (nW), and moderate accuracy (~ ± 1 °C). The chosen circuit topology in [7] is based on [8], but modifications were proposed to allow ultra-low power consumption while still achieving moderate accuracy. Among the performed optimizations, the principal ones are: (i) the use of a simple frequency doubler gate that saves power and improves linearity, (ii) use of power gating technique to turn off the analog part of the sensor whenever possible, and (iii) use of non-conventional flip-flop architecture to save power in the digital block.

This article extends the author´s previous work [7], including new results and investigations summarized below:

- A design exploration demonstrating the performance benefits of the inclusion of the frequency doubler (Section 3),
- A Monte Carlo Analysis to check the robustness of the designed STS against the fabrication process effects (Section 5),
- An investigation of the temperature coefficient external clock impact on the performance of the proposed circuit, and its correction method (Section VI),
- Preliminary silicon results (Section 8),
- The inclusion of architecture details, for example, inverter buffers and parallel-to-serial converter (Sections 2.4 and 2.8),
- Additional simulation results in Section 4.

This paper is organized as follows. Section 2 presents the architecture of the proposed STS. Section 3 and 4 show the Pre-Layout and Post-Layout simulation results. Monte Carlo analysis is presented in Section 5. An investigation of the temperature coefficient of the external clock signal on the performance of the STS is presented in Section 6. The Silicon results are shown in Section 7 and the comparison of this paper with related works is on Section 8. Finally, conclusions are in Section 9.

2 Designed STS

2.1 Top view

The STS, shown in Fig. 2, is composed of two sub-blocks: the analog and the digital one. The analog part is responsible for sensing the temperature and generating a square wave signal, called PTAT_CLK, whose frequency is linearly Proportional To Absolute Temperature (PTAT). The digital block converts the square wave signal into a digital output of 10 bits using a low power counter. Furthermore, a simple CMOS switch is also used to turn off the analog part whenever possible to save power.

A simplified view of the analog block is shown in Fig. 3. It is composed of: (i) temperature sensor, (ii) voltage oscillator, and (iii) frequency doubler.

The temperature sensor, called just "sensor" in Fig. 3, generates an output current (I_{PTAT}) that is linearly proportional to the absolute temperature (PTAT). I_{PTAT} is then injected in the ring-oscillator that generates a square wave output voltage also PTAT, called PTAT_CLK_before. Finally, the frequency doubler just multiplies the frequency of this signal by a factor of two, then producing a voltage called PTAT_CLK.

A simplified view of the digital block is shown in Fig. 4. It is mainly composed of a digital counter, flush counter, and output register. The 10-bits counter is responsible for converting the analog input coming from the analog block into a digital code, playing the role of an ADC. The flush counter is necessary to reset the counter by the end of one conversion cycle. Therefore, this block is activated after EXT_CLK goes to 0, indicating that the counting has ended. And finally, the output register stores each bit of the digital word during the data conversion.

2.2 Temperature sensor

Figure 5 shows the schematic diagram of the temperature sensor. It is simply a constant g_m-bias circuit with additional

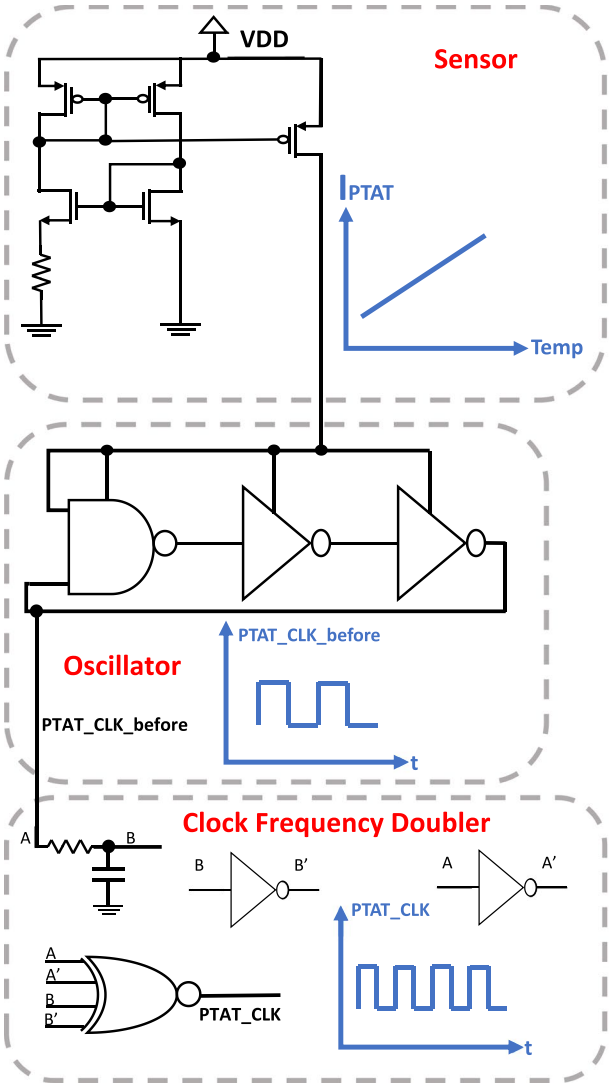

Fig. 3 The analog block of the STS

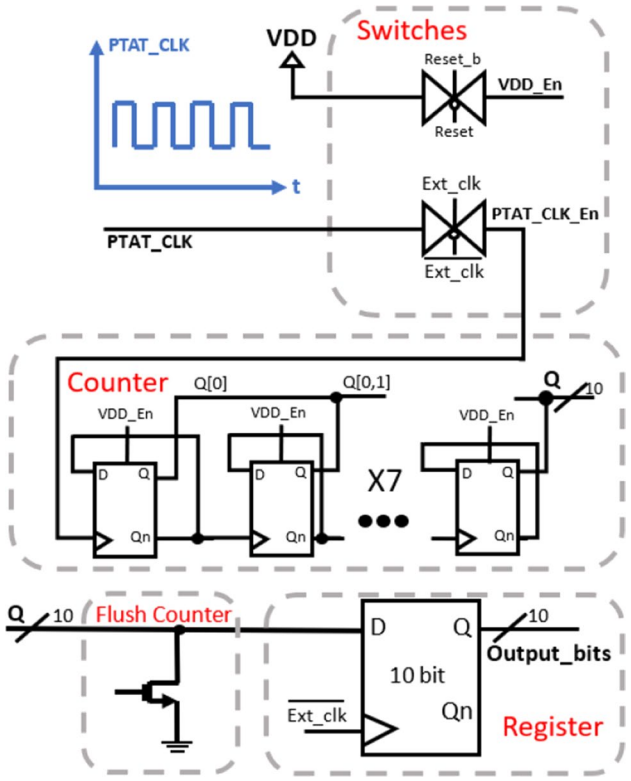

Fig. 4 The digital block of the STS

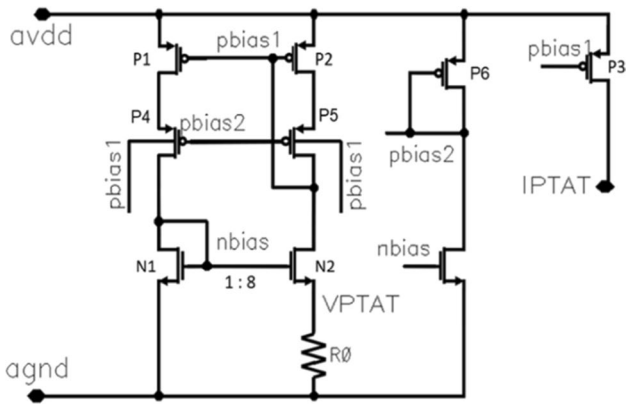

Fig. 5 Sensor schematic circuit

P4 and P5 devices to decrease the effect of supply voltage variation on the output current. The inclusion of the cascode devices was needed to guarantee accurate I_{PTAT} current for a large range of supply variation (i.e., 0.5–1.8 V). Since the core transistors of the used technology are halo implanted, their output impedance is not high enough, even when the device is designed with a large length. The operation of the sensor is summarized below.

First of all, consider that the drain-source current (I_{DS}) of an NMOSFET working in subthreshold mode and saturation (*i.e.*, $V_{ds} > 4\ U_T$) is approximately given by Eqs. (1) and (2) [10]:

$$I_{DS} \approx I_0 \times e^{\frac{(V_{GS}-V_{TH})}{n \times U_T}} \tag{1}$$

$$I_0 = \mu_n \times C_{OX} \times \frac{W}{L} \times (n-1) \times U_T^2 \tag{2}$$

where V_{GS} is the gate-source voltage, Vth is the threshold voltage, Cox is the oxide capacitance, W and L are the width and length of the transistor, μn is the electron mobility on NMOS device, UT is the thermal voltage, and η is the gate coupling coefficient on the threshold region. The thermal voltage is given by κ·T/q, and equal to about 25 mV at 300 K. Therefore, isolating V_{GS} in Eq. (1), Eq. (3) is obtained:

$$V_{GS} = n \times U_T \times ln\left(\frac{I_{DS}}{I_O}\right) + V_{TH} \quad (3)$$

Secondly, consider that devices P1 and P2 are equal, and that N1 and N2 have the same W/L, but different multiplicities. There is just one instance of N1, but 8 (named "x") instances of N2. Due to the positive feedback loop presented in the circuit, the difference between the gate-source voltage (ΔV_{GS}) of N1 and N2 appears across resistance R_0 and is described by (4):

$$V_{PTAT} = \Delta V_{GS} = V_{GS1} - V_{GS2} = n \times U_T \times ln(x) \quad (4)$$

Note that Eq. (4) neglects the body effect of N2. Note also that the voltage across the resistor, called V_{PTAT}, is directly proportional to U_T, and then it is directly proportional to the absolute temperature. Consequently, the generated current in the resistor R0 with resistance R is given by (5) and is also a PTAT quantity.

$$I_{PTAT} = V_{PTAT}/R \quad (5)$$

To achieve low power consumption, R must have a high value, which leads to a large silicon area. In this project, a P + poly resistor of 4.6 MΩ with a silicon area of 132 µm × 88 µm. The negative temperature coefficient of the p-poly resistor (*i.e.* ~800 ppm/°C) slightly increases the overall positive temperature coefficient (TC) of Eq. (5). An N-well diffusion resistor would offer high sheet resistance, but it was avoided because of its inherent non-linearity that would reduce the sensor linearity.

The n-well terminals of P1, P2, P3 and P6 are connected to the supply voltage. The n-well connections of P4 and P5 were connected to the voltage pbias1 to slightly reduce the value of the V_{TH} voltage, therefore making it easier to keep these transistors in saturation over corner process variations. The connection between the n-well and drain terminal does not affect the linearity of I_{PTAT}. Linearity is not affected because P4 and P5 are cascode devices, and their influence is mainly the reduction of the channel length modulation effect in P1 and P2 transistors caused by variations in the supply voltage.

The sensor circuit of Fig. 5 can be adequately designed to be robust against the fabrication process effects. The P3 transistor can be designed as a few transistors with CMOS switches connecting them in parallel and digital inputs to select the desired connections. The parallel transistors can have their width dimensions with a binary-weighted distribution. Using this strategy, the average value of I_{PTAT}, proportional to the equivalent width of the P3 transistor in the fabricated circuit, can be appropriately increased or decreased to compensate for the resistor tolerance.

2.3 Oscillator and clock frequency doubler

As can be seen in Figs. 2 and 3, the current generated in the sensor block is mirrored to supply a starved-current ring oscillator. The starved-current topology is ideal when low power consumption is desirable. There is a linear dependence between the supply current (I_{PTAT}) and its oscillation frequency. This relationship can be analyzed based on the formula that describes the current in a capacitor as a function of its voltage, given by Eq. (6).

$$I = CdV/dt \quad (6)$$

where C represents the capacitance value, which, in this case, refers to the intrinsic capacitances of the PMOS and NMOS transistors used in the logic gates of this oscillator. Since these capacitances are approximately constant, the greater the current I, the greater the variation of the voltage at the capacitor nodes (dV/dt), these nodes being the inputs and outputs of the logic gates. Since the voltages at the output nodes of the logic gates always have the same minimum and maximum voltage levels (0 V and 500 mV, respectively), an increase in the dV/dt variation rate necessarily implies an increase in the clock pulse frequency generated on this oscillator's output. Therefore, there is a linear conversion between the PTAT current at the oscillator's supply input into a clock pulse with PTAT frequency at the oscillator's output.

One of the challenges faced when designing the oscillator, responsible for the conversion of the current I_{PTAT} to the PTAT square wave (PTAT_CLK_before), is the linearity and the power consumption trade-off, as will be explained further.

In order to achieve a wide frequency span between the temperature limits (− 30 °C and 100 °C), a wide amplitude span of I_{PTAT} would also be needed. However, the greater the span of the I_{PTAT} amplitude, the greater the non-linearity in the sensor operation. With a large current span, high-order terms, not described by Eq. (4), start to be not negligible. An example of it would be the body effect of N2 transistor. Therefore, the span of I_{PTAT} was minimized and kept within a range to maximize the linearity of the sensor.

Taking into account the information above, a possible and conservative approach to achieve the desired resolution without increasing the span of I_{PTAT} would be keeping a short output frequency span in the oscillator, while increasing the active cycle of the counter. In this way, the counter would be able to perform the required counting and achieve the desired resolution. The sensor resolution is proportional to the number of counts performed.

However, this approach limits the minimum sampling frequency of the STS, and also increases the overall power consumption. A better solution proposed and employed in

this project was to use a digital clock frequency doubler. This circuit doubles the output frequency span without any compromise on linearity. A drawback of this approach is the modification of the waveform duty cycle. Nevertheless, simulation results showed that as long as the duty cycle stayed within the range of 20–80%, no issues were carried for the counter.

While the clock frequency doubler (digital gate) consumes a significant amount of power, the sensor itself (analog circuit) consumes even more. Thus, if the sensor would be designed to achieve the same frequency span without using the frequency doubler, not only the linearity would be worse, but also the total power consumption would be higher. Figure 6 shows the simulation of the frequency doubler circuit.

2.4 Inverter buffers

The starved ring oscillator's driving capability is limited because of its inherently starved operation. Therefore, it was necessary to include a buffer between the output of the ring oscillator and the frequency doubler's input. A simple digital buffer composed of two NOT gates in series could be used for this purpose. However, since a signal phase inversion is not an issue and our design aims to save energy, a single NOT gate was employed. The same buffer was also used in the frequency doubler design.

2.5 Resolution definition

The output voltage of the frequency doubler and its oscillation frequency are called PTAT_CLK and F_{PTAT}, respectively. Equation (7) describes the frequency span, $\Delta F_{PTAT,}$ on the entire temperature range (ΔT) of –30 °C to 100 °C. Similarly, Eq. (8) describes the counting span, ΔC_{OUNT}.

$$\Delta F_{PTAT} = F_{PTAT}(100°\mathrm{C}) - F_{PTAT}(-30°\mathrm{C}) \tag{7}$$

$$\Delta C_{OUNT} = C_{OUNT}(100°\mathrm{C}) - C_{OUNT}(-30°\mathrm{C}) \tag{8}$$

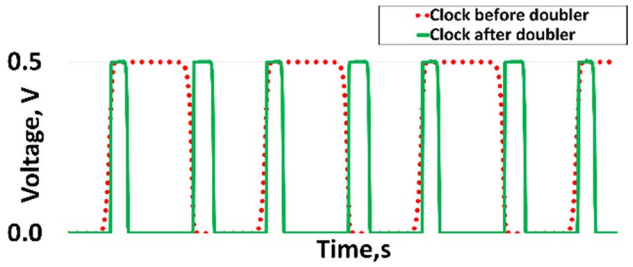

Fig. 6 An operation example of the frequency doubler circuit

The active time of the counter (T_{active}) is defined as (9), where D is the duty cycle, F_S is the external sampling frequency and T_S is the sampling period.

$$T_{active} = \frac{D}{F_S} = D \times T_S \tag{9}$$

The relation between frequency span, counting span, and active time of the counter is given by (10):

$$\Delta F_{PTAT} = \frac{\Delta C_{OUNT}}{T_{active}} \tag{10}$$

Finally, the resolution of the digital output generated by the STS is given by (11). Note that it depends on the external sampling frequency, its duty cycle, and also the frequency span.

$$Resolution = \frac{\Delta T}{\Delta C_{OUNT}} = \frac{130 \times F_S}{\Delta F_{PTAT} \times D} \tag{11}$$

2.6 Counter and register

To reduce the power consumption, the counter and register were carefully designed using a non-conventional Flip-Flop D (FFD) topology shown in Fig. 7. Based on [9], the minimum power consumption of an FFD is achieved if the C2MOS topology is used, a result especially valid for FF corners, for which the power consumption is the highest.

The FFD circuit employs two types of inverters. The first is the conventional one. The second one is clocked, which means it is driven by the CLK and the inverted CLK signals. Thus, the inversion logic is only performed during the high phase of the CLK signal. Please note that since the adjacent clocked inverters are driven by inverted clock cycles, there is no short-circuit condition on this device.

2.7 Operation of the STS

Figures 8 and 9 exemplify the operation of the Smart Temperature Sensor for two different temperature values: – 30 ºC and 100 ºC. The Reset is an internal signal responsible to start a new counting and resetting the counter output. The CLK_Ext is an external signal, with a sampling frequency

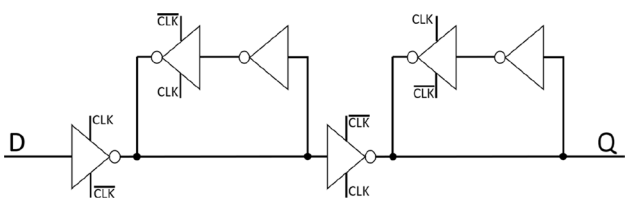

Fig. 7 Schematic of the C2MOS topology FFD circuit

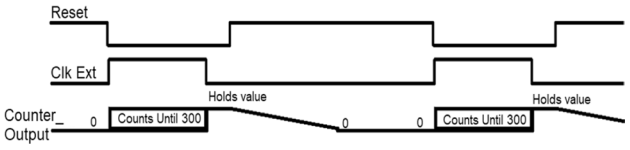

Fig. 8 An operation example of the digital block at − 30 °C

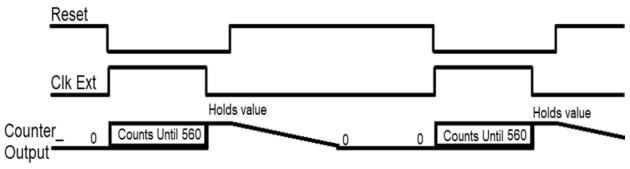

Fig. 9 An operation example of the digital block at 100 °C

F_S, used as a reference during the counting. It means the counting is only performed by the digital circuit during the high state of CLK_Ext. This signal is not generated by the STS circuit. Its nominal frequency is 100 Hz, which is the maximum sampling frequency value that does affect the output counting period, controlled by PTAT_CLK, necessary to guarantee a nominal output resolution of 0.5 ºC.

For the coldest operating region (*i.e.*, − 30 ºC), the counting stops at the value of 300. For the hottest temperature (*i.e.*, 100 ºC) and using the same fixed period of CLK_Ext, the counting takes place until the value of 560. In this way, the resulting delta counting is 260, with a resolution of 0.5 °C, according to Eq. (11).

After the external clock go to logic level zero, the counting is interrupted, and the Reset goes to high state after a short delay. This delay is required to allow the counter output to be loaded into the register. The register, on the other hand, always presents the digital temperature value at its output.

2.8 Parallel-to-serial converter

The designed STS has ten digital outputs (Output_bits in Fig. 4) proportional to the measured temperature. To reduce the number of pins required by the designed sensor, an integrated Parallel-to-Serial Converter, shown in Fig. 10, was used at the output of the STS. The FFDs were implemented using the C2MOS topology [9], and the multiplexer (MUX) circuit topology is shown in Fig. 11.

The operation of the Parallel-to-Serial converter is explained as follows. The load (LD) signal controls the loading process of the ten output bits from the STS into the FFDs input pins. More specifically, the LD signal activates the control input of the MUXs, thus allowing the bit at the input "A" to be loaded in the FFD. After a short period, the

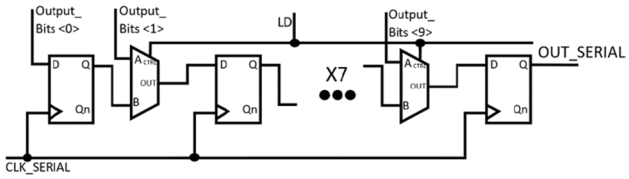

Fig.10 A 10 bits Parallel-to-Serial Converter schematic circuit

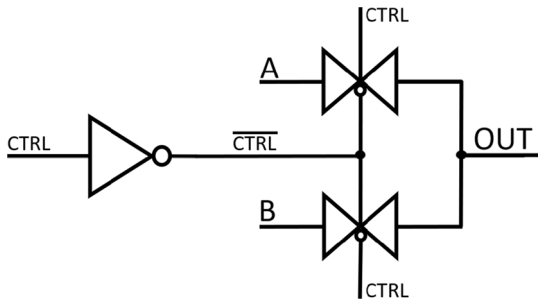

Fig. 11 MUX schematic circuit

signal LD goes to the low level and stays that way until the next pulse of the EXT_CLK signal.

Then, the CLK_SERIAL signal acts as an input clock for all FFDs and propagates the loaded data in each FFD, one by one, to the output pin, called OUT_SERIAL. Finally, all bits (starting with the most significant bit) representing the value counted by the STS device is available at the OUT_SERIAL. The nominal frequency for CLK_SERIAL is 4 kHz.

Finally, the layout of the proposed STS sensor and chip including other circuits are shown in Fig. 12. The occupied area of the STS is 142 µm × 286 µm. The layout of the sensor itself (Fig. 5) was designed using traditional guidelines to ensure the best layout matching, such as common centroid configuration and the inclusion of dummies devices.

3 Pre-layout simulation results

As discussed in Section 2.3, the frequency doubler circuit makes the STS achieve a high-frequency span while presenting a good linearity performance. This approach reduces the operating time for the analog block and reduces the total power consumption.

Note that a higher frequency PTAT_CLK signal leads to a higher count (higher resolution) for a given sampling period. As a design exploration investigation, three versions of the analog block were designed: (i) An Analog block with frequency doubler, (ii) An Analog block without frequency doubler, and (iii) An Adjusted Analog block without frequency doubler. All of them were designed considered the same temperature span. Regarding silicon area, the overhead

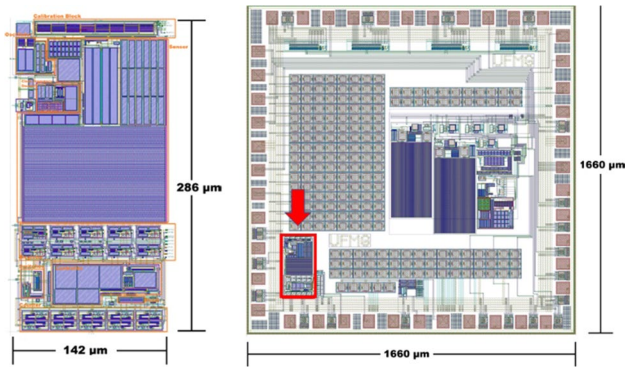

Fig. 12 The layout of the proposed STS and the chip top-level view

caused by the inclusion of the frequency doubler is minimal. This block is composed of a few logic gates (one xor gate and a few inverters).

The analog block in version (iii) was modified to present approximately the same frequency span of version (i). More specifically, to achieve a higher current and frequency span, the resistance "R" of R0 was reduced, and a few transistors of Fig. 5 were optimized. Table 1 shows a performance comparison of the three (Pre-Layout) analog block versions.

Regarding case (iii), it is possible to see that its linearity is significantly damaged to achieve a similar frequency span of (i). Moreover, its power consumption was also severely increased due to the higher sensor current (I_{PTAT}).

An alternative approach would be the design of the analog block without frequency doubler and with a reduced frequency span, to achieve better linearity, e.g., case (ii). As can be seen from Table 1, power consumption from case (i) is 40.2 nW, compared to 25.4 nW from case (ii). It is important to note that power consumption and energy are related as described by Eq. (12), where F_S is the sampling frequency (CLK_Ext signal).

$$Power = Energy \times F_S \tag{12}$$

Considering the nominal duty cycle value of 45% and a nominal sampling frequency of 100 Hz, the Analog block is active during 4.5 ms, which corresponds to an energy consumption of 181 pJ in case (i) and 114 pJ in case (ii). In order for case (ii) to operate with the same output resolution from case (i), the Analog block must stay active during twice the time, so this block would consume 228 pJ during the full measurement cycle. Therefore, the Analog block from case (i) consumes about 21% less energy in order to achieve same output resolution. Moreover, this alternative approach would also require a longer minimum sampling period (> 10 ms), and a lower maximum sampling frequency (< 100 Hz).

4 RC post-layout simulation results

The designed STS works properly for a large supply voltage range from 0.5 to 1.8 V. To demonstrate the operation for the tightest power consumption specification, the following simulations were run with a supply voltage of 0.5 V. Moreover, the following specs were also adopted: 0.5 °C output resolution, 100 Hz of external clock reference (CLK_Ext), and 45% of external clock duty cycle. The circuit was also checked using different corner process models.

4.1 PTAT_CLK signal and the output counted value

Figure 13 shows the simulated PTAT_CLK and EXT_CLK signals at 21 °C. Since the frequency of the PTAT_CLK signal is 73.6 kHz, it is not possible to properly visualize this signal on Fig. 13. Thus, Fig. 14 zooms into a specific region from the PTAT_CLK signal when EXT_CLK is at logic level 1.

Figure 15 shows the simulation of the LD and OUT_SERIAL signals at 21 °C of the Parallel-to-Serial Converter described in Section 2.8. As shown in Fig. 15, after the LD signal goes to level 1, the digital output OUT_SERIAL starts displaying the counted bits. The last bit value is retained on the output until the next cycle. The value indicated by OUT_SERIAL, in this example, corresponds to 0100111101. This 10-bit sequence corresponds to a decimal number of 317. It is worth mentioning that a CMOS inverter buffer was included in the output pin, "OUT_SERIAL". Therefore, an inverted bit string is expected to appear at this node.

Table 1 Performance comparison of the pre -layout analog block

	Linearity error (°C)	Power consumption @ 100 °C (nW)	Current span (nA)	Frequency span (kHz)
(i): Analog block *with* frequency doubler	0.33	40.2	9.9	61.4
(ii): Analog block *without* frequency doubler	0.33	25.4	9.9	30.7
(iii): Adjusted Analog block *without* frequency doubler	8.91	141.2	27.0	54.7

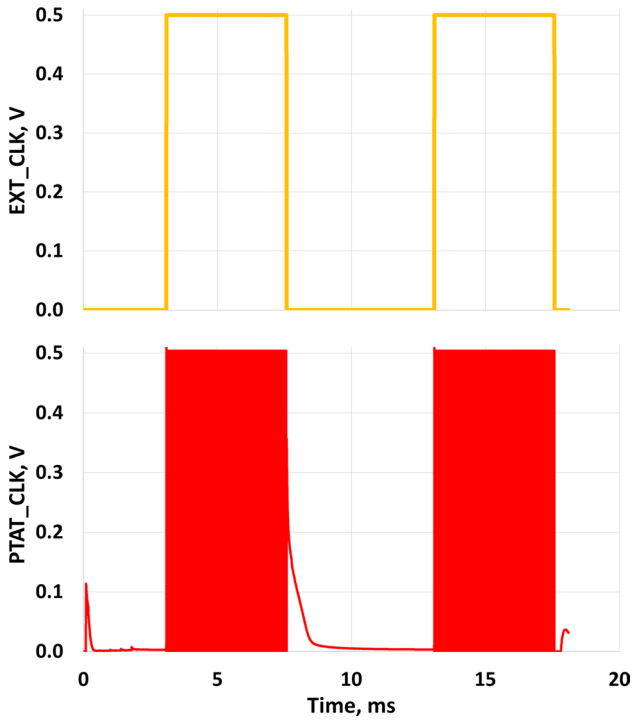

Fig. 13 Simulated EXT_CLK and PTAT_CLK signals, respectively, at 21 °C using nominal transistor electrical models

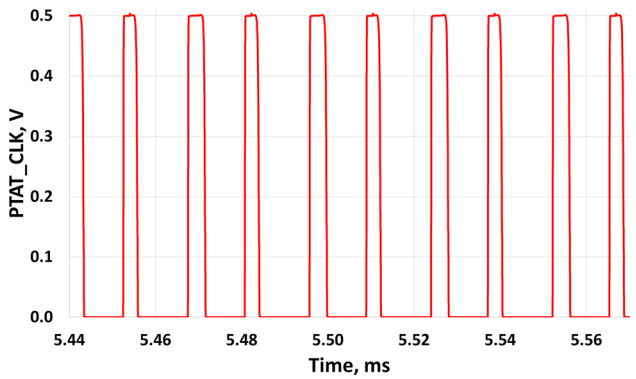

Fig. 14 The simulated PTAT_CLK signal during high-level state from EXT_CLK signal at 21 °C using nominal transistor electrical models

4.2 PTAT_CLK signal and the output counted value as a function of temperature

Figure 16 shows the frequency of output voltage of the frequency doubler (FPTAT), using the three process models: TT, SS, and FF. As can be seen, all three plots are very linear with a worst-case R-squared parameter (R^2) of 0.99997 for the FF case.

To achieve the same resolution for all three process corners, the external clock duty cycle was adjusted

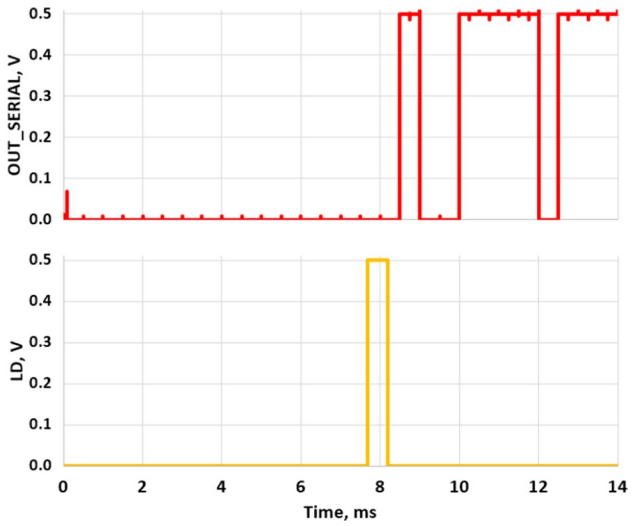

Fig.15 The simulated OUT_SERIAL and LD signals, respectively, during a full cycle of EXT_CLK signal at 21 °C

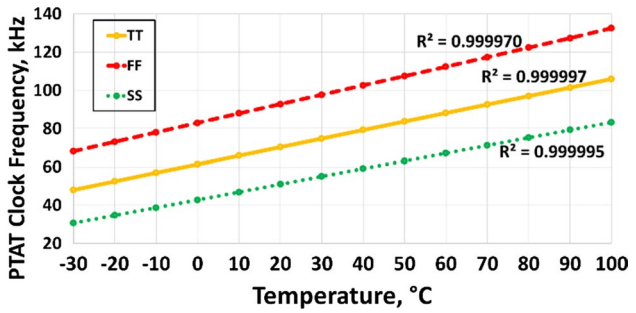

Fig. 16 Simulated PTAT_CLK frequency as a function of temperature for corner cases TT, SS, and FF

accordingly. The duty cycle adjustment is explained in details in this section. This adjustment means that the counting time has been modified to allow the proper output counting in all possible corners. This modification in the external clock duty cycle can be understood as a possible calibration parameter. Note that it is not an issue, because two-point calibration is normally required to guarantee proper and optimum operation in temperature sensors [1–4, 8].

Figure 17 shows the digital output code generated by the digital counter and the simulated nonlinearity is given in Table 2. As can be seen, the worst non-linearity occurs in the FF corner case. Analyzing the linearity over the temperature for the FF corner case, it was verified that its worst degradation happens for temperatures higher than 90 °C, as highlighted in Fig. 18.

Therefore, if the designed sensor is employed in an application that operates in the extended commercial temperature

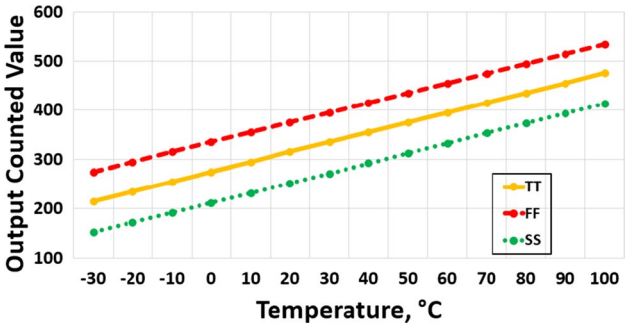

Fig. 17 Simulated output counted value as a function of temperature for corner cases TT, SS, and FF

Table 2 Post-layout simulated linearity errors

	TT (°C)	FF (°C)	SS (°C)
Maximum frequency linearity error	±0.24	±1.19	±0.44
Maximum output count linearity error	<0.5	±1.0	±0.5

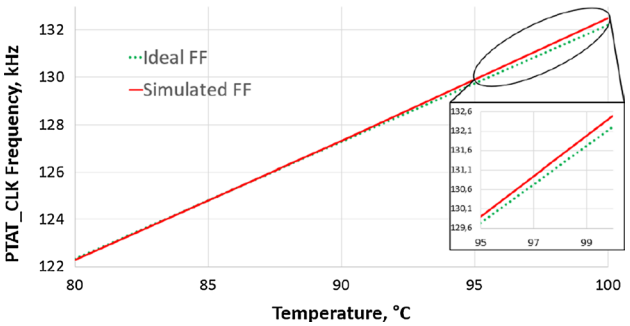

Fig. 18 The simulated PTAT_CLK frequency as a function of temperature for corner case FF

range (*i.e.*, −20 °C to+85 °C), the worst frequency linearity error for the FF corner case would be just ±0.49 °C.

4.3 Power consumption

Figure 19 shows the STS power consumption as a function of temperature using process corners. As expected, the highest (lowest) power consumption happens for the FF (SS) corner cases. Using the nominal models (TT), the highest power consumption is less than 35 nW. This power estimation does not include the power consumption of the external clock generator.

Figure 20 shows the power consumption of the design STS for different sampling periods (T_S) but keeping the STS operation for a fixed time window of 4.5 ms. It means that

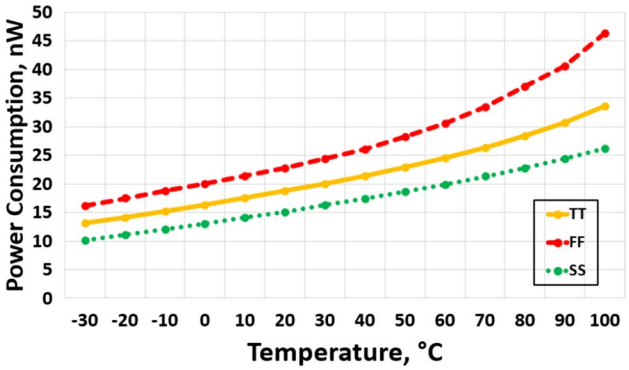

Fig. 19 The simulated power consumption as a function of temperature for process corner TT, FF, and SS

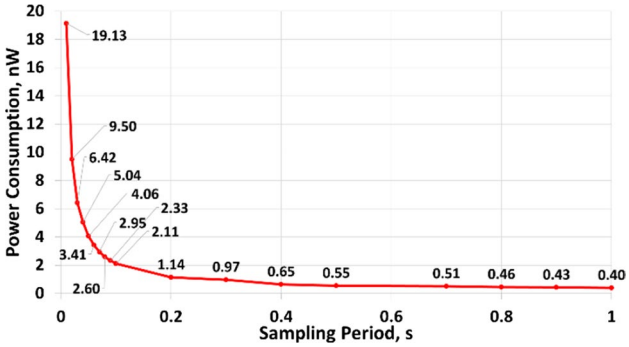

Fig. 20 The simulated Power consumption as a function of the sampling period at 27 °C

the duty cycle is different for each point in Fig. 20. The longer the sampling period, the shorter the duty cycle.

The minimum sampling period of 4.5 ms is required for the analog sub-block and the counter circuit to achieve the desired output resolution of 0.5 °C. After 4.5 ms, both blocks are turned off using a simple transmission gate when the CLK_Ext_signal goes to a low state.

For instance, for a sampling period of 10 ms (nominal F_S), the duty cycle is 45%, and the high state of the CLK_Ext signal is 4.5 ms. For a sampling period of 100 ms (low F_S), the duty cycle is only 4.5%, while the high state of the CLK_Ext signal is still 4.5 ms. As can be seen, the power consumption decreases exponentially with the increase of the sampling period. Adjusting the sampling period and its duty cycle (external clock signal) can be made according to the system specification of power consumption and repeatability of the temperature measurement. For example, if the temperature measurement is made every 1 s, the power consumption will be less than 1 nW.

An alternative way of reducing power consumption is by sacrificing digital output resolution. This is done by reducing the high state period of the EXT_CLK signal.

Note that the resolution is directly proportional to the external sampling frequency and its duty cycle, according to Eq. (11).

Figure 21 shows the simulated power consumption as a function of the digital output resolution at 27 °C for a sampling frequency of 100 Hz. The resolution is swept by adjusting the duty cycle of EXT_CLK for each point. As result, the number of counts is reduced as the resolution gets worse and duty cycle is lowered. As can be seen, the power consumption is significantly reduced if the resolution is sacrificed—ideal approach for applications that do not require high accuracy measurements.

Figures 20 and 21 show the percentage of power consumption from each block that is part of the STS device at nominal operation. The classification of analog and digital for sub-circuits implemented in the STS is done accordingly to Figs. 2, 3 and 4, explained in Section 2. As can be seen, ninety percent of the power consumption comes from the current (I_{PTAT}) and the oscillation signal (PTAT_CLK) generation. The counting and control circuits consume just 10% of total power. The most power-hungry circuit in the STS is the sensor circuit of Fig. 5, consuming about 29% of total consumption. Lower power consumption can be achieved if the resistance of resistor R0 is increased, resulting in an area penalty.

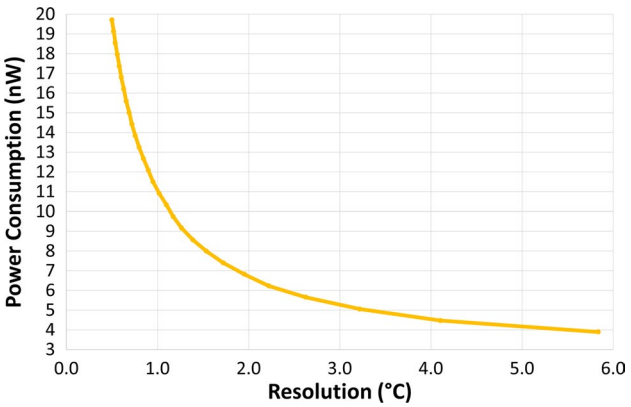

Fig. 21 The simulated power consumption as a function of the digital output resolution at 27 °C

5 Monte-Carlo analysis

To investigate the robustness of the STS against the impact of fabrication effects, Monte-Carlo (MC) analysis was performed for the post-layout extracted analog block. The analog block generates the I_{PTAT} current and the PTAT_CLK, while the digital block counts and controls the logic. Because of the expected digital nature of the digital block, its performance (counting and controlling) is not functionally affected by the fabrication process effects. Therefore, the digital block was not included in the MC analysis to reduce the extremally long simulation time. The MC simulation considered 200 samples, including both mismatch and process variations.

Table 3 presents the MC results for the linearity error and duty cycle values considering the entire operating temperature range (− 30 °C to 100 °C). Additionally, the variation of the power consumption and the PTAT_CLK frequency (at 27 °C) were also estimated. It is worth mentioning that the analog power consumption reported in Table 3 is actually higher than the real analog power consumption. The real power consumption should be lower than the one presented in Table 3 because, in the real operation of the circuit, the analog block is turned off (please, see the analog switch in Fig. 2) during the low-level phase of the EXT_CLK signal, which corresponds to 55% of the period of operation. It means that the analog block stays ON for about 45% of the full cycle of measurement, therefore, significantly reducing the total power consumption of this block (See Fig. 22).

From Table 3, it is noticeable that the fabrication process effects did not severely affect the duty cycle of the PTAT CLK signal. The worst-case duty cycle is still higher than 20%—the minimum value required by the digital counter. The maximum duty accepted by the counter is 80%. Regarding the power consumption, the worst-case scenario presents a value 18% higher than the nominal case (see Fig. 23).

The variation of the PTAT_CLK frequency was estimated to be about ± 22% for a three-sigma condition (99.73% of all samples). Figure 24 shows PTAT_CLK frequency mean values as a function of temperature with

Table 3 Results of the Monte-Carlo analysis

	Mean	Standard deviation	Lowest value	Highest value
PTAT_CLK Duty Cycle (%)	25.6	2.3	20.7	33.1
Power Consumption at 27 ºC (nW)	33.0	2.3	27.8	38.9
PTAT_CLK Frequency at 27 ºC (kHz)	73.6	5.2	60.0	86.1
Linearity Error (°C)	0.62	0.30	0.06	1.93

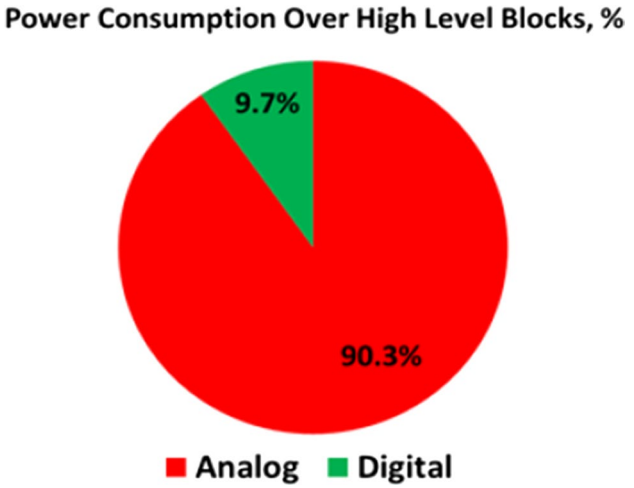

Fig. 22 The Percentage of power consumption over high-level blocks from the STS device

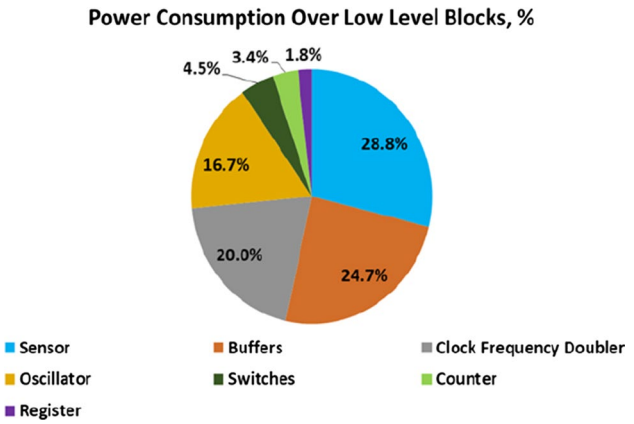

Fig. 23 The Percentage of power consumption over low-level blocks from the STS device.

delta frequency bars, representing the maximum and minimum estimated values.

Finally, regarding the linearity error, the MC analysis estimated a worst-case error of 1.93 °C. However, to fully comprehend the variability impact, the histogram of the linearity error is presented in Fig. 25.

As shown in Fig. 25, most samples had a linearity error less than 1 °C. A total of 11 samples had maximum frequency linearity error above 1.19 °C, which is the highest value presented in Table 2 when considering FF, SS, and TT process corners. Since the previously presented corners simulations did not consider mismatch and SF/FS cases, this result is expected.

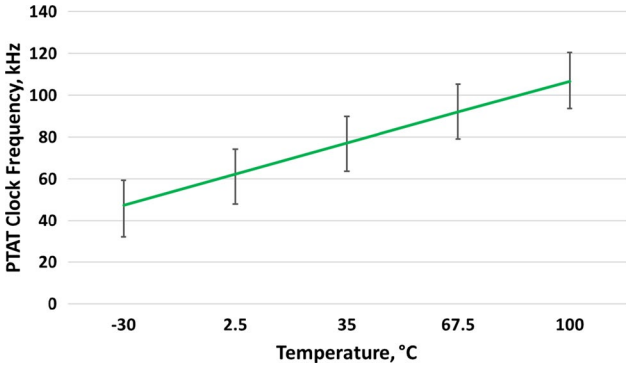

Fig. 24 Simulated PTAT_CLK frequency as a function of temperature including process and mismatch variations

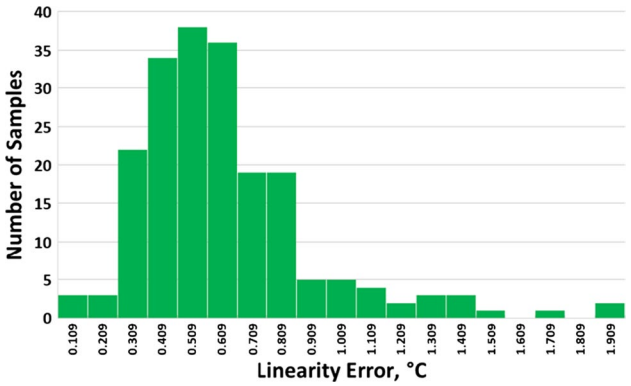

Fig. 25 Histogram of linearity error generated by the MC analysis

6 External clock (EXT_CLK) signal with a temperature coefficient

So far in this paper, the EXT_CLK signal was considered to have a constant period value over the temperature range. Since real oscillators suffer from temperature variation, this section investigates the impact of the temperature coefficient of EXT_CLK signal on the digital output signal (Output_bits).

To perform the proposed investigation, the TC of the low power and low-frequency CMOS oscillator proposed in [11] was used as a reference. Therefore, the simulations presented in this section considered the EXT_CLK with a TC of 0.07 Hz/°C. Figure 26 shows the EXT_CLK frequency as a function of temperature. As can be seen, EXT_CLK frequency varies from 104 to 94.9 Hz when considering the full operation temperature range.

Thus, Eq. (13) describes the temperature dependency of EXT_CLK signal frequency (F_S):

$$F_S = -0.07 \times temperature + 101.9 \quad (13)$$

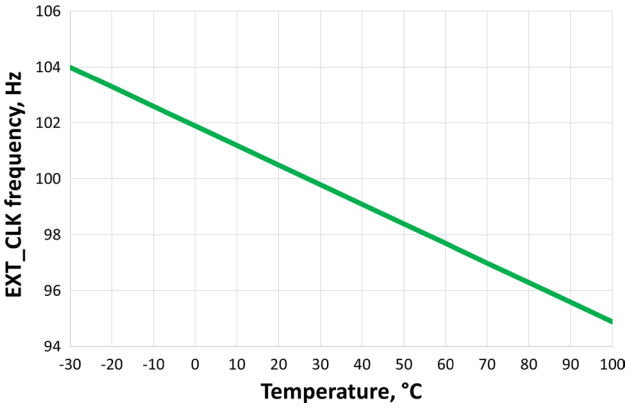

Fig. 26 The simulated EXT_CLK signal frequency as a function of temperature

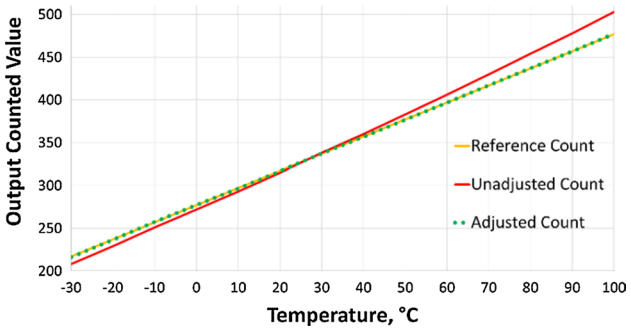

Fig. 27 Simulated output counted value as a function of temperature for three cases: (i) reference, (ii) unadjusted and (iii) adjusted counts

It is possible to rewrite Eq. (9) in Eq. (14), where T_{active_ref}, is named here the reference active time of the counter with zero TC.

$$T_{active,\_ref} = D \times T_S = \frac{D}{F_S} = \frac{D}{100} \tag{14}$$

Thus, considering the effect of temperature described by Eq. (13), a new equation can be written to represent the active time of the counter, Tactive', when the EXT_CLK has a temperature coefficient.

$$T_{active}{}' = D \times T_S = \frac{D}{F_S} = \frac{D}{-0.07 \times temperature + 101.9} \tag{15}$$

Moreover, Eq. (10), that describes the counting, can also be rewritten using (14) and the proper terminology:

$$C_{OUNT\_ref} = \frac{T_{active\_ref}}{F_{PTAT}} = \frac{D}{100 \times F_{PTAT}} \tag{16}$$

Then, Eq. (16) can be simply written as (17):

$$\frac{F_{PTAT}}{D} = \frac{1}{100 \times C_{OUNT\_ref}} \tag{17}$$

Now considering the temperature coefficient and using Eqs. (15) and (17):

$$C_{OUNT}{}' = \frac{T_{active}{}'}{F_{PTAT}} = \frac{1}{F_{PTAT}} \times \frac{D}{-0.07 \times temperature + 101.9} \tag{18}$$

Equation (18) reveals that the final temperature counting depends on the operation temperature if the real oscillator responsible for generating the EXT_CLK has a temperature coefficient different from zero.

Equation (17) can be used in Eq. (18) since D, and F_{PTAT} variables are the same for both cases (EXT_CLK with and without TC). Thus, C_{OUNT}' is given by:

$$C'_{OUNT} = C_{OUNT\_ref} \times \frac{100}{-0.07 \times temperature + 101.9} \tag{19}$$

Finally, Eq. (19) can be simplified as (20), where β represents the term that is multiplying C_{OUNT_ref}:

$$C'_{OUNT} = C_{OUNT\_ref} \times \beta \tag{20}$$

Equation (20) highlights the relation between C_{OUNT}´ and C_{OUNT}, which is just β.

Thus, if the C_{OUNT}´ was multiplied by 1/β, a new count, called, $C_{OUNT,adjusted}$, equal to the C_{OUNT_ref} is obtained, as described by (21):

$$C_{OUNT,adjusted} = C_{OUNT\_ref} = C'_{OUNT} \times \frac{1}{\beta} \tag{21}$$

Equation (21) importantly reveals that although the temperature information (counting) generated by the STS can be affected by the TC of real oscillators, a correction term, β, can be applied to mitigate its effect.

6.1 Simulation considering EXT_CLK with a temp. coefficient

Figure 27 shows the results of the count for three cases, (i), (ii), and (iii). In case (i), the EXT_CLK signal has no TC, and is called the reference (C_{OUNT_ref}). Cases (ii) and (iii) consider EXT_CLK with TC, but without (C_{OUNT}´), and with correction term ($C_{OUNT-adjusted}$), respectively.

As can be seen, the temperature coefficient of TC significantly affects the count (red curve). Moreover, its maximum linearity error is also worse for ± 3.9 °C.

Nonetheless, an adjusted count is obtained if the correction term is applied as described by Eq. (21). The new adjusted count is very close to the reference count, and the maximum linearity error is reduced to 0.75 °C, which

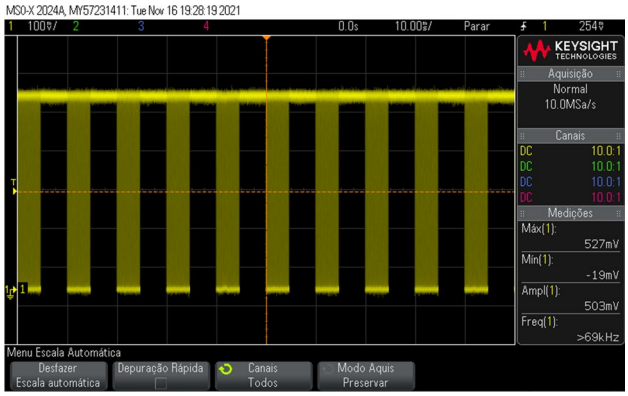

Fig. 28 Measured PTAT_CLK during full cycle from EXT_CLK signal at 21 °C

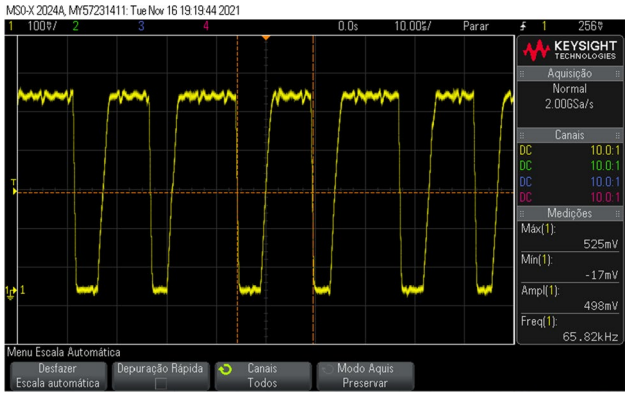

Fig. 29 The measured PTAT_CLK signal during high-level state of the EXT_CLK signal at 21 °C

proves the correction method's effectiveness for the count and the linearity error.

The maximum linearity error after the count correction is slightly higher than the reference case because of the digital nature of the counting process. However, this value can be reduced if a better resolution is employed.

7 Silicon results

A preliminary test of the fabricated circuit was performed at room temperature (21 °C) to check the proper operation of the STS device. Figure 28 shows the measured PTAT_CLK during several cycles of the EXT_CLK.

As mentioned before, the analog block only works during the high-state of the EXT_CLK signal. Figure 29 shows the measured frequency of the PTAT_CLK signal. Both figures are similar to Figs. 13 and 14 (Section 4.1), meaning the proper operation of the analog block. The measured frequency, 65.8 kHz (at 21 °C), also agrees with the simulation results presented in Figs. 14, 16, and 24.

Figure 30 shows the measured LD and OUT_SERIAL signals at room temperature over multiple EXT_CLK cycles. Figure 31 shows just one cycle. These measured results are in agreement with simulation results shown in Fig. 15.

Each bit shown in Fig. 31 has a time length of 0.5 ms, and the measured sequence is 1011110010. Since this output signal passed through an inverting buffer, the real temperature signal counted is 0100001101, corresponding to a decimal number of 269.

As expected, the measured bit string is a little different from the simulated bit string, 0100111101 which corresponds to a decimal number of 317. The ideal simulation results shown in Fig. 15 are ideal and did not include process effects.

Finally, Fig. 32 shows the test setup done in our laboratory to measure the output signals of the fabricated STS

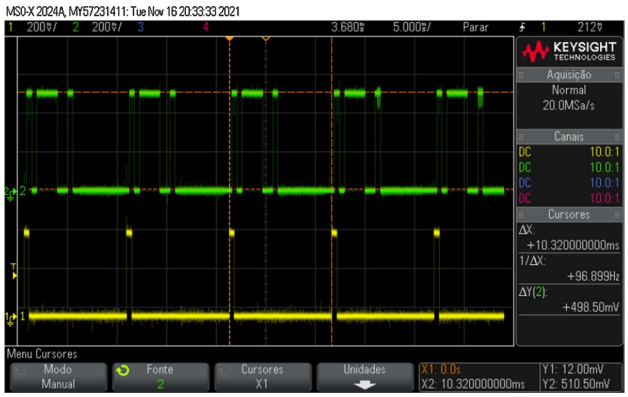

Fig. 30 The measured LD and OUT_SERIAL signals during multiple cycles from EXT_CLK signal

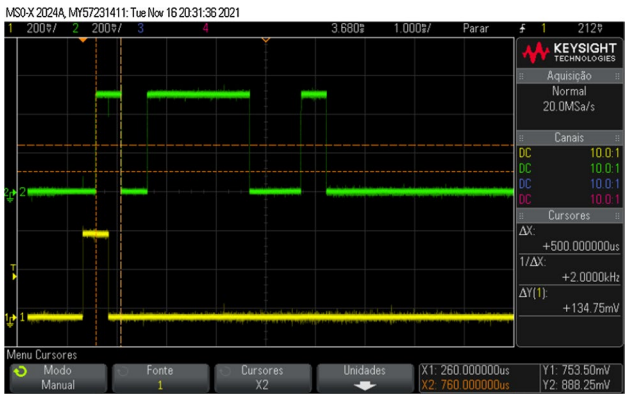

Fig. 31 The Measured LD and OUT_SERIAL signals during full cycle from EXT_CLK signal. Bit string: 1011110010. Non-inverted bit string: 010001101

device. The fabricated circuit's main input/output pins are VDD, VSS, EXT_CLK, CLK_SERIAL, LD, PTAT_CLK, and OUT_SERIAL.

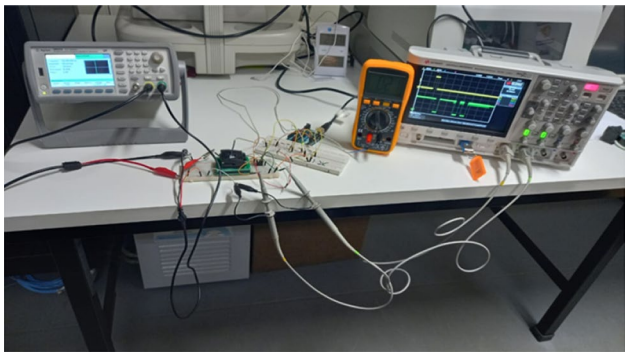

Fig. 32 Laboratory setup to test the STS device

A waveform generator was employed to produce the VDD and EXT_CLK signals. An Arduino Uno was programmed to produce the CLK_SERIAL and LD signal, while a digital oscilloscope was used to measure PTAT_CLK, OUT_SERIAL, and LD signals. The GND reference from the oscilloscope probe, Arduino board, Waveform Generator, and the chip VSS pin was tied together.

Finally, it is worth to mention that a thermocouple and a digital multimeter was used to measure the chip temperature.

8 Comparison with related works

Table 4 compares the designed STS (post-layout results) with related works. All of the sensors considered in the comparison have an FDC topology. This type of architecture allows for low power consumption but usually is not as highly precise as STS based on ADCs. Moreover, all related works are smart sensors that generate a digital output code.

From Table 4, it is possible to see that this work presents the lowest power consumption and also the lowest energy per conversion. Although a fair comparison between simulated and silicon proved circuits cannot be made, the results reveal that the proposed circuit is promising in terms of low power consumption.

Equation (12) shows that even if different values of sampling frequency are chosen, the designed circuit still presents the lowest power consumption. Regarding the minimum supply voltage (VDD_{MIN}), this work presents the lowest value in Table 4. The achieved performance is comparable to work [8], implemented in 130 nm process, with the exception that the analog part of [8] operates with a supply voltage of 0.2 V.

Since our work was implemented using 180 nm process, there is still a margin of optimization if newer CMOS technologies are used. The use of halo-implanted transistors with low output impedance in the used CMOS technology made necessary the inclusion of cascode devices in the sensor of Fig. 5 to allow proper operation in the large supply voltage range of 0.5–1.8 V.

The simulated results show promising operation regarding the absolute accuracy, although it is expected that noise and other causes of inaccuracy will show up in the silicon measurements. Finally, the designed circuit has the third-largest range regarding the temperature of operation. If a reduced temperature range is considered, the accuracy of the designed STS will be better.

9 Conclusion

This work presents topology of a smart temperature sensor with ultra-low power consumption and low supply voltage operation while achieving moderate accuracy ($< \pm 1$ °C). The simulated worst-case power consumption at 100 °C using FF process corner and a sampling frequency of 100 Hz is less than 50 nW.

The proposed approach to include a frequency doubler proved to be efficient. This technique can be employed in other smart temperature sensors based on frequency to

Table 4 Comparison of this work with similar works on literature

Article	This work	[1]	[2]	[3]	[4]	[5]	[8]
Year	2020	2014	2017	2018	2019	2017	2016
CMOS process (nm)	180	180	180	130	130	65	130
VDD_{MIN} (V)	0.5	1.2	1.8	1.1	1.1	0.5	0.2 / 0.5
Area (mm^2)	0.041	0.09	0.118	0.0014	0.0014	0.009	0.0625
Energy per Conversion (nJ)	0.19	2.2	93.6	75	150	4.8	0.23
Power (µW)	0.019	0.071	93.6	0.15	0.15	8.8	0.023
Absolute Error (±°C)	0.24/−0.24	1.5/−1.4	2 / -2	0.36/−0.27	1.1/−0.9	0.8/−0.75	1.5/−1.7
Sample Frequency (Hz)	100	32.8	1 k	2	1	1.8 k	100
Temp. Range (°C)	−30 ~ 100	0 ~ 100	−20 ~ 120	7 ~ 42	−60 ~ 40	−55 ~ 125	0 ~ 100
Silicon?	No	Yes	Yes	Yes	Yes	No	Yes

digital conversion. The preliminary silicon results show the functionality of the designed circuit, although a full temperature characterization was not performed.

Moreover, temperature coefficient of the external clock on the performance of the sensor was modeled and a correction parameter was presented. To the best of the authors' knowledge, it is the first time that the temperature coefficient of the external clock signal is investigated for an STS based on Frequency to Digital conversion. The proposed analysis can be applied to other temperature sensors.

Finally, the designed circuit may be the right candidate for Wireless Sensor Networks or on-chip temperature monitoring systems, where high-precision sensors cannot be placed because of power and supply voltage constraints.

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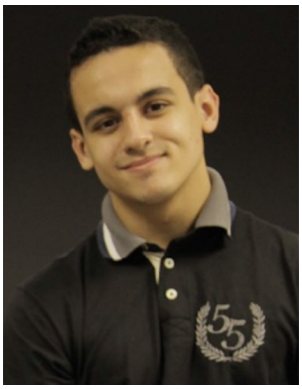

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