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MIXED SIGNAL LETTER

A low-power and robust quaternary SRAM cell for nanoelectronics

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Abstract
This paper presents an efficient and low-power quaternary static random-access memory (SRAM) cell based on a new quaternary inverter. For implementation, carbon nanotube field-effect transistors (CNTFETs) are used. Stacked CNTFETs are appropriately used in the proposed design to achieve a considerably low static power dissipation. The proposed SRAM has a more significant static noise margin due to its single quaternary digit line, and it is appropriate for MVL SRAM design as there are more than two stable states. The simulation results using Synopsys HSPICE with 32 nm Stanford comprehensive CNTFET model demonstrate the correct and robust operation of the proposed designs even in the presence of major process variations. In addition, the proposed SRAM cell is applied in a 4×4 SRAM array structure to demonstrate the efficiency of the proposed SRAM. The results indicate that the proposed design significantly lowers the power consumption and provides comparable static noise margins compared to the other state-of-the-art CNTFET-based circuits.

Keywords Quaternary logic · Static random access memory · Carbon nanotube field effect transistor · Nanoelectronics

1 Introduction

Some of the essential objectives considered in the VLSI design are the reduction of power consumption, delay, and complexity. To achieve these goals, changing computation logic and technology attitudes are essential. By the inevitable scaling down of the feature size in modern binary chips, interconnection has become the dominant factor of power consumption, delay, and area.

As a result, acquiring a new computing method has become necessary to overcome these limitations. Multiple-valued logic (MVL) is an alternative logic that utilizes more than two significant logic levels. One of the most important advantages of MVL is the capability of packaging more information within a single digit. In addition, MVL permits more information to be transmitted over a given set of wires, which reduces the complexity of interconnects and leads to more energy efficiency in digital integrated circuits. The MVL structures have a lower noise margin due to the voltage band division between more true states.

Moreover, using MVL can reduce the number of operations necessary to implement a particular mathematical function and thus have advantages in terms of hardware efficiency and power dissipation and provide a higher speed of operation [1, 2].

It is noteworthy that among the radices greater than two, radices which are the power of two, such as radix-4 (quaternary logic), are more of interest due to their simple conversion to radix-2 and vice versa. The most promising applications of MVL are memories and arithmetic circuits [1]. Hence, bigger blocks can be designed in quaternary logic to reduce chip area because of its compatibility with binary logic to design systems. Using quaternary logic leads to simplicity and higher performance because of reducing the limitations of interconnections.

On the other hand, scaling down the CMOS technology has led to challenges such as intensive short-channel effects, reduced gate control, exponentially rising static currents, severe process variations, and high power density [3]. In addition, higher power density increases the chip

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temperature and leads to performance degradation, failures, and costly packaging. Therefore, some other nanoscale technologies have been investigated to replace the conventional Si-based CMOS technology. Considering these nanotechnologies, carbon nanotube FET (CNTFET) is the most encouraging option for replacing the Si MOSFET in the time to come. This is due to its inherent similarities with the conventional MOSFET and the existence of both n-type and p-type transistors, which have led to comparable designing techniques with the CMOS technology. In addition, the capability of having CNTFETs with desired threshold voltages makes it a promising option for designing efficient multiple-valued logic circuits [4, 5].

SRAMs are widely used in embedded systems, system-on-chips, field-programmable gate arrays, and high-performance processors as caches, reservation stations, and branch target buffers and contribute to a considerable portion of the die area and power consumption [6, 7]. As a result, designing efficient and robust CNTFET-based quaternary SRAM cells is remarkable. Interconnections are the main reason for the power dissipation of SRAM. SRAM occupied a large area of an SoC, then quaternary SRAM by decreasing interconnection led to lower power and occupied area intensively.

This paper proposes a robust and low-power CNTFET-based quaternary SRAM cell based on an energy-efficient modified quaternary inverter for nanoelectronics.

The rest of the paper is organized as follows: a review of CNTFET is presented in Sect. 2. The related works explain in Sect. 3. The proposed designs are introduced in Sect. 4. Simulation results, such as power, delay, static noise margin, DC analysis, and SRAM array, are given in 5, followed by the conclusion in Sect. 6.

2 A review of carbon nanotube FET (CNTFET)

A carbon nanotube (CNT) is a tube of graphene that can be categorized into single-walled nanotubes (SWNT), made up of one cylindrical wall and multi-walled nanotubes (MWNT), made up of more than one cylinder [8]. One of the physical properties of a CNT is its chirality vector that is determined by the (n, m) pair. SWCNTs are categorized into three different types (armchair, chiral, and zigzag) based on the chiral vector of CNTs. If n—m = 3 k (kεZ), an SWNT is metallic; otherwise, it is a semiconductor [9]. The semiconductor CNT can be used as the channel of carbon nanotube transistors. The I–V characteristics of a CNTFET are similar to a MOSFET, while the CNTFET has a combination of a high-mobility and ultra-thin body channel. Ballistic carrier transport in CNT decreases the resistivity, considerably increases the speed, and reduces the power density in the channel of CNTFET [10].

Different types of CNTFET, including Schottky Barrier CNTFET, tunneling CNTFET, and MOSFET-like CNTFET, have already been investigated in the literature. The MOSFET-like CNTFET is appropriate for designing high-performance and energy-efficient digital circuits due to its similarity to MOSFET in terms of inherent electrical characteristics and device structure and absence of Schottky Barrier [11]. The structure of a MOSFET-like CNTFET is illustrated in Fig. 1.

The approximate gate width of a CNTFET can be calculated using Eq. (1) [12]:

$$W_{gate} \approx Max(W_{\min}, N \times Pitch) \tag{1}$$

W_{min} denotes the minimum width of the gate, which is determined based on the limitations of lithography. N indicates the number of nanotubes used in the channel, and $Pitch$ indicates the distance between the centers of two adjoining SWCNTs under the same gate.

The threshold voltage of a CNTFET is the voltage required to make a conducting channel between source and drain and turn ON the transistor. The threshold voltage of a CNTFET can be determined by changing the diameters of CNTs, making it flexible for designing digital circuits and appropriate for designing multi-valued logic circuits. The threshold voltage is considered almost half of the bandgap and calculated as Eq. (2) [12]:

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV\pi}{eD_{CNT}} \approx \frac{0.43}{D_{CNT}}. \tag{2}$$

where Eg is the bandgap of CNT, e is the unit electron charge, a ($\approx$0.249 nm) is the carbon to carbon bond length in a CNT, $V\pi$ ($\approx$3.033 eV) is the carbon π-π bond energy in the tight-binding model, and D_{CNT} is the CNT diameter (in nanometre) which can be calculated by Eq. (3) [12].

$$D_{CNT} = \frac{a\sqrt{n^2 + nm + m^2}}{\pi} \approx 0.0783\sqrt{n^2 + nm + m^2} \tag{3}$$

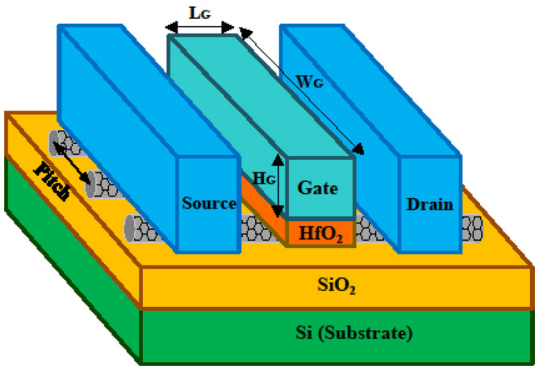

Fig. 1 Schematic diagram of MOSFET-like CNTFET

It can be concluded from Eqs. (2) and (3) that the threshold voltage of a CNTFET is defined by its chirality vector (n, m) by setting the diameter of its CNTs. It is worth pointing out that many applicative and effective solutions have already been introduced in the literature for growing CNTs with a determinate chirality and adopting the eligible threshold voltage for multi-tube CNTFETs [13–17]. Nevertheless, designing CNTFET-based circuits with fewer distinct CNT diameters decreases fabrication complexity and enhances manufacturability.

One of the significant advantages of binary logic compared with MVL is its higher noise margin. The noise margin is more intensive when various noise sources such as temperature, process variations, crosstalk effect in interconnections are considered. However, the impact of these sources is significantly lower in CNFET technology compared with CMOS technology [18, 19].

3 Related works

In the past years, many quaternary designs based on CNTFETs have been presented in the literature [10, 20–23]. On the other hand, as mentioned before, SRAM is an essential cell into digital circuits, and many SRAMs in binary and quaternary logics have been presented until now [24–27]. Some of them are transferred designs of their CMOS counterparts; another group is unique for CNTFET.

Therefore, five quaternary inverters have been selected for evaluation and comparison with the proposed design. These designs are shown in Fig. 2. These designs are completely made by CNTFET and include only one supply voltage and ground level. These investors were replaced in the proposed SRAM cell structure, and then SRAM cells based on different quaternary inverters were compared together. Furthermore, the SRAM structure of [24] is used as a comparison.

The quaternary inverter of Fig. 2a [10] was designed based on binary invertors. This design consumes large static power. The design of Fig. 2b [20] consumes more static power in 3-out-of-4 states of logic levels than the aforementioned designs. Another inverter was proposed in [21] and illustrated in Fig. 2c has three supply voltages. The design of [22] is shown in Fig. 2d. In this design, the input voltage is decoded into binary signals then these signals are weighted with the same values to generate the output. The design applies CNFETs as load. In this design, the values of loading CNFETs are selected such that the weighting takes place properly for different logic levels. This design has the largest average power consumption and PDP compared to other designs. Figure 2e shows the invertor of [23] this design using two separated paths with diode connection to generate '1' and '2' logic levels. This design has many different chirality and has static power consumption. The SRAM design of [24] is shown in Fig. 2f. This design has two split bit-line and three transmission gates in the SRAM structure, leading to more power consumption and read and write delay than the proposed SRAM.

4 The proposed designs

A quaternary (4-valued) function *F(x)* with *k* variables, where $x = \{x_1, x_2, x_3, \ldots, x_k\}$ and each x_i adopt values from $Q = \{0,1,2,3\}$, is a mapping $f: \{0,1,2,3\}^k \rightarrow \{0,1,2,3\}$. The 0, 1, 2 and 3 symbols denoting the quaternary values are commonly equivalent to voltage levels around *0 V*, *VDD/3*, *2VDD/3* and *VDD*, respectively.

4.1 Quaternary inverter

The proposed CNTFET-based quaternary inverter using pseudo-nFET logic is demonstrated in Fig. 3. The pseudo-nFET logic has high speed and low transistor count. The pseudo-nFET based inverter is presented in [20] that the main problem is its large static power consumption. Therefore, the stacking approach is appropriately used to considerably reduce the static power consumption in the proposed design [28].

By utilizing the device stacks, a considerable reduction in static ON and OFF currents is obtainable by simultaneously turning ON and OFF more than one transistor between supply and ground and increasing the resistance of this path [29]. In addition, the $|V_{DS}|$ of the transistors are reduced, which leads to lower static currents. Moreover, the threshold voltages of the added transistor are increased because of reducing the V_{SB} in the added pMOS device. So the static currents will be considerably decreased. This design consists of seven CNTFETs such that T6 and T7 are used as the pull-up devices, and the others are used as the pull-down logic network.

By adjusting the chirality of the nanotubes, the threshold voltages of the CNTFETs are determined. It is noteworthy that the threshold voltages for (T1, T6, T7), (T2, T5), and (T3, T4) are 0.69, 0.42 and 0.22 V, respectively.

When the input voltage is lower than 220 mV (at a power supply voltage of 0.9 V), T1–T3 turns OFF and pulls the output voltage up to VDD. When the input voltage is between Vth1 and Vth2 (220 and 420 mV), T3 turns ON and hence the output voltage, determined by the resistance ratio of T5-T7, is approximately 2VDD/3. When the input is between Vth2 and Vth3 (420 and 690 mV), T2 and T3 turn ON, and the output voltage, determined by the

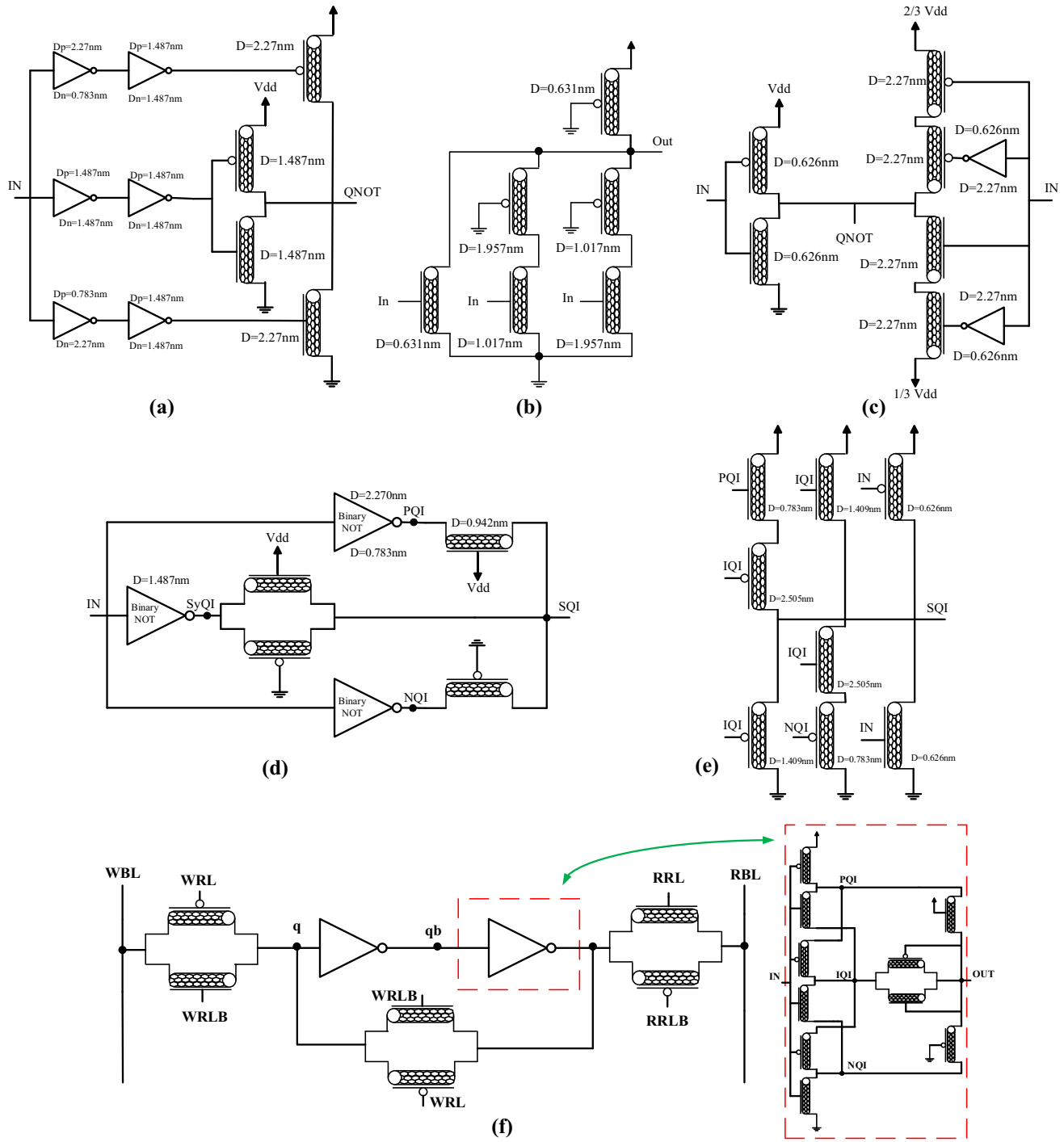

Fig. 2 Quaternary inverters, and SRAM (**a**) [10], (**b**) [20], (**c**) [21], (**d**) [22], (**e**) [23], (**f**) [24]

resistance ratio of T4, T6, and T7, is nearly VDD/3. For the zero logic, when the input voltage is higher than 690 mV, T1-T3 turns ON, hence the output is held at 0 V. The transient response and the voltage transfer characteristics (VTC) of the proposed quaternary inverter are demonstrated in Fig. 4.

4.2 Quaternary SRAM cell

This section introduces and describes the proposed quaternary SRAM cell with one *qit* (quaternary digit) line (QL). The conventional binary SRAMs use two-bit lines (BLs) for reading. However, a single-bit line SRAM has a larger static noise margin (SNM) [30]. Hence, this style is

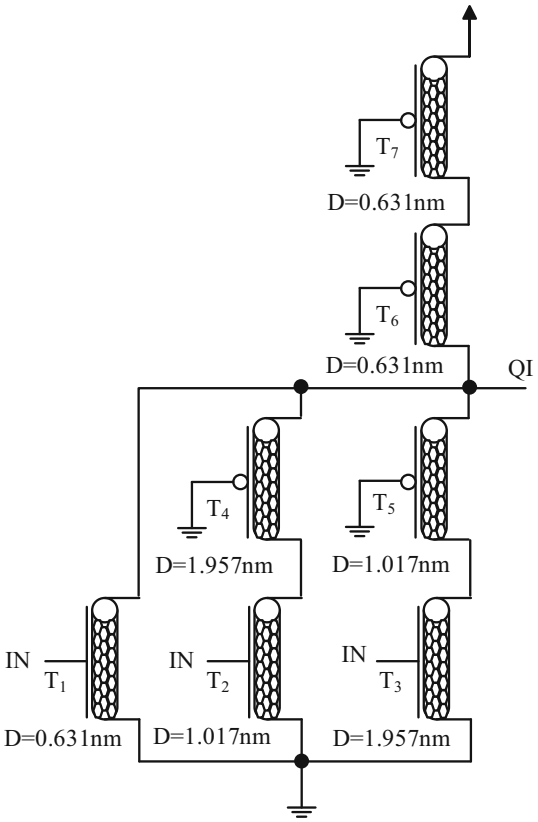

Fig. 3 The proposed quaternary inverter (QI)

more appropriate for MVL SRAM design as more than two stable states. The parameter values of the proposed SRAM are denoted in Table 1. Transistor level implementation of the proposed quaternary SRAM cell is shown in Fig. 5. Two cross-coupled proposed quaternary inverters are used as the essential components of the storage element for

Table 1 The parameter values of the proposed SRAM

Transistor number	Parameter Values			
	Chirality (n, m)	Vth	Tubes	Vdd
1, 6, 7, 8, 13, 14	(8, 0)	0.7 v	3	0.9 v
2, 5, 9, 12	(13,0)	0.4 v	3	0.9 v
3, 4, 10, 11	(25,0)	0.2 v	3	0.9 v
15, 16	(19,0)	0.3 v	5	0.9 v

holding the quaternary data based on quad stability. One transmission gate connected to *QL* for both read and write operations is used to access the back-to-back inverters, which is activated by the word line (*WL*) and its complement (*WLB*).

There are three operating states related to the SRAM: hold, read and write, that illustrated in Fig. 6. These states are described as follows:

Hold: The transmission gate is disabled by applying the *WL* signal low, and the data is held in the latch. When q has logic 0, transistors T6-T10 are ON to hold node *q* to 0 and node *qb* to VDD. For *q* = VDD/3 (logic 1), transistors T3, T5, T6, T7, T9, T10, T11, T13, T14 are ON to hold node *q* to 0.3 V, and *qb* to 'VDD-q' (*qb* = 2VDD/3). For *q* = 2VDD/3 (logic 2), transistors T2, T3, T4, T6, T7, T10, T12, T13, T14 are ON to hold *q* to 2VDD/3 and *qb* to VDD/3, and for *q* = VDD (logic 3), transistors T1, T2, T3, T13, T14 are ON to hold *q* to VDD and *qb* to 0 V.

Write: *W* denoted the write operation in Fig. 6. The input data which must be written into the cell is applied to the *QL* Because of using only one *QL* for both read and

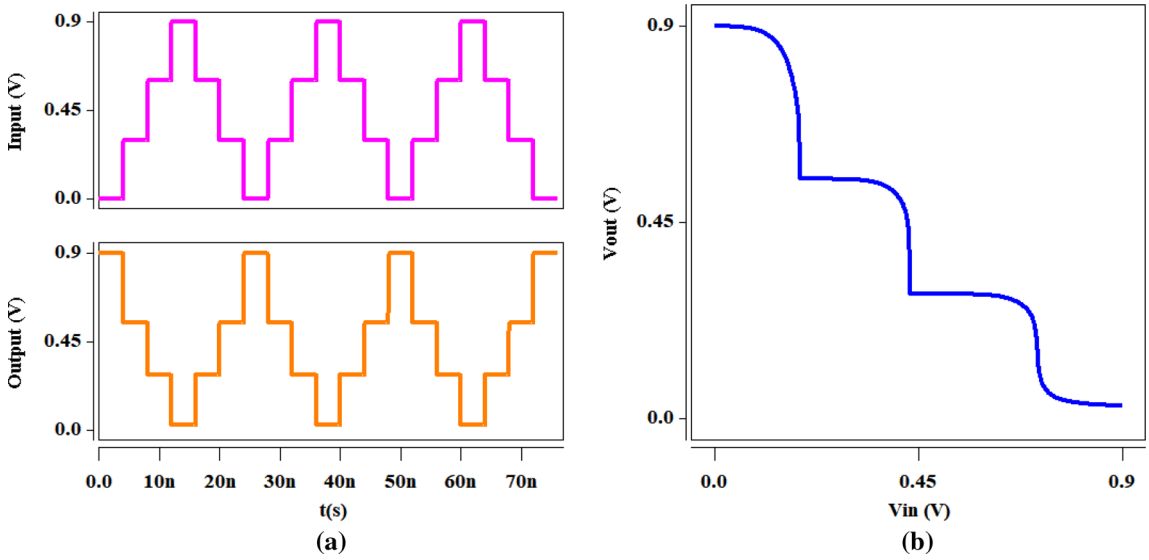

Fig. 4 Characteristics of the proposed quaternary inverter (**a**) Transient response (**b**) DC response

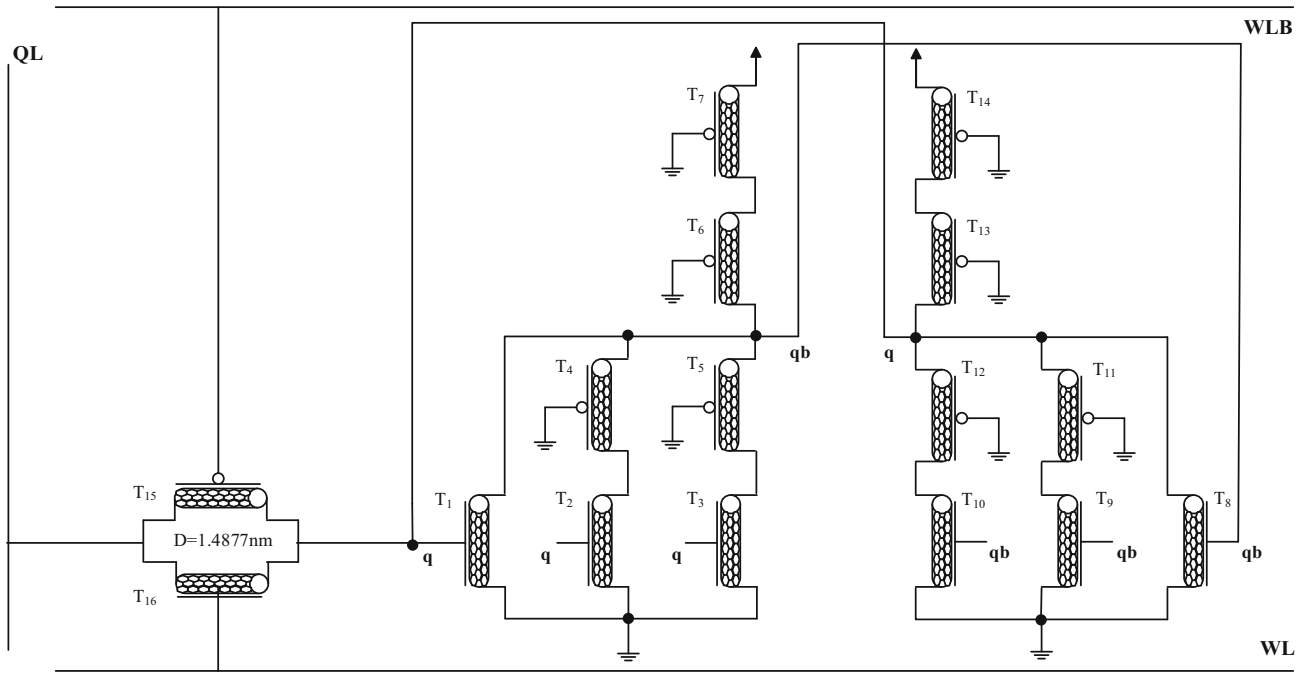

Fig. 5 Transistor level implementation of the proposed quaternary SRAM cell

write operations. Switch signal and WL signal are used to control read and write operation. Write operation occurs when the input path is connected (the switch signal is high). Also, the transmission gate is enabled by applying a *WL* signal with high. The value of *QL* is stored in node *q*, and '*VDD-q*' is stored in *qb*.

Read: *R* denoted the read operation in Fig. 6. The read operation occurs when the input path is disconnected (the switch signal is low). Then the transmission gate is enabled by applying a *WL* signal with high, and the stored value can transfer into the *QL* and be read from the cell.

5 Evaluation

The Synopsys HSPICE simulator with the 32 nm Stanford comprehensive CNTFET SPICE model [31, 32] is used to simulate the designs at 0.9 V supply voltage.

5.1 Performance evaluation of the quaternary inverters (QIs)

In this section, the proposed quaternary inverter is simulated, and their performance is evaluated and compared with some of the best previously presented designs. The designs of [10, 20–23] are picked for simulation and comparison. The performance parameters of the proposed design and the other designs are given in Table 2. Propagation delay is calculated from the input reaching half of its swing volts until the output reaches half of its swing voltage. (Based on Picosecond).

Although the design of [10] has a very small delay, it has a very high average and static power consumption, making it unsuitable for applications such as SRAM design.

In addition, using stack transistor in the proposed QI considerably decreases the static power consumption and reduces the average power by a penalty of delay increment. However, It is worth pointing out that power saving is becoming very important, especially in portable devices that do not require very high speed. Some applications such as nano-micro-sensor nodes and distributed control systems need low energy consumption and long battery lifetimes rather than speed. It is noteworthy that the proposed structure improves the average and static power consumption compared to other designs.

5.2 The performance measure for an SRAM.

Simulation results of the proposed SRAM based on the modified quaternary inverter and other quaternary inverters of [20–23] and SRAM of [24] are given in this section.

5.2.1 Read and write delays

The write delay is estimated as the time from the moment that the *switch* signal rises and crosses *VDD/2* to when the data in *q* crosses 50% of its logical interval while *WL* is high. The read delay is defined as the time required to sense

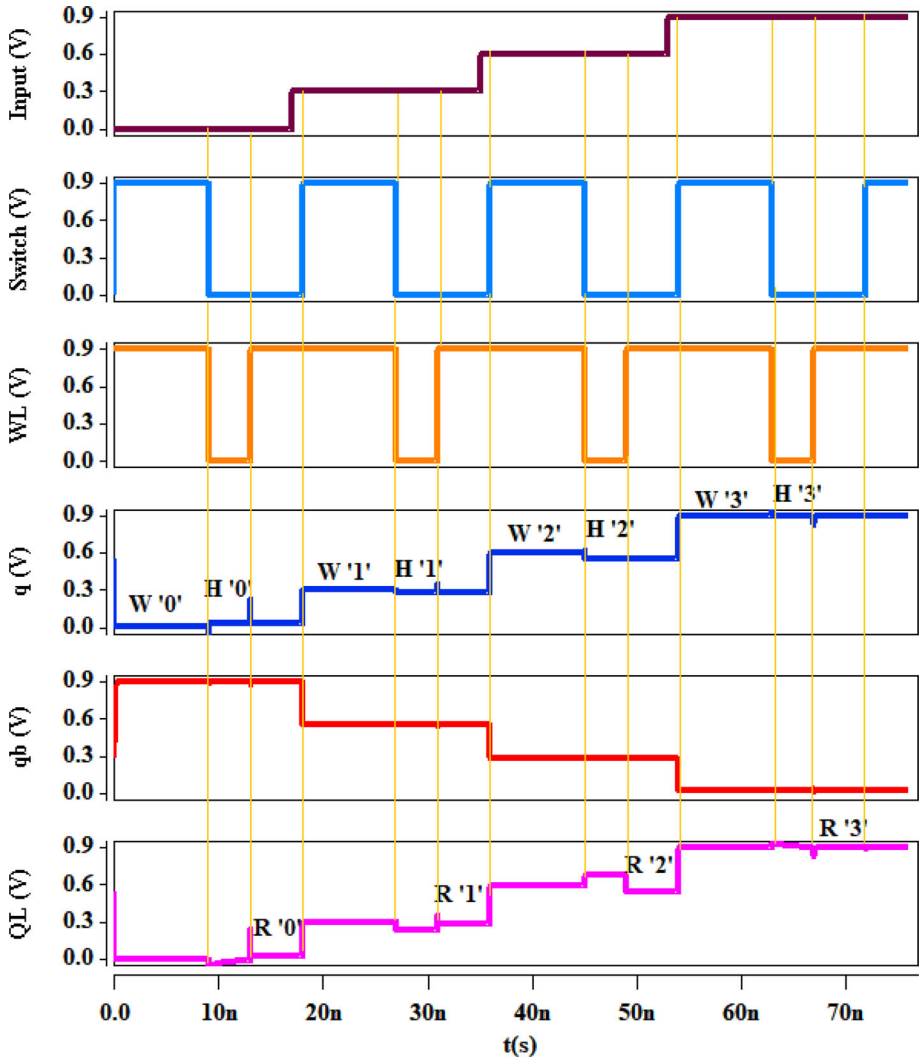

Fig. 6 Transient response of the proposed quaternary SRAM, ('W' denote write, 'H' denote hold, and 'R' denote read)

Table 2 Average power, static power, and propagation delay of the QIs

Inverter	Average Power (μW)	Static Power (μW)	Propagation Delay (pS)
QI of [10]	24.31	21.61	3.060
QI of [20]	1.15	1.10	6.28
QI of [21]	0.87	0.69	5.99
QI of [22]	1.47	1.16	12.46
QI of [23]	0.85	0.70	17.82
The Proposed QI	0.51	0.49	19.70

the data in the *QL* after the voltage of *WL* rises and crosses *VDD2* while the *switch* signal is low.

Read and write delays of SRAM cells are given in Table 3. According to the results, there is no considerable difference between the delays of the SRAMs as the adding stack transistor to the pull-up network of the modified quaternary inverter does not change its output capacitors.

5.2.2 Power consumption

Power consumption is a significant concern in memory design, and reduction of the power consumption in memories leads to a significant decrease in total power consumption in VLSI chips. Power consumption is the average power consumed during reading and writing all of the logic.

Table 3 Read and write delays of the SRAM cells

Delay	Write (*pS*)	Read (*pS*)
SRAM cell based on [20]	3.5	0.260
SRAM cell based on [21]	3.4	0.270
SRAM cell based on [22]	4.0	0.267
SRAM cell based on [23]	4.03	0.268
SRAM cell [24]	5.35	0.747
Proposed SRAM cell	3.7	0.260

The average power consumption and static power dissipation of the quaternary SRAM cells are given in Table 4. According to the results, the proposed SRAM cell has considerably lower powers than the CNTFET-based SRAM based on the *QI* of [20–23] and SRAM [24]. According to the results, the average improvement percentage of using the proposed SRAM in terms of average and static power consumptions is 53 and 54, respectively.

5.2.3 Static noise margin

The static noise margin (SNM) demonstrates the stability of an SRAM cell against DC noise disturbances. SNM is obtained by drawing the inverter voltage characteristic (VTC) and its mirror (VTC^{-1}) in the same plot (butterfly curve) and finding the diagonal of the smallest square in the plot.

The butterfly curves of the SRAM cells under process variation are represented in Fig. 7. DC analysis was used to obtain figures that show the overlapping transfer characteristics of the two cross-coupled inverters. In the figures, *q* is swiped, and *qb* is obtained, then *qb* is swiped, and *q* is acquired.

The most significant process variation in multi-diameter CNTFET-based designs is the CNT diameter variations which directly impact the bandgap of the CNTs and hence the threshold voltage of the CNTFETs. As a result, the Monte Carlo simulation has been conducted to assess the diameter and pitch variations with ± 10% Gaussian distributions and variation at the 6σ level.

The values of SNMs of the SRAMs for different voltage levels under process variations are reported in Table 5. According to the simulation results, the SNM of the proposed SRAM cell is larger than the other designs at 1 (0.3 v), and it is also acceptable in 0, 2, 3 values.

One of the parameters that affect the stability of SRAM cells is the pull-up ratio which is the ratio between sizes of the load transistor (pull up) to the size of the access transistor. Add stack transistor to pull-up network, decrease the strength of the pull-up transistor that determines the difficulty of flipping the state of the cell. With decreased pull-up ratio, it is easier to pull the node to GND, and hence the SNM is increased.

5.2.4 SRAM array

A 4 × 4 SRAM array using the proposed SRAM cell is presented as a testbed to show that the proposed circuit has correct functionality and is practical to design larger arithmetic blocks. The *WLs* shared in rows, and *QLs* are shared in columns.

To demonstrate the efficiency of the proposed SRAM cell, the results of simulations for the 4 × 4 SRAM array are shown in Table 6. The results show that the 4 × 4 SRAM array based on the proposed SRAM cell has significantly lower power consumption and read and write delay compared to the 4 × 4 SRAM array based on Refs. [20–24].

6 Conclusion

A low-power and robust CNTFET-based quaternary SRAM cell has been proposed for nanoelectronics. Obtaining the desired threshold voltage is a unique characteristic of CNTFET, making it appropriate for designing multiple-valued systems. Stacked CNTFETs are appropriately used in the proposed design to achieve a considerably low static

Table 4 Power consumption of the quaternary SRAM cells

Design	Average Power (μW)	Static Power (μW)
SRAM cell based on [20]	2.14	2.18
SRAM cell based on [21]	1.34	1.41
SRAM cell based on [22]	2.29	2.40
SRAM cell based on [23]	2.21	2.33
SRAM cell [24]	5.77	5.78
Proposed SRAM cell	1.02	1.05

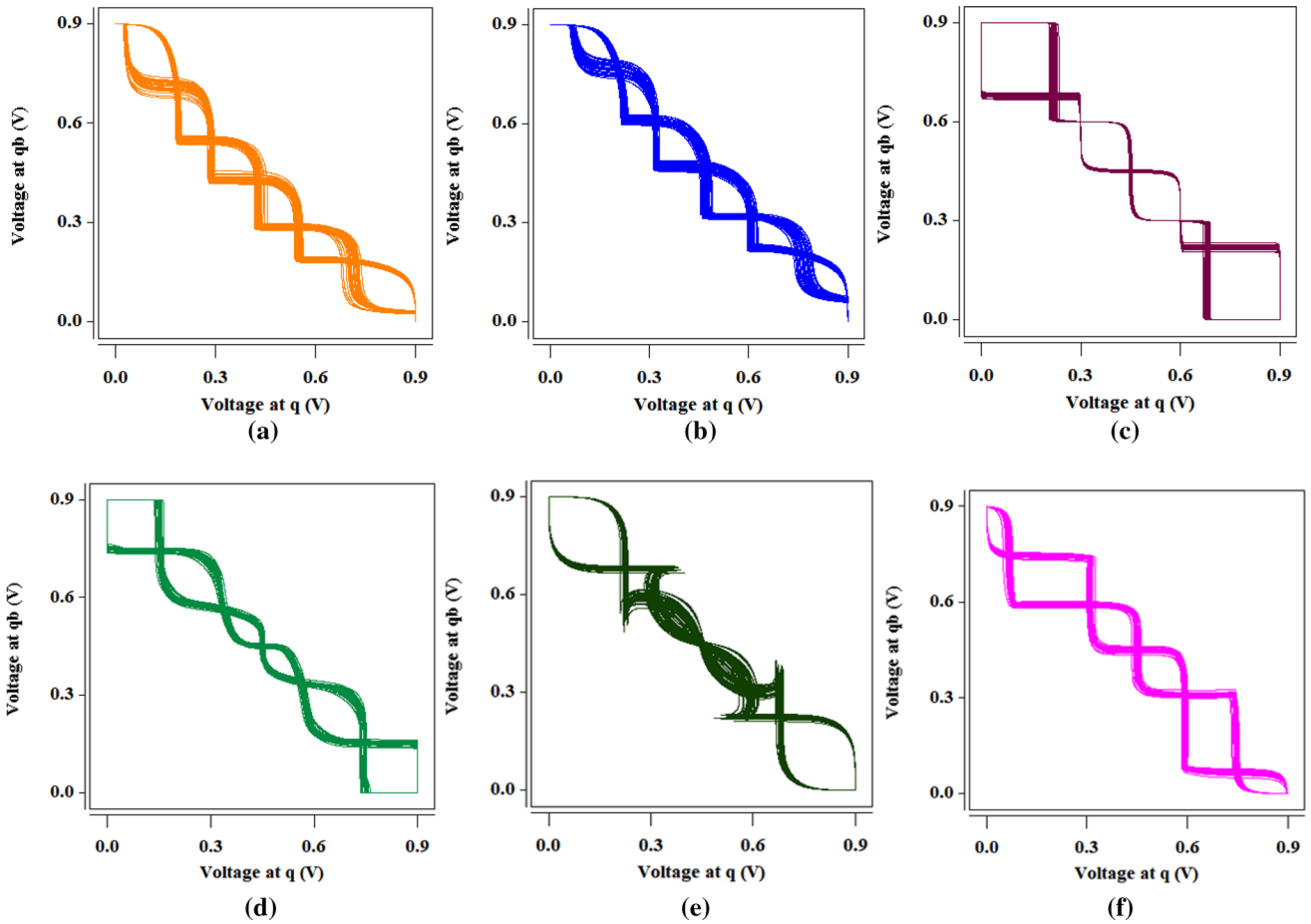

Fig. 7 DC analysis of the SRAM cells under process variations (**a**) Proposed design, (**b**) Design based on QI of [20] (**c**) Design based on QI of [21], (**d**) Design based on QI of [22], (**e**) Design based on QI of [23], (**f**) Design based on [24]

Table 5 SNM of the SRAM cells under process variations

Design	Logic '0'	Logic '1'	Logic '2'	Logic '3'
QI of [20]	61 mV	71 mV	98 mV	64 mV
QI of [21]	251 mV	63 mV	145 mV	284 mV
QI of [22]	193 mV	55 mV	65 mV	195 mV
QI of [23]	174 mv	58 mv	58 mV	185 mV
QI of [24]	56 mV	120 mV	120 mV	56 mV
The Proposed QI	124 mV	90 mV	96 mV	124 mV

power dissipation. Simulation results using HSPICE have been exposed that the proposed quaternary inverter and SRAM cell provide lower power consumption and comparable static noise margin and operate with robustness even in the presence of process variations. In addition, according to the simulation results, utilizing the proposed SRAM cell in designing a 4×4 SRAM array as a test bench has on average 56% lower power consumption and static power than their state-of-the-art counterparts and has a robustness that makes it suitable for energy-efficient systems.

Table 6 Parameter values of the quaternary SRAM Arrays

Design	Average Power (μW)	Static Power (μW)	Write (ps)	Read (ps)
SRAM Array based on [20]	35.20	35.07	2.5	0.58
SRAM Array based on [21]	23.22	23.05	2.6	0.59
SRAM Array based on [22]	39.04	38.96	2.7	0.46
SRAM Array based on [23]	37.7	37.3	2.8	0.47
SRAM Array based on [24]	88.1	88.8	3.6	0.76
Proposed SRAM Array	16.09	15.79	2.5	0.43

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Declarations

Conflict of interest Not applicable.

References

1. Dubrova, E. (1999). Multiple-valued logic in VLSI: challenges and opportunities. *Proceedings of NORCHIP*, 340–350.
2. Navi, K., Doostaregan, A., Moaiyeri, M. H., & Hashemipour, O. (2011). A hardware-friendly arithmetic method and efficient implementations for designing digital fuzzy adders. *Fuzzy Sets and Systems, 185*, 111–124. https://doi.org/10.1016/j.fss.2011.06.006
3. Raychowdhury, A., & Roy, K. (2005). Carbon-nanotube-based voltage-mode multiple-valued logic design. *IEEE Transactions on Nanotechnology, 4*, 168–179. https://doi.org/10.1109/TNANO.2004.842068
4. Moaiyeri, M. H., Doostaregan, A., & Navi, K. (2011). Design of energy-efficient and robust ternary circuits for nanotechnology. *IET Circuits, Devices & Systems, 5*, 285–296.
5. Reshadinezhad, M. R., Moaiyeri, M. H., & Navi, K. (2012). An energy-efficient full adder cell using CNFET technology. *IEICE Transactions on Electronics*. https://doi.org/10.1587/transele.E95.C.744
6. Lin, S., Kim, Y. B., & Lombard, F. (2012). Design of a ternary memory cell using CNTFETs. *IEEE Transactions on Nanotechnology, 11*, 1019–1025. https://doi.org/10.1109/TNANO.2012.2211614
7. Bala, S., & Khosla, M. (2019). Design and performance analysis of low-power SRAM based on electrostatically doped tunnel CNTFETs. *Journal of Computational Electronics, 18*, 856–863. https://doi.org/10.1007/s10825-019-01345-z
8. McEuen, P. L., Fuhrer, M., & Park, H. (2002). Single-walled carbon nanotube electronics. *IEEE Transactions on Nanotechnology, 99*, 78–85. https://doi.org/10.1109/TNANO.2002.1005429
9. Lin, S., Kim, Y. B., & Lombard, F. (2011). CNTFET-based design of ternary logic gates and arithmetic circuits. *IEEE Transactions on Nanotechnology, 10*, 217–225. https://doi.org/10.1109/TNANO.2009.2036845
10. Moaiyeri, M. H., Navi, K., & Hashemipour, O. (2012). Design and evaluation of CNFET-based quaternary circuits. *Circuits, Systems, and Signal Processing, 31*, 1631–1652. https://doi.org/10.1007/s00034-012-9413-2
11. Raychowdhury, A., & Roy, K. (2007). Carbon nanotube electronics: Design of high-performance and low-power digital circuits. *IEEE Transactions on Circuits and Systems I, 54*, 2391–2401. https://doi.org/10.1109/TCSI.2007.907799
12. Deng, J. (2007). Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nanotube field effect transistors. *Doctoral Dissertation. Stanford University*. https://doi.org/10.1109/TED.2007.909030
13. Lin, A., Patil, N., Roy, K., Badmaev, A., De Arco, L. G., Zhou, C., Mitra, S., & Wong, H. S. P. (2009). Threshold voltage and on-off ratio tuning for multiple-tube carbon nanotube FETs. *IEEE Transactions on Nanotechnology, 8*, 4–9. https://doi.org/10.1109/TNANO.2008.2004706
14. Wang, B., Poa, C. P., Wei, L., Li, L. J., Yang, Y., & Chen, Y. (2007). (n, m) selectivity of single-walled carbon nanotubes by different carbon precursors on Co-Mo catalysts. *Journal of the American Chemical Society, 129*(29), 9014–9019. https://doi.org/10.1021/ja070808k
15. Yang, F., Wang, X., Zhang, D., Yang, J., Luo, D., Xu, Z., Wei, J., Wang, J. Q., Xu, Z., Peng, F., et al. (2014). Chirality-specific growth of single-walled carbon nanotubes on solid alloy catalysts. *Nature, 510*, 522–524. https://doi.org/10.1038/nature13434
16. Bastani, N. H., Moaiyeri, M. H., & Navi, K. (2017). Carbon nanotube field effect transistor switching logic for designing efficient ternary arithmetic circuits. *Journal of Nanoelectronics and Optoelectronics, 12*(2), 118–129. https://doi.org/10.1166/jno.2017.1978
17. Khezeli, M. R., Moaiyeri, M. H., & Jalali, A. (2019). Comparative analysis of simultaneous switching noise effects in MWCNT bundle and Cu power interconnects in CNTFET-based ternary circuits. *IEEE Transactions on Very Large Scale Integration VLSI Systems, 27*(1), 37–46.
18. Khezeli, M. R., Jalali, A., & Moaiyeri, M. H. (2018). On the impacts of process and temperature variations on the crosstalk effects in MWCNT bundle nanointerconnects in ternary logic. *IEEE Transactions on Nanotechnology, 17*(2), 238–249. https://doi.org/10.1109/TNANO.2018.2789999
19. Khezeli, M. R., Moaiyeri, M. H., & Jalali, A. (2019). Active shielding of MWCNT bundle interconnects: An efficient approach to cancellation of crosstalk-induced functional failures in ternary logic. *IEEE Transactions on Electromagnetic Compatibility, 61*(1), 100–110. https://doi.org/10.1109/TEMC.2017.2788500
20. Liang, J., Chen, L., Han, J., & Lombardi, F. (2014). Design and evaluation of multiple valued logic gates using pseudo N-type carbon nanotube FETs. *IEEE Transactions on Nanotechnology, 13*, 695–708. https://doi.org/10.1109/TNANO.2014.2316000
21. Sharifi, F., Moaiyeri, M. H., Navi, K., & Bagherzadeh, N. (2015). Robust and energy-efficient carbon nanotube FET-based MVL gates: A novel design approach. *Microelectronics Journal, 46*(12), 1333–1342. https://doi.org/10.1016/j.mejo.2015.09.018
22. Doostaregan, A., & Abrishamifar, A. (2019). A new method for design of CNFET-based quaternary circuits. *Circuits, Systems, and Signal Processing*. https://doi.org/10.1007/s00034-018-0981-7
23. Daraei, A., & Hosseini, S. A. (2019). Novel energy-efficient and high-noise margin quaternary circuits in nanoelectronics. *AEU - International Journal of Electronics and Communications., 105*, 145–162. https://doi.org/10.1016/j.aeue.2019.04.012
24. Ghasemian, A., Abiri, E., Hassanli, K., & Darabi, A. (2022). HF-QSRAM: Half-select free quaternary SRAM design with required peripheral circuits for IoT/IoVT applications. *ECS Journal of Solid State Science and Technology*. https://doi.org/10.1149/2162-8777/ac4798
25. Prasad, G., Mandi, B. C., & Ali, M. (2020). Power optimized SRAM cell with high radiation hardened for aerospace applications. *Microelectronics Journal-Elsevier*. https://doi.org/10.1016/j.mejo.2020.104843
26. Prasad, G., Kumari, N., Mandi, B. C., & Ali, M. (2020). Design and statistical analysis of low power and high speed 10T static random access memory cell. *International Journal of Circuit Theory and Applications-Wiley, 48*(8), 1319–1328. https://doi.org/10.1002/cta.2802
27. Prasad, G. M., & BC., Ali, M. (2021). Low power and write enhancement RHBD 12T SRAM cell for aerospace applications. *Analog Integrated Circuits and Signal Processing-Springer*. https://doi.org/10.1007/s10470-020-01786-8
28. Venkatachalam, V., & Franz, M. (2005). Power reduction techniques for microprocessor systems. *ACM Computing Surveys, 37*(3), 195–237. https://doi.org/10.1145/1108956.1108957
29. Ye, Y., Borkar, S., & De, V. (1998). A new technique for standby leakage reduction in high-performance circuits. *1998 Symposium*

on VLSI Circuits. Digest of Technical Papers, 40–41. https://doi.org/10.1109/VLSIC.1998.687996
30. Nakata, S., Suzuki, H., Makino, H., Mutoh, S., Miyama, M., & Matsuda, Y. (2011). Increasing static noise margin of single-bit-line SRAM by lowering bit-line voltage during reading. *IEEE International Midwest Symposium on Circuits and Systems, Seoul, South Korea*. https://doi.org/10.1109/MWSCAS.2011.6026600
31. Deng, J., & Wong, H. S. P. (2007). A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application|Part I: Model of the intrinsic channel region. *IEEE Transactions on Electron Devices, 54*(12), 3186–3194. https://doi.org/10.1109/TED.2007.909030
32. Deng, J., & Wong, H. S. P. (2007). A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application|Part II: Full device model and circuit performance benchmarking. *IEEE Transactions on Electron Devices, 54*(12), 3195–3205. https://doi.org/10.1109/TED.2007.909043

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