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A 60-dB dynamic range two-stage RMS power detector

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Abstract
This study presents a true root-mean-square (RMS) power detector with a wide dynamic range in a 180-nm BiCMOS process. An RMS power detector based on a current feedback loop composed of two current-squaring cells and a transconductance amplifier is proposed and analysed. By placing the layout of two current-squaring cells symmetrically and setting the appropriate loop gain, the impact of the process mismatch on the dynamic range can be reduced, thus achieving a wide dynamic range of 34 dB from − 18 to 16 dBm at a 5 V supply voltage. A two-stage detector consisting of two identical RMS detectors and a preamplifier is also presented. The two-stage RMS detector demonstrates a dynamic range of 60 dB from − 44 to 16 dBm at 1.5 GHz with a ± 1.5 dB log error, making it suitable for both receiver and transmitter signal power detection.

Keywords Power detector · Root mean square (RMS) · Segmented power detection · Current feedback power detection

1 Introduction

Power detectors (PDs) are crucial components of radio frequency (RF) wireless transceivers. In the transmitter, PDs detect the output power of the power amplifier and help achieve automatic power control [1]. In the receiver, PDs are used to realise signal intensity indication and automatic gain control [2]. Owing to the large difference between the powers of the detected transmitted and received signals, the PD requires a considerable dynamic range to meet the requirements of transceivers. In modern wireless communication systems, high-peak-to-average ratio (PAPR) modulation schemes are widely used to improve spectral efficiency and increase data throughput. Among the various types of PDs, RMS PDs average the signal over time regardless of the signal's shape. Therefore, RMS PDs are suitable for the measurement of high-PAPR signals. However, they suffer from limited dynamic range [2–6].

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Various structures have been proposed to increase the dynamic range of the RMS PDs. In [2], the common source pairs and multi-DAC-based offset compensation was used to expand the dynamic range to 28 dB, with a maximum detection power of − 2 dBm. In [3], a balanced Wheatstone full-bridge structure with positive and negative thermistors was proposed, and a dynamic range of 23 dB was achieved. However, its minimum detection power, which is only 0dBm, was easily disturbed by thermal noise from the bulk. The work reported in [4] achieved a 34 dB dynamic range using diodes working at both positive and negative cycles. Nevertheless, the minimum detection power depended on the bias voltage of the diodes and was easily affected by process and power mismatch. Similarly, the PD in [1] with cascading gain amplifiers and squaring circuits also deviated from the ideal curve at lower end of the dynamic range owing to the mismatch.

As the dynamic range of a single RMS PD is limited, it is necessary to conduct research on multistage RMS PDs. A PD composed of a capacitor attenuation array and unbalanced source-coupled rectifiers was proposed in [5] to achieve a dynamic range of 45 dB, whereas its minimum detection power of − 10 dBm limits its application in the receiver. Another PD, including four gain amplifiers and four squaring circuits, was reported in [1], realising a dynamic range of over 40 dB with the help of a modem. Another method to achieve a wide dynamic range is to use

two parallel PDs with a modified output stage [6]. Despite its dynamic range of 47 dB, it suffered from a maximum detection power of no more than − 6 dBm, which limits the detection capabilities for high-power signals.

In this paper, an RMS current feedback power detector (CFPD) is proposed, which realises true RMS operation and provides a dynamic range of over 30 dB. By placing the layout of the two current-squaring cells symmetrically and setting the appropriate loop gain, the linearity of the PD at the lower end can be improved. Additionally, the dynamic range is extended by cascading two CFPDs and a preamplifier to over 60 dB from − 44 to 16 dBm at 1.5 GHz with a ± 1.5 dB log error, making it suitable for both receiver and transmitter signal power detection. Compared with previous works, the proposed two-stage RMS PD not only has a larger dynamic range but also simplifies the circuit design.

The remainder of this paper is organized as follows. The principle of the proposed RMS CFPD is analysed in detail in Sect. 2. Section 3 presents a two-stage RMS power detector based on the proposed CFPD. Additionally, the effect of the bias current I_0 on the loop gain and dynamic range is demonstrated. In Sect. 4, simulation and measurement results are presented and discussed. Finally, the conclusions are presented in Sect. 5.

2 RMS current feedback power detector analysis

This section elaborates on the operating principles of the proposed RMS CFPD. As shown in Fig. 1, the RMS CFPD is composed of an RF current-squaring cell (RF CSC), RMS current-squaring cell (RMS CSC), transconductance amplifier (TCA) and output buffer, turning the RF input wave into the RMS output voltage.

2.1 Current squaring cell

The current-squaring cell (CSC) is the core component of the entire CFPD. The schematic of the RF CSC is shown in

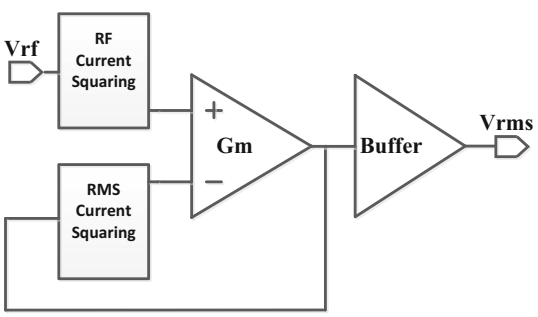


Fig. 1 Block diagram of proposed CFPD

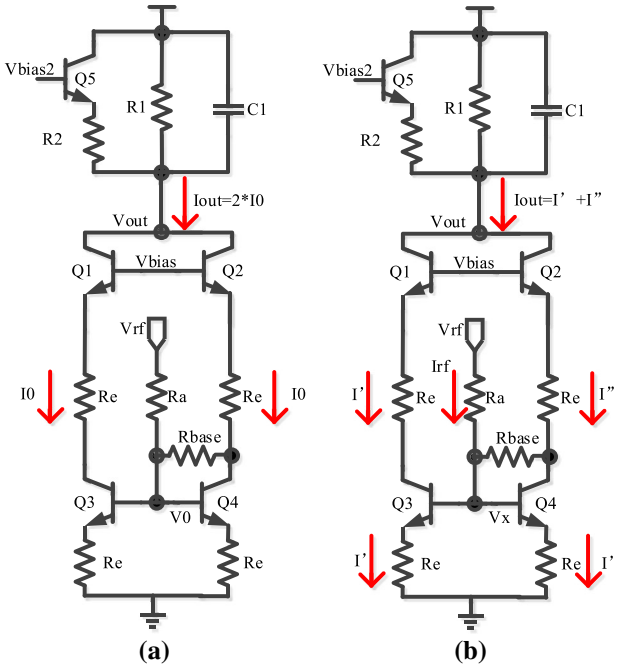


Fig. 2 Schematic of the RF CSC (**a**) no signal input (**b**) RF signal input

Fig. 2. The sizes of the transistors and the other components of the RF CSC are listed in Table 1.

It squares the input signal and filters it. Compared with the RF CSC, the RMS CSC has no filter capacitor C1 and operates in the DC state. The input impedance of the RF CSC is.

$$R_{in} = (R_e + 1/gm_{Q2})//(R_e + 1/gm_{Q4}) + R_a = \frac{R_e + V_T/I_0}{2} + R_a \quad (1)$$

where gm_{Q2} and gm_{Q4} are the transconductances of the transistors Q_2 and Q_4, respectively. I_0 is the bias current of $Q_2 \sim Q_4$ and V_T is the thermal voltage of the transistors. When the bias current I_0 is the PTAT current, the input impedance does not change with the temperature. The RF CSC acts as an impedance terminal and converts the voltage to current as:

Table 1 Size of transistors and other components of RF CSC

Components	Size
$Q_1 \sim Q_4$	200 nm*10 μm*3
Q_5	200 nm*10 μm *2
R_a	500 ohms
R_{base}	500 ohms
R_e	220 ohms
C_1	0.1 μF (off-chip)

$$I_{rf} = \frac{V_{rf}}{R_{in}} \tag{2}$$

When there is no signal input, the base bias voltage of Q_4, which is connected as a diode, is V_0, and the base bias voltages of Q_1 and Q_2 are V_{bias}. Ignoring the voltage drop on the resistors R_e and R_{base}, the following formulae can be obtained from the voltage-current relationship of the transistor:

$$I_0 = I_s * \exp(V_0/V_T) \tag{3}$$

$$I_0 = I_s * \exp[(V_{bias} - V_0)/V_T] \tag{4}$$

When there is an RF signal input, the base voltage of Q_4 becomes V_x, and the current flowing through the transistor Q_4 becomes I'. The current flowing through Q_2 becomes I''. The following formulae can then be obtained:

$$I' = I_s * \exp(V_x/V_T) \tag{5}$$

$$I'' = I_s * \exp[(V_{bias} - V_x)/V_T] \tag{6}$$

$$I' = I'' + I_{rf} \tag{7}$$

From (3), (4), (5), (6) to (7), the output current I_{OUT}, current gain A_I and squaring current I_{SQR} can be solved as follows:

$$I_{OUT} = I_0 * \sqrt{(I_{rf}/I_0)^2 + 4} \tag{8}$$

$$A_I = d_{I_{OUT}}/d_{I_{in}} = \left[\sqrt{1 + 4 * (I_0/I_{rf})^2}\right]^{-1} \tag{9}$$

$$I_{SQR} = I_{OUT} - 2 * I_0 = I_0 * \sqrt{(I_{rf}/I_0)^2 + 4} - 2 * I_0 \tag{10}$$

Expand (10) into Taylor series as:

$$I_{SQR} = I_0 * \left[2 + \frac{(I_{rf}/I_0)^2}{4} - \frac{(I_{rf}/I_0)^4}{64} + o(x^4)\right] - 2 * I_0 \approx I_{rf}^2/(4 * I_0),\ when\ |I_{rf}| << 4 * I_0 \tag{11}$$

Equation (11) shows that when $|I_{rf}| << 4 * I_0$, CSC squares the input current; when $|I_{rf}| >> 2 * I_0$, the absolute value of the input current is taken as:

$$I_{SQR} \approx |I_{rf}| - 2 * I_0, when |I_{rf}| >> 2 * I_0 \tag{12}$$

Properly increasing the R_a can reduce the input current, thereby increasing the maximum power that the power detector can detect. In the implementation, we chose R_a as 500 Ω. Transistor Q_5, resistors R_1, and R_2 form an active load circuit, and its AC impedance is

$$R_{load} = \left(\frac{R_1 * V_T + I_{OUT} * R_1 * R_2}{I_{OUT} * R_1 - V_T}\right)//R_1 \cong \left(\frac{V_T}{I_{OUT}} + R_2\right)//R_1 \tag{13}$$

As shown in (13), as the input power increases, R_{load} decreases to prevent V_{OUT} from falling too much to saturate the transistors $Q_1 \sim Q_4$ and cause the latter TCA to deviate from the operating point. Capacitor C_1 performs the role of signal filtering and shorts high-frequency components to the AC ground. Therefore, only the RF CSC of the entire current feedback loop works in the RF band, which greatly reduces the bandwidth requirements of the TCA and output buffer. The RMS CSC is completely symmetrical with the RF CSC and works in the DC state; therefore, the filter capacitor can be removed.

2.2 RMS power detector based on current feedback loop

As shown in Fig. 1, the entire CFPD includes a TCA and an output buffer in addition to the CSCs, as shown in Fig. 3.

Transistor Q_{12} replicates the feedback current and generates an RMS voltage on the resistor R_{13}, which is buffered after passing through the output buffer. The function of Q_{16} is to compensate for the input voltage drop of the RMS CSC so that the collector voltages of Q_{11} and Q_{12} are the same to achieve current matching. When the loop is established, the TCA has the same voltage at both input terminals, as follows:

$$mean\left|I_{rf}^2/(4 * I_0)\right| * R_{load} = I_{back}^2/(4 * I_0) * R_{load} \tag{14}$$

where I_{back} denotes the feedback current injected into the RMS CSC. The above formula can be simplified as:

$$I_{back} = \sqrt{mean\left(I_{rf}^2\right)} = \sqrt{mean\left(V_{rf}/R_{in}\right)^2} \tag{15}$$

set R_{13} the same as R_{in}, V_{rms} can be derived as

$$V_{rms} = (1 + R_{14}/R_{15}) * I_{back} * R_{in} = Gain_{buffer} * \sqrt{mean(V_{rf})^2} \tag{16}$$

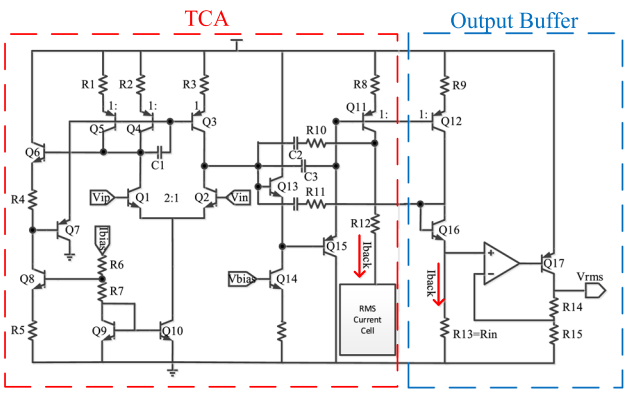


Fig. 3 TCA and an output buffer

Equation (16) indicates that the output voltage of the proposed CFPD is the true RMS value of the input RF signal. As described in [1], the process mismatch on CSCs causes the lower end of the conversion characteristic to deviate from the ideal curve. Therefore, the dynamic range was limited. In our proposed CFPD, the mismatch on both sides of Eq. (14) can be offset by placing the layout of the two CSCs totally symmetrically; thus, the dynamic range can be expanded.

3 Expanded dynamic structure based on CFPD

A segmented power detection method was used to expand the dynamic range. The proposed two-stage power detector in Fig. 4(a) consists of two CFPDs and a preamplifier, that adopts the Meyer structure [7], as shown in Fig. 4(b).

The reason for using the Meyer amplifier is that it can achieve a wide matching bandwidth. Its input impedance R_{in_amp} was designed to be 50 Ω by current and voltage feedback. A detailed derivation process can be found in [7]. The input impedance of the entire power detector is

$$R_{in\_whole} = R_{in}//R_{in\_amp} \cong R_{in\_amp} = 50\ \Omega \tag{17}$$

Therefore, the entire two-stage power detector can achieve broadband impedance matching without an additional matching network.

As shown in Fig. 4(a), for an RF input signal, two channels generate a DC output signal, namely, V_{OUTA} and V_{OUTB}. Unlike the method in [1], which requires a modem to determine which output should be used to estimate the signal power, the proposed scheme is very simple. When the signal power indicated by the high-power path is higher than its sensitivity, V_{OUTA} is used to indicate the signal power; otherwise, V_{OUTB} is used. This benefits from the wide dynamic range of the proposed CFPD. Otherwise, more gain stages are required, and each stage will have a corresponding DC output, which requires more complex discrimination methods.

To expand the dynamic range as much as possible, the two CFPDs must have the same transfer characteristics, which can be affected by the loop gain of the CFPD. The loop gain of the entire current feedback loop is

$$Gain_{LOOP} = \frac{\partial V_{feedback}}{\partial V_{diff}} \cong \frac{G_m^2 * R_{load} * V_{diff}}{I_0} \tag{18}$$

where G_m and V_{diff} are the transconductance and input voltage of the TCA, respectively. It can be seen from (11) that increasing I_0 also increases the maximum input power that is allowed by the square-law relationship. However, as (18) indicates, increase in I_0 also reduces the loop gain of the current feedback loop. Therefore, the feedback current cannot follow the input current exactly owing to the finite gain of TCA. This phenomenon is especially obvious when the input power is small. As shown in (18), the loop gain is proportional to V_{diff}. When a low-power signal is input, the initial V_{diff} is small, so the loop gain is much smaller than when a large signal is input.

In addition, the mismatch of the TCA with the finite gain affects the lower end of the dynamic range as the loop gain is small. This makes the transfer characteristics of the two CFPDs inconsistent, and the dynamic range is greatly restricted. Therefore, the size of the I_0 needs to be carefully selected, and a trade-off is made between the maximum detectable input power and the loop gain.

4 Measured results and discussion

The proposed RMS PD was designed and implemented using a 0.18 μm SiGe BiCMOS process. Figure 5 shows a photograph of the fabricated chip with an area of 2.15 mm × 2.59 mm, including four current feedback power detectors, six preamplifiers, and pads.

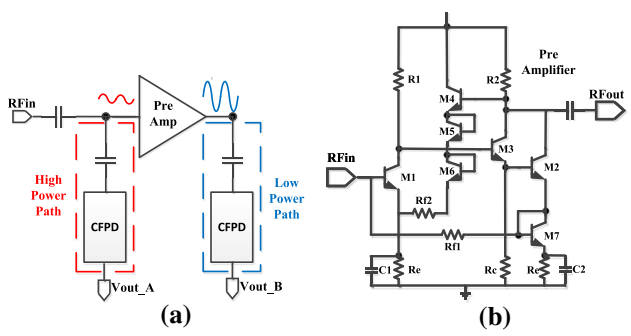


Fig. 4 Wide dynamic structure based on CFPDs: (**a**) proposed two-stage power detector (**b**) preamplifier using the Meyer structure

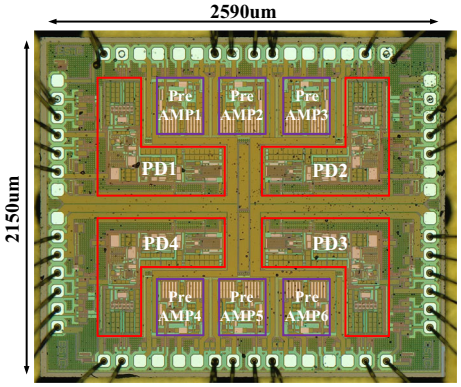


Fig. 5 Fabricated chip in 0.18 μm SiGe BiCMOS

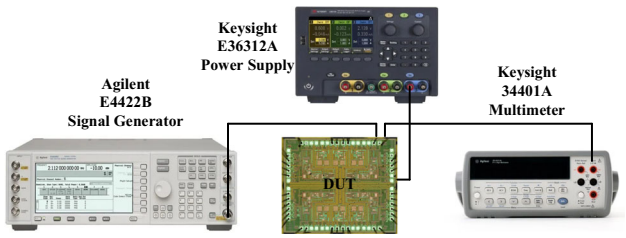


Fig. 6 Measurement setup of the proposed RMS power detector

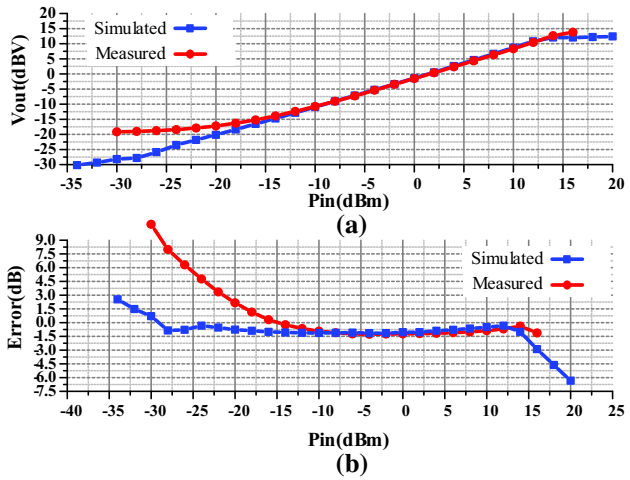


Fig. 7 The transfer characteristics and measurement error of a single CFPD measured at 1.5 GHz under a 5 V power supply

PD1, PD2, and PreAmp1 form a two-stage power detector, and the other components are used for auxiliary testing and can be removed to save area in actual applications. A single CFPD occupies an area of 0.43 mm^2 and consumes 3.39 mW at a 5 V supply voltage. The measurement setup is shown in Fig. 6. An Agilent E4422B signal generator was used as the input RF signal source, and the output DC voltage was measured using a Keysight 34401A multimeter.

The RMS power detection function was verified. Figure 7 shows the transfer characteristics and errors of a single CFPD, both measured and simulated at 1.5 GHz under a 5 V power supply.

The logarithmic-linear relationship between the output DC voltage and RF input power indicates the RMS operation of the proposed CFPD. The simulation result shows a dynamic range from − 32.5 to 15 dBm with a ± 1.5 dB error. The measurement result deviates from the simulated result at the lower end of the curve and achieves a dynamic range from − 18 to 16 dBm. As shown in [1] and formula (18), this is mainly caused by the process mismatch and limited loop gain in the cases of low-power signals, so that the feedback current cannot exactly follow the input current.

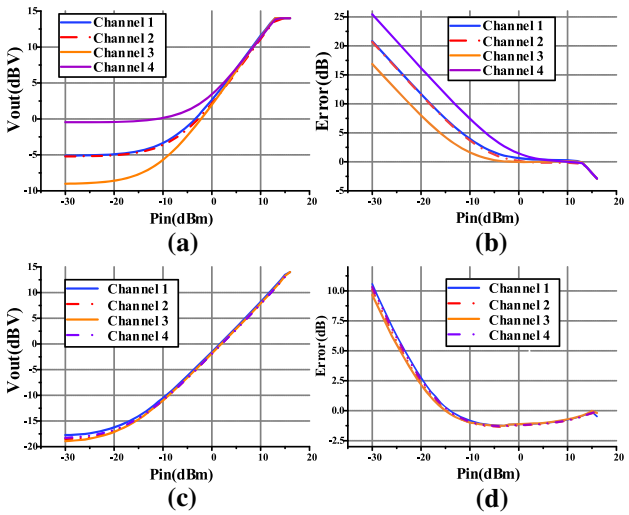


Fig. 8 four CFPDs measured at 1.5 GHz (**a**) transfer characteristics when I_0=150 μA (**b**) measurement error when I_0=150 μA (**c**) transfer characteristics when I_0=45 μA (**d**) measurement error when I_0=45 μA

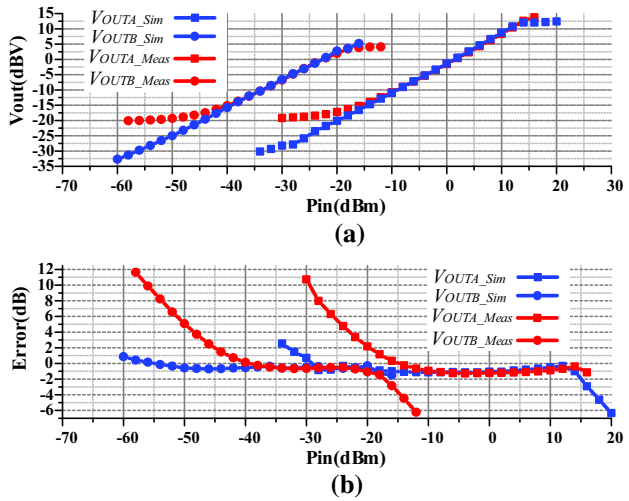


Fig. 9 Measurement of the proposed two-stage RMS power detector at 1.5 GHz (**a**) transfer characteristics (**b**) measurement error

Figure 8 illustrates the mismatch error between the four CFPDs at 1.5 GHz when I_0 is 150 and 45 μA. When I_0 is 150 μA, the maximum mismatch error between the four channels is larger than when I_0 is 45 μA. The mismatch is even worse when a low-power signal is input, as the loop gain becomes smaller under this condition, which is consistent with the theory in Sect. 3.

The new two-stage segmented RMS detector was simulated and measured with 1.5 GHz signals as shown in Fig. 9.

The simulation results show that it achieves a dynamic range from − 60 to 15 dBm with ± 1.5 dB log error. The horizontal distance between V_{OUTA} and V_{OUTB} is the gain of the preamplifier, which is 25 dB. The slope of the V_{OUTA}

Table 2 Comparison with published RMS power detectors

Ref	Freq (GHz)	Tech	Dynamic range (dB)	Minimum detectable power (dBm)	Maximum detectable power (dBm)
[1]	0.7–4	28 nm CMOS	44	− 39	5
[4]	8–12	65 nm CMOS	34	1	35
[5]	0.4–5	180 nm CMOS	45	− 10	35
[6]	2–40	130 nm BiCMOS	47	− 53	− 6
[8]	0.3–10	180 nm CMOS	42	− 12	30
[9]	0.5–3	130 nm CMOS	58	− 50	8
This work	0.1–1.5	180 nm	60	− 44	16

and V_{OUTB} is equal because a small I_0 is used to improve the loop gain and relieve the mismatch. The measured transfer curves of V_{OUTA} and V_{OUTB} overlap approximately − 18 dBm; therefore, the entire dynamic range is continuous from − 44 to 16 dBm. The reduction in the measured dynamic range is also caused by the process mismatch and limited loop gain when the input power is small. Nevertheless, by setting a reasonable loop gain, the proposed two-stage RMS power detector still has a dynamic range of 60 dB wider than that in previous works, making it suitable for both receiver and transmitter signal power detection. Table 2 summarises the results of the performance comparisons.

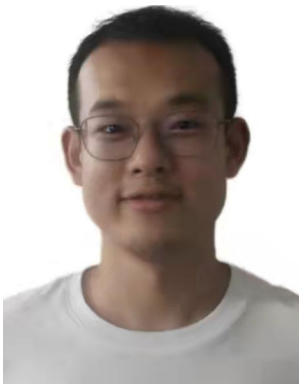
5 Conclusions

To increase the dynamic range of RMS PDs, this paper proposes a novel RMS PD based on a current feedback loop, which realises true RMS operation. The RMS CFPD is composed of an RF current-squaring cell, an RMS current-squaring cell, a transconductance amplifier, and an output buffer, turning the RF input wave into the RMS output voltage. By placing the layout of two current-squaring cells symmetrically and setting the appropriate loop gain, the linearity of the PD at the lower end can be improved, thus increasing the dynamic range. To extend the dynamic range further, a segmented power detection structure composed of two proposed CFPDs and a Meyer preamplifier was designed and implemented. Compared with previous works, the proposed two-stage RMS PD not only has a larger dynamic range but also simplifies the circuit design. Measurements show that this new two-stage RMS PD can work with signals up to 1.5 GHz and maintain the measurement error below ± 1.5 dB over a 60 dB dynamic range.

References

1. Choi, J., Lee, J., Xi, Y., Myoung, S. S., Baek, S., Kwon, D. H., Bui, Q. D., Lee, J., Oh, D., & Cho, T. B. (2016). Wide dynamic-range CMOS RMS power detector. *IEEE Transactions on Microwave Theory and Techniques, 64*(3), 868–880. https://doi.org/10.1109/TMTT.2016.2519030
2. Sejc, I., Popuri, S., & Sturm, J. (2018). Design of DAC based RMS power detector for RF applications. In *2018 Austrochip Workshop on Microelectronics (Austrochip)* (pp. 32–37). IEEE. https://doi.org/10.1109/Austrochip.2018.8520707.
3. Li, J. H., & Liao, X. (2021). A novel RF power detector based on positive and negative thermistors using standard CMOS technology. *IEEE Electron Device Letters*. https://doi.org/10.1109/LED.2021.3121285
4. Li, C., Yi, X., Boon, C. C., & Yang, K. (2019). A 34-dB dynamic range 0.7-mW compact switched-capacitor power detector in 65-nm CMOS. *IEEE Transactions on Power Electronics, 34*(10), 9365–9368. https://doi.org/10.1109/TPEL.2019.2908283
5. Hao, X., Zheng, Y., Tian, F., Zhou, Q., Li, H., Liu, Z., Liu, J., & Liao, H. (2019). A reverse-RSSI logarithmic power detector with+ 35-dBm maximum detectable power in 180-nm CMOS. *IEEE Microwave and Wireless Components Letters, 29*(9), 610–613. https://doi.org/10.1109/LMWC.2019.2933184
6. Gong, Y., Lee, S., Ying, H., Omprakash, A. P., Gebara, E., Gu, H., Nicholls, C., & Cressler, J. D. (2019). A broadband logarithmic power detector using 130 nm SiGe BiCMOS technology. In *2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)* (pp. 1–4). IEEE. https://doi.org/10.1109/BCICTS45179.2019.8972724.
7. Wu, T. H., Syu, J. S., & Meng, C. C. (2009). Analysis and design of the 0.13-um CMOS shunt-series series–shunt dual-feedback amplifier. *IEEE Transactions on Circuits and Systems I: Regular Papers, 56*(11), 2373–2383. https://doi.org/10.1109/TCSI.2009.2015603

8. Wang, J., Zheng, Y., Yang, F., Tian, F., & Liao, H. (2015). A wide band CMOS radio frequency RMS power detector with 42-dB dynamic range. In *2015 IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 1678–1681). IEEE. https://doi.org/10.1109/ISCAS.2015.7168974.
9. Varga, G., Wolf, B., van Rey, T., Ashok, A., & Heinen, S. (2016). Design of an integrated CMOS highly sensitive true RMS RF power detector for cognitive radio applications. In *2016 12th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME)* (pp. 1–4). IEEE. https://doi.org/10.1109/PRIME.2016.7519534.



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