A 9T high-stable and Low-Energy Half-Select-Free SRAM Cell Design using TMDFETs

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Abstract

The revolution in technology is so fast that even silicon devices are not able to meet the current demand of high speed, low power, and minimal area. The CMOS SRAM cells are the ones, affected the most by the revolutionary scaling of the devices. Due to various limitations of CMOS in deep sub-micron, new devices have emerged. One such device is the transition metal dichalcogenide field-effect transistor (TMDFET) to have prominent properties. This paper presents a novel read decoupled feedback-cutting 9T (RDFC9T) SRAM cell with high static noise margins (SNMs). The 16 nm CMOS and TMDFET devices are being used to design and compare the proposed design, showing the superiority of the TMDFET-based design. Furthermore, to evaluate the comparative performance of the proposed RDFC9T SRAM cell, it has been compared with the published SRAM cells introduced as 6T, 10T-P1, HFSE9T, and SB11T redesigned by 10 nm TMDFET device at V_{DD}=0.7 V. The suggested cell exhibits 3.20X and 1.71X/1.15X/5.26X higher read SNM and write SNM as compared to the 6T and 6T/HFSE9T/10T-P1 SRAM cells, respectively. The cell exhibits 1.11X/2.10X and 1.06X/1.30X smaller read delay (T_{RA}) and write delay (T_{WA}) than that of the HFSE9T/SB11T SRAM design, correspondingly. In terms of power performance, the RDFC9T cell shows 0.86X/0.68X and 0.56X/0.37X/0.35X less read power and write power than the SB11T/6T and SB11T/10T-P1/6T cell, respectively. Moreover, the proposed design shows robustness against harsh process variations and mitigates the half-select issues to support bit-interleaving architecture. Here, we have also shown the layout of the projected RDFC9T cell and a comparison with the published designs.

Keywords TMDFET · CMOS · SNM · Delay · SRAM

1 Introduction

The miniaturization of the devices leads to a tremendous rise in handheld devices, which leads to the requirements of low power consumption battery-operated devices (Tu, 2012). Lowering power dissipation in static random-access memory (SRAM) cells results in total power reduction in a system on chip (SoC). This reduction is significant as a fraction of the SoC is engaged by the SRAM cells (Oh, 2016). As, we know that supply voltage scaling (V_{DD}) is the simplest way to lower power consumption in the SRAM cells

because the static power and dynamic power reduce linearly and quadratically, respectively, with V_{DD} reduction (Roy, 2011). Still, the threshold voltage (V_{th}) of the transistor variation increases in the low V_{DD} domain due to the Random Dopant Fluctuation (RDF) and Line Edge roughness (LER), known as variation sources (Roy, 2011). As V_{th} is increasing in the low V_{DD}, the mismatch between the transistors in an SRAM cell is aggravated, resulting in read/write ability degradation (Agarwal, 2005). The researchers gave various solutions to these problems which lead to other problems, so people started thing about the new nanodevices. Various devices have been proposed out of which "Transition metal dichalcogenide field-effect transistor (TMDFET)", is as an evolving 2-dimensional (2-D) channel device, lessens the unwanted effects from process variation, which can be as a possible substitute device to silicon-based CMOS and other transistor structures (Gholipour, 2017a, b). Although, the TMDFETs show lots of advantages over CMOS (Gholipour, 2017a, b) (Gholipour, 2017a, b) (Chen, 2016) (Yu, 2015),

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when the memory cells are designed using it, the conventional 6T SRAM cell designed with TMDFETs still shows poor operational yield at a low V_{DD} due to the presence of read-write sizing requirements (Ahmad, 2017). Therefore, a new topology of the SRAM cell is required to increase the performance. For this reason, a number of SRAM cells have been recently projected in the literature. In conventional 8T SRAM cell (Chang, 2005), both two data storing nodes are separated from read bit line during the read operation to achieve read static noise margin (RSNM) as high as to hold static noise margin (HSNM). The differential read decoupled 9T SRAM cells have been proposed in(Kursun, 2008) to enhance RSNM. The same bit lines are used for the read and write operations. The number of transistors connected to the bit line are doubled and consequent, the read delay is increased. SRAM cells presented in(Gupta, 2018; Wang, 2014a, b) make use of a revised edition of the buffered read path for reducing the bit line leakage in the read access path and to increase RSNM. The use of Schmitt-trigger-based inverter in the SRAM cell design(Roy, 2011) increases the cell's stability and mitigates the process variation due to offering sharp voltage-transfer characteristic (VTC) and the existence of a feedback mechanism. In (Hasan, 2012), a transmission gate-based 8T SRAM cell was recommended to enhance the variability of the cell. However, this cell undergoes poor read stability. The addition of an add-on transistor in the pull-down path of the previous cell leads to a leakage power reduction of the cell, which was proposed by Roy and Islam (Islam, 2018). However, this cell cannot operate at low V_{DD} due to offering poor HSNM. The fully differential 8T SRAM cell designed in (Anh-Tuan, 2011) employs an additional inverter-based NAND gate to control access transistor and therefore eliminates the half-select issue induced by the conventional 6T SRAM cell. SRAM cells suggested in (Yadav, 2017)(Shin,2017) suffer from poor WSNM due to the use of series-connected NMOS access transistor with cross-section word lines (WLs) to support BI. Another Schmitt trigger based improved SRAM is proposed in (Gholipour, 2020) for IoT applications.

Single-ended SRAM cells show potentially low dynamic power because of a single bit line. Since bit lines have large capacitive loading especially for the sub-100 nm regime, the switching of bit line consumes a substantial amount of dynamic power consumption for the period of every read/write operation. Though, it increases read/write delay and writing '1'ability, at the identical time, reduces at low V_{DD} (Ahmad, 2017). SRAM cells recommended in (Izadinasab, 2021) and (Bayoumi, 2007) use "feedback cutting techniques" to enhance the write static noise margin (WSNM) but suffer from high write delay. A 7T cell, discussed in (Takeda, 2005), utilizes an optional extra transistor within one of the inverters and suffers from more possibilities of

hold failure. The power-gated technique used in 11T SRAM cell design (Pailly, 2020) disconnects the storage Q node from power rails during the write operation and therefore improves WSNM. The connection of several transistors to the same bit line increases read delay and dynamic power. Another 11T SRAM cell has been presented in (Golipour, 2021) to increase RSNM and WSNM simultaneously. These improvements are achieved by read decoupling and power cutoff techniques. Nonetheless, the cell suffers from high delay and power during the read operation related to high bit line overall capacitance.

Therefore, to address the above-mentioned challenges, a read-decoupled and feedback-cutting mechanism-based 9T (RDFC9T) SRAM cell is introduced. The suggested cell optimizes both RSNM and WSNM simultaneously and minimizes the leakage and dynamic power consumption. Moreover, the presented RDFC9T SRAM cell is robust against the PVT variations during read and write operation by showing a tighter spread in RSNM and WSNM. Furthermore, the half-select issues are removed by the proposed design for soft-error immune enhancement.

The paper is divided into the following sections: Sect. 2 presents the proposed RDFC9T SRAM cell and its operating procedure. The simulated results and analysis are shown in Sect. 3. Finally, Sect. 4 gives the conclusion of this research work.

2 Proposed RDFC9T SRAM cell design

2.1 Review of TMDFET Device

TMD monolayer is an emergent nanomaterial with a 2-D honeycomb lattice and robust thin-film structure (Gholipour, 2017a, b). It has a finite bandgap by nature, no need to further narrow down to be semiconducting. Due to this reason, the difficulty of production and the process variation effects are extremely reduced (Chen, 2016). The TMD materials with the chemical formula as MX_2, where transition metal is given as M (e.g. Mo, W) and chalcogen atom is represented as X. The highly reviewed TMD materials of MoS_2 and WSe_2 have a bandgap of 1.80 eV and 1.62 eV, respectively (Gholipour, 2017a, b).

Fig.1 demonstrates a monolayer MoS_2 comprising of a molybdenum atomic layer placed between two atomic layers of sulfur. The thickness of monolayer MoS_2 is 0.65 nm. Two major aspects of this monolayer material which makes it appropriate for transistors making are: (i) absence of dangling band, and (ii) high thermal stable structure (Gholipour, 2017a, b). The structure of a monolayer MoS_2-based transistor is demonstrated in Fig. 1(b). MoS_2 is used for the channel, and both source and drain electrodes are presumed
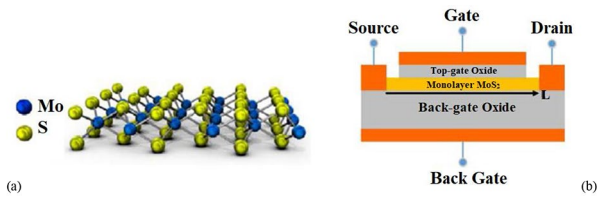
Fig. 1 (a) Structure of the monolayer MoS_2 and (b) structure of the monolayer MoS_2-based transistor structure (Gholipour, 2017a, b).

to be ohmic contacts. The top and the bottom gate vary the electrostatics in the channel, which are of metal. The reference point is the source.

2.2 Proposed Cell Structure

The diagram of the proposed Read Decoupled Feedback Cutting 9T SRAM cell is demonstrated in Fig. 2. It comprises of two normal cross-coupled inverters (INV1-INV2) pair that is the core of the memory cell. The inverted pairs are responsible for retaining the data stored in the two internal nodes Q and QB. The N1 transistor is a read and writes access transistor. The Column Control Selection Line (CSL) drives it. The columnar bit line (BL) is fed to the N1 transistor. The read decoupling transistor N4 is controlled by the QB node, which is connected between R1 and R2 nodes. One NMOS transistor ST is connected between R2 and ground, which is activated by a row-based read word line (RWL). The ST transistor is unique as it is a largerin size and is distributed by each row in a specific row. The N2 and N3 act as the write access transistors, are controlled by write word line (WWL). The transistor P1 is applied as feedback cutting FET, which is arranged between the two inverters. The three operations of the SRAM cell are Hold, Read & Write modes. The various control signals for various operations
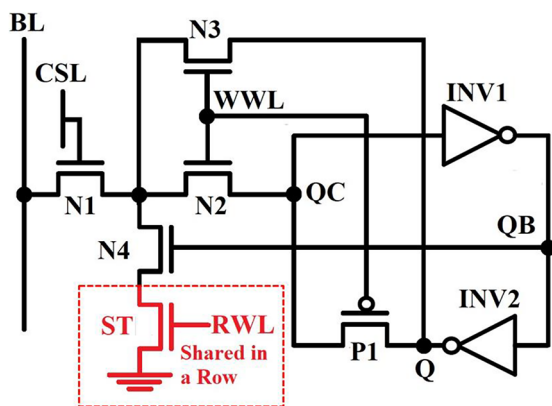
Fig. 2 Schematic of the proposed RDFC9T SRAM cell annotated with channel width to length ratio

are tabulated in Table 1. Distinct operations of the proposed SRAM cell is described below.

Hold Operation.

While the cell is in hold mode, the CSL and the WWL signals are maintained at GND to turn OFF the access transistors N1, N2, and N3 respectively. The BL signal is precharged to V_{DD} for reducing the leakage. For retaining the data through the feedback path, P1 is ON due to the WWL signal. The ST transistor is in an OFF state as RWL is set to GND thus maintains the data stored at nodes Q and QB as shown in Fig. 3.

2.3 Read Operation

For the read process, the WWL signal is kept at GND. This is done to eliminate the write path and to ensure that the feedback path exists P1 transistor is turned on. Once the BL is precharged to V_{DD} then the RWL is asserted. The data stored in the QB decided the charge stored on BL i.e., discharged or remains at V_{DD}. Let us consider that QB stores logic 1, which turns switches the N4 transistor to ON state. The BL signal is discharged to GND through the N1-N4-ST path (see Fig. 4), while if QB would have stored logic 0 the N4 is turned off and the BL will remain at V_{DD} (see Fig. 4). A sense amplifier (not shown) is utilized to sense a drop of 50 mV in the BL voltage for a reference voltage, hence completes the read operation.
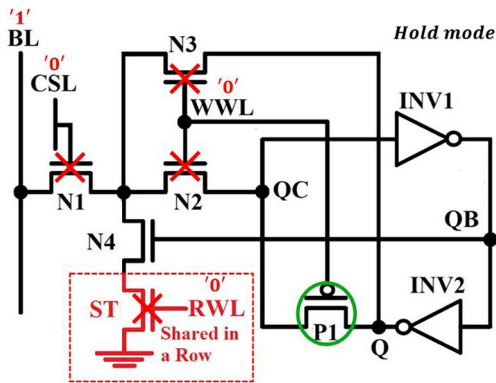
Write Operation.

The CSL and WWL signals are assereted to switch on the N1, N2, and N3 transistors for the write operation. The ST transistor is turned off as the RWL signal is placed at GND. The feedback path is now no longer exists as the P1 transistor is off due to the WWL signal which is set to V_{DD}. The braking of the feedback path is required for writing logic 1. If the path is not broken, writing of logic 1 is not possible, so the P1 transistor when switched off removes the feedback path formed by the cross-coupled inverters INV1 and INV2 for the successful writing of logic 1. Write driver (not shown) drives BL to V_{DD} for writing logic 1 or driven to GND for writing 0 to storage node Q.

Considering writing operation of logic 1 to node Q in which logic 0 is stored. The BL is set to V_{DD}, and this supply voltage is passed to node QC. The rise in the volatge level of QC node which changes INV1 output. So, the voltage level of output node QB rapidly falls from V_{DD}. Thus, this reduces the input voltage of the INV2. This will cause the output of the INV2 to rise which causes the node Q to rise results in the successful writing of logic 1 (see Fig. 5), while the node QB stores logic 0. Similarly, for logic 0 can be written in a complementary fashion as shown in Fig. 5 in (b) section. The N1-N3 transistor path is used to write data

Table 1 Level of control signals in different operations

Signals	Hold	Read	Write '1' @ Q	Write '0' @ Q
BL	1	Precharged	1	0
CSL	0	1	1	1
WWL	0	0	1	1
RWL	0	1	0	0

Fig. 3 Hold operation of the proposed RDFC9T SRAM cell
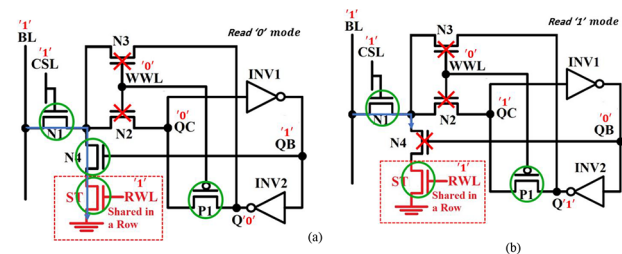
Fig. 4 (a) Read '0' operation and (b) read '1' operation of the proposed RDFC9T SRAM cell.

in the storing node, which increases the write operation pace and write-ability.

3 Simulation Setup and Result Analysis

This section presents the simulation results and discussion. First, we have compared the major design metrics of the proposed RDFC9T SRAM cell designed with 16 nm MOS-FET and TMDFET devices at 0.7 V supply voltage and room temperature of 25 °C. Then, the proposed RDFC9T SRAM cell has been designed using a 10 nm TMDFET device. The proposed cell's performance has been compared to the other recently published SRAM cells such as conventional 6T (as a basic cell), differential writing 10T (10T-P1) (Gupta, 2018), half-select single-ended 9T (HFSE9T) (Sharma, 2019), and single-bit line 11T (SB11T) (Pailly, 2020) SRAM cells redesigned by 10 nm TMDFET at the

same environmental conditions. The SPICE-compatible TMDFET device model developed in structure (Gholipour, 2017a, b) has been utilized for the simulations.

3.1 MOSFET Versus TMDFET

To study and evaluate the performance of the MOSFET and TMDFET devices, we have designed the proposed RDFC9T SRAM cell with the nano devices at 16 nm channel length. Since the proposed RDFC9T SRAM cell uses a separate read and writes path, it is free from the sizing requirements induced by the conventional 6T SRAM cell. Furthermore, the proposed SRAM cell shows high RSNM and WSNM due to read decoupled and feedback cutting techniques. Therefore, the minimum device size can be used. For this reason, the channel length and width of 10 nm have been chosen. The various parameters of MOSFET and TMDFET devices are given in Table 2. Fig.6 shows in (a) and (b) the drain-source current (I_{DS}) versus gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}), respectively for both two n-type devices at $V_{DD} = 0.7$ V. It is noted from the figures that the TMDFET device shows higher I_{ds} than the MOSFET device.

Table 3 comprehensively compares the stability, delay, dynamic power, PDP, and leakage power of the proposed RDFC9T SRAM cell designed with TMDFET and MOSFET devices at $V_{DD} = 0.7$ V. The read butterfly curves shown in Fig.7, in Fig. 7(a) compares the RSNM of the proposed RDFC9T SRAM cell designed with MOSFET and TMDFET devices at $V_{DD} = 0.7$ V. A 1.04X higher RSNM is attained by designing the proposed RDFC9T SRAM cell with TMDFET devices. Furthermore, the TMDFET-based proposed SRAM cell demonstrates 1.02X higher WSNM than that of the MOSFET-based one as shown in Fig. 7(b). These improvements are related to the better VTC of the TMDFET devices.

The proposed RDFC9T SRAM cell shows 3.56X/4.02X improvement in read/write delay when it is designed with TMDFET devices at $V_{DD} = 0.7$ V. This is due to the TMDFET devices shows higher I_{DS} than that of MOSFET as displayed in Fig. 6. Furthermore, the dynamic power of the
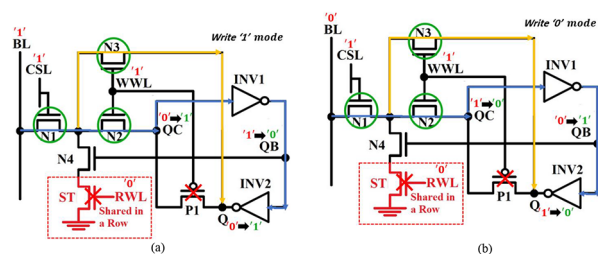
**Fig. 5** (a) Write '1' operation and (b) write '0' operation of the proposed RDFC9T SRAM cell.

Table 2 Parameters of MOSFET and TMDFET devices for simulation

parameters	Description	MOSFET	TMDFET
L	Channel length	16 n	16 n
W	Channel width	16 n	16 n
T_{ox}	Oxide thickness	0.95 n	0.95 n
T_{ox_2}	Back gate oxide thickness	-	10 n
?	Strain	-	0

Fig. 6 I_{DS} versus (a) V_{GS} and (b) V_{DS} for both n-type MOSFET and TMDFET devices at $V_{DD} = 0.7$ V.

TMDFET-proposed RDFC9T SRAM cell during read/write operation is decreased by 1.29X/1.50X. Due to the lower OFF-current in the TMDFET device compared to MOSFET one, the proposed RDFC9T SRAM cell designed with TMDFET dissipates 1.20X less leakage power. The TMDFET-proposed RDFC9T SRAM cell shows better read/write PDP compared to the MOSFET device as depicted in Table 3.

3.2 Proposed RDFC9T SRAM Cell Versus Other State-of-the-Art SRAM Cells

To estimate the comparative performance of the proposed RDFC9T SRAM cell in terms of major design metric, it is compared and analyzed with other SRAM cells including 6T, 10T-P1, HFSE10T, and SB11T. All these cells have been designed with 10 nm TMDFET devices. The parameter values of the TMDFET device used for the simulations are given in Table 4. As we know, the 6T SRAM is a single port where the read and write paths in the 6T SRAM cell are the same which creates a conflict between pairs of pull-down transistor and access transistor and pull-up transistor and access transistor. For the same reason, an improvement in the RSNM leads to degradation in the WSNM, and vice versa. Therefore, for acceptable RSNM and WSNM, the cell ratio ($CR = \left(\frac{W}{L}\right)_{pull-down} / \left(\frac{W}{L}\right)_{access}$) should be between 1.2 and 3 and the pull-up ratio ($PR = \left(\frac{W}{L}\right)_{pull-up} / \left(\frac{W}{L}\right)_{access}$) should be less than or equal to 1.8 [20]. For this reason, we have allocated a channel width of 30 nm and 20 nm to pull down and access transistors, respectively, to achieve CR=1.5. Furthermore, pull-up transistors have the same strength as access transistors to have PR=1. The other cells have been sized with this approach for a decent assessment. The channel width to channel length ratio (W/L) for every transistor of all the under-test SRAM cells has been annotated in Fig. 8.
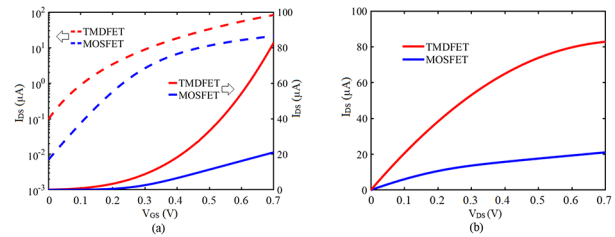
Table 5 gives a comprehensive comparison between the proposed RDFC9T, and other studied SRAM cells designed with 10 nm TMDFET devices in terms of stability, delay, dynamic power, leakage power, and PDP at 0.7 V supply voltage, and room temperature of 25 ˚C. The proposed SRAM cell and the other type of SRAM cells, except the 6T, show RSNM as good as HSNM due to the employment of read decoupling technique, which fully isolates the internal storing nodes Q and QB from the bit lines during the read operation. Fig.9 illustrates the read butterfly curves of all the compared SRAM cells at $V_{DD} = 0.7$ V. From Fig. 9(a), an improvement of 3.20X in the RSNM is observed in the proposed RDFC9T SRAM cell compared to the conventional 6T SRAM cell.

The proposed RDFC9T, HFSE9T, and SB11T SRAM cells utilize a single-ended writing structure. The writing '1' problem in these cells is eliminated by using the write-assist technique. Therefore, The WSNM for these SRAM cells is high. Two stacked transistors are present in its write path, the HFSE9T SRAM cell is showing 1.15X lower WSNM than two other SRAM cells as depicted in Fig. 9(b). This problem is removed in the projected SRAM cell by adding an extra write-access N3 transistor. The traditional 6T SRAM cell shows the second-best WSNM, which is 3.08X higher than the 10T-P1 SRAM cell.

The standard 6T SRAM cell utilizes the simple differential structure and therefore shows the lowest T_{RA} amongst all the examined SRAM cells. Other SRAM cells perform their read operation in form of single-ended cells. The SB11T SRAM cell has the highest T_{RA} between single-ended reading SRAM cells due to the connection of several FET devices to the same bit line, thus increases the overall bit line capacitance. This increment in turn slows the

Table 3 Table 2. Comparison between MOSFET- and TMDFET-based proposed SRAM cell in terms of major design metrics at $V_{DD} = 0.7$ V

Device type	HSNM (mV)	RSNM (mV)	WSNM (mV)	T_{RA} (ps)	T_{WA} (ps)	Read Power (nW)	Write Power (nW)	Leakage Power (nW)	Read PDP (e-17 sW)	Write PDP (e-21 sW)
MOSFET	180.7	180.7	345.3	162.67	120.86	201.88	517.31	41.18	32839.82	62522.087
TMDFET	187.3	187.3	351.5	45.65	30.10	156.41	345.38	34.25	7140.117	10395.938
Improvement	1.04X	1.04X	1.02X	3.56X	4.02X	1.3X	1.5X	1.20X	4.6X	6X
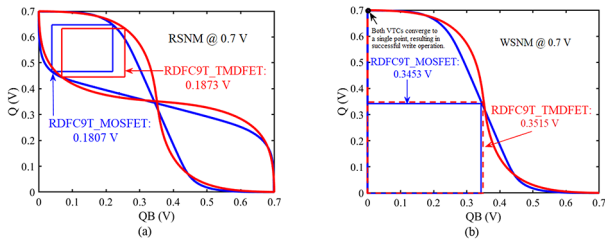
Fig. 7 (a) RSNM and (b) WSNM of the proposed RDFC SRAM cell designed with MOSFET and TMDFET devices at $V_{DD} = 0.7$ V.
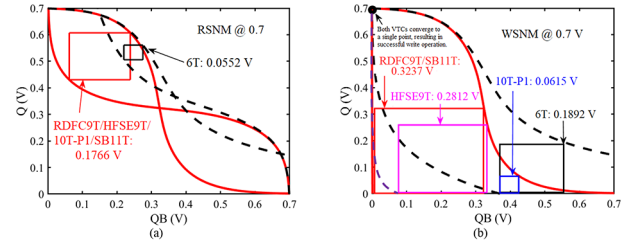
Fig. 9 (a) RSNM and (b) WSNM of all the compared SRAM cells designed with TMDFET devices at $V_{DD} = 0.7$ V.
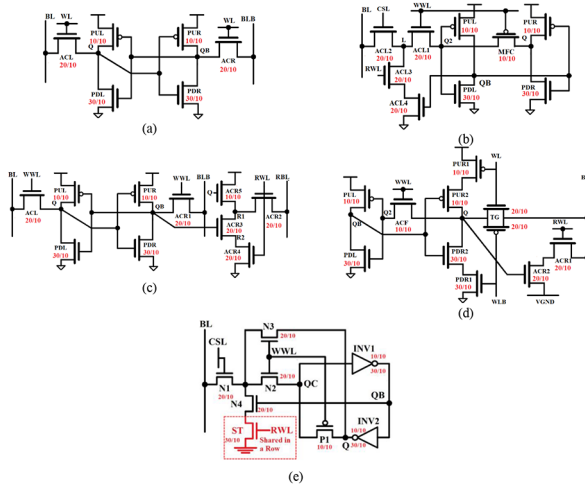
Fig. 8 Schematic of the under-test SRAM cells with annotated channel width to length ratio, (a) 6T, (b) HFSE9T, (c) 10T-P1, (d) SB11T, and (e) proposed RDFC9T

Table 4 Various parameters of TMDFET device for simulations

parameters	Description	TMDFET
L	Channel length	10 nm
W	Channel width	10, 20, and 30 nm
Tox	Top gate oxide thickness	2.8 nm
Tox_2	Back gate oxide thickness	10 nm
?	Strain	0

discharging rate of the bit line. Although the read path of the proposed RDFC, HFSE9T, 10T-P1 SRAM cells is the same, which consists of three stacked transistors, however,

the T_{RA} is reduced by 1.11X in the proposed cell. This is because the ST transistor in the proposed SRAM cell is distributed in a specified row entirely, and therefore it must be strong enough.

The conventional 6T and 10T-P1 SRAM cells use the same differential writing structure and therefore show the same lowest T_{WA} compared to all the studied SRAM cells. Other SRAM cells employ a single-ended writing structure with a write-assist technique. The SB11T SRAM cell has the highest T_{WA} due to having the highest overall bit line capacitance, as mentioned above. The proposed RDFC9T SRAM cell offers a 1.06X improvement in T_{WA} compared to the HFSE9T SRAM cell, which is because of the introduction of additional write-access N3 transistor to increase the writing '1' speed into the Q node.

The read and write power consumption in the conventional 6T SRAM cell is the highest due to its fully differential structure. The 10T-P1 SRAM cell employs a differential writing structure and shows the second highest write power. Since bit lines capacitance plays an important role in dynamic power consumption, the SB11T SRAM cell consumes higher read/write power than those of HFSE9T and proposed RDFC9T SRAM cells. The proposed RDFC9T SRAM cell offers higher read power than the 10T-P1 SRAM cell due to having lower T_{RA} and consumes equal write power when compared with the HFSE9T SRAM cell at $V_{DD} = 0.7$ V.

The employment of three-bit lines in the design of 10T-P1 SRAM cells increases the leakage power dissipation. Due to the stacked transistors in the read and write path and the single-ended structure, the proposed RDFC9T and

Table 5 Comparison of the proposed cell with the published works

Cells	HSNM (mV)	RSNM (mV)	WSNM (mV)	T_{RA} (ps)	T_{WA} (ps)	Read Power (nW)	Write Power (nW)	Leakage Power (nW)	Read PDP (e-21 sW)	Write PDP (e-21 sW)
6T	176.6	55.2	189.2	23.84	15.73	214.74	916.98	79.74	5119.4016	14424.0954
HFSE9T [16]	176.6	176.6	281.2	38.23	27.45	152.55	320.13	67.93	5831.9865	8787.5685
10T-P1 [1]	176.6	176.6	61.5	38.23	15.73	145.28	864.74	81.23	5709.504	14475.7476
SB11T [19]	176.6	176.6	323.7	72.06	33.68	170.50	571.36	72.69	12286.23	19243.4048
RDFC9T	176.6	176.6	323.7	34.34	25.90	146.94	320.13	67.29	5045.9196	8291.367

HFSE9T SRAM cells consume the lowest leakage power among all the compared SRAM cells. Still, the RDFC9T SRAM cell indicates 1.01X lower leakage power than the HFSE9T SRAM cell due to having an extra PMOS device, which minimizes leakage power, attributed to the hot-carrier injection mechanism in short-channel devices. The SB11T SRAM cell show higher leakage power after 6T SRAM cell. The higher leakage power observed in SB11T SRAM cells compared to proposed RDFC9T and HFSE9T SRAM cells is due to the introduction of an n-type-FET device inside the cross-coupled inverters pair, which increases the leakage current in the storage cell.

Definition of the metric of PDP makes a trade-off between delay and power. The proposed RDFC9T SRAM cell shows the lowest read/write PDP among all the under-test SRAM cells at $V_{DD} = 0.7$ V. This can be explained by the moderate performance of the proposed RDFC9T SRAM cell in terms of delay and power. On the other hand, the SB11T SRAM cell shows the highest read/write PDP due to its highest delay and power.

The studied SRAM cells are being compared in terms of area; their layouts have been implemented using 32 nm design rules. Fig.10 shows the layout of the proposed RDFC9T SRAM cell.

To study the effect of process variations on the SRAM cell's performance, we have done Monte-Carlo (MC) simulations with a sample size of 5,000. For this reason, we have considered the changes in channel length, channel width, and oxide thickness. All of these parameters are presumed to have an independent normal Gaussian distribution with a 3σ variation of 10% (Izadinasab, 2021). Fig.11 in (a) shows the distribution plot of RSNM for proposed RDFC9T and 6T SRAM cells to analyze the robustness of these SRAM cells during read operation. The proposed RDFC9T (6T) SRAM cell shows a Mean (μ) = 0.1766 V (0.0552 V) in addition to
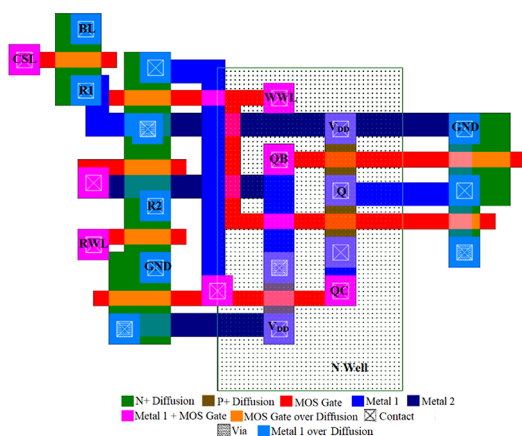
a standard deviation (σ) = 0.0027 V (0.0067 V), which provides a variability (σ/μ) of 0.015 (0.121). As a result, the proposed RDFC9T SRAM cell offers 8.07X lower variability in RSNM due to the employment of the read decoupling technique. Furthermore, the robustness of all the analyzed SRAM cells during a write operation is evaluated.

Fig.11(b) depicts the distribution plot of WSNM for the variou SRAM cells. The proposed RDFC9T SRAM cell reduces WSNM variability by 1.29X/6.00X/1.18X compared to 6T/10T-P1/HFSE9T. This is because of the use of the write-assist technique to mitigate the writing '1' problem induced by single-ended SRAM cells and the introduction of an additional write-access N3 transistor. Table 6. compares the variability of RSNM & WSNM of the proposed cell with the other cells.

3.3 Elimination of Half-Select Problem in Proposed RDFC9T SRAM Cell

The bit-interleaving architecture of the proposed RDFC9T SRAM cell is demonstrated in Fig.12, which is demonstrating a simplified 2×2 array designed by the proposed cell during a write operation. The proposed cell is placed at four different states: (1) selected cell, (2) row half-selected cell, (3) column half-selected cell, and (4) unselected cell. The selected and unselected cells behave as normal write and hold operations as discussed in the previous section. For the column half-selected cell, both write-access transistors N2 and N3 are turned off due to pulling down the WWL_1, which is row-based. This control signal, on the other hand, turns the write-assist transistor P1 on to establish the feedback path. Furthermore, the RWL_1 is also set to GND to
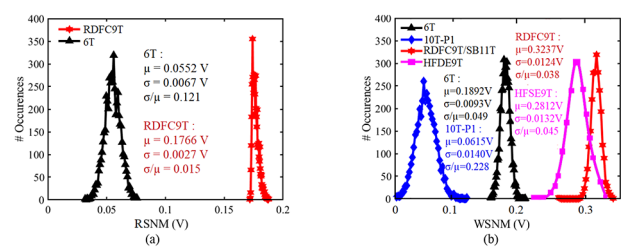

Fig. 11 Distribution plots of (a) RSNM and (b) WSNM for all the compared SRAM cells designed with TMDFET devices at $V_{DD} = 0.7$ V.

Fig. 10 Layout of the proposed RDFC9T SRAM cell drawn based on 32 nm design rules

Table 6 Variation of RSNM and WSNM of proposed cell with the other cells

SRAM Cells	RSNM variability	WSNM variability
6T	0.121	0.049
HFSE9T	0.015	0.045
10T-P1	0.015	0.228
SB11T	0.015	0.038
RDFC9T	0.015	0.038

turn off the transistor ST. Therefore, the internal storing nodes Q and QB are fully decoupled from the bit line and any disturbance paths to flip the initial state of them during a write operation in the selected cell. For the row half-selected cell, the read/write access transistor N1 is disabled due to placing the column-based control signal CSL_1 at a low logic level. Both N2/N3 and P1 transistors are at *ON* and *OFF* states, respectively, because the WWL_0 is at the high logic level. Furthermore, as the RWL_0 is pulled down, the ST transistor is turned off. Therefore, the cell core of the proposed cell is isolated from the bit line and other detrimental paths. However, miswriting may occur due to being the transistor P1 at OFF state. For this reason, Fig.13 illustrates the simulated results (MC simulation with 5000 samples) of the internal storing nodes Q and QB of the row half-selected while performing a write '0' and '1' operations in the selected cell. It can be observed that none of the internal nodes are flipped over 4 ns, which is a much longer time than write delay (T_{WA}). Furthermore, it is observed from Fig.14, which shows the butterfly curve of the row
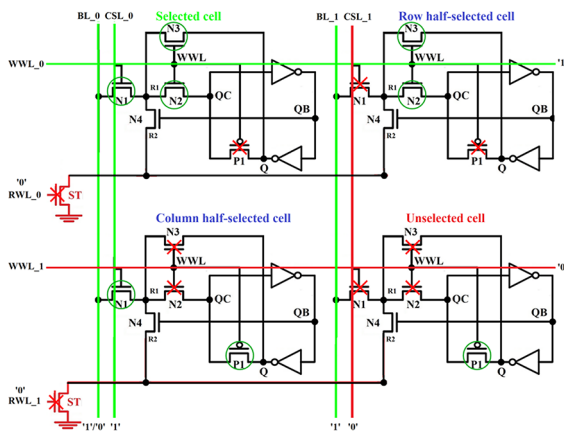

Fig. 14 SNMs of the row half-selected cell at $V_{DD} = 0.7$ V

half-selected cell during writing '1' operation in the selected cell, that the cell shows good static noise margin (SNM) to oppose the inversing of the nodes' initial values.

Moreover, the proposed RDFC9T SRAM cell is free from half-selected problems during read operation due to using column-based Bl and CSL and row-based RWL. This can be proven by the butterfly curve of the row half-selected cell as shown in Fig.14. This magnitude of SNM is enough to avoid the flipping of the stored values. Furthermore, this figure also shows the butterfly curve of the row half-selected cell during hold operation. This amount of SNM prevents data flip. Therefore, the suggested cell is free from half-selected problems.

4 Conclusions

In this article, an efficient, stable, and PVT invariant RDFC9T SRAM cell using TDMFET, and CMOS devices is proposed. The proposed RDFC9T SRAM cell is free from half-select problems, and so the Bit-Interleaving architecture can be used to increase soft-error immunity. The obtained results illustrate that the TDMFET-based design has better performance than the CMOS one. Designs based on TMD-FET devices imply that the proposed RDFC9T SRAM cell is more stable compared to other under test SRAM cells for the read and write operations. Furthermore, it has moderate operational delay and power, resulting in low PDP. When all the SRAM cells are exposed to harsh process variations, the proposed design shows lower variability during read/write operation.

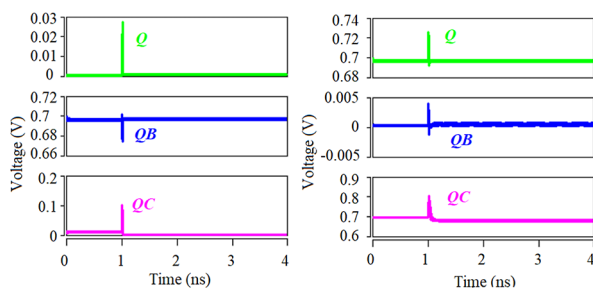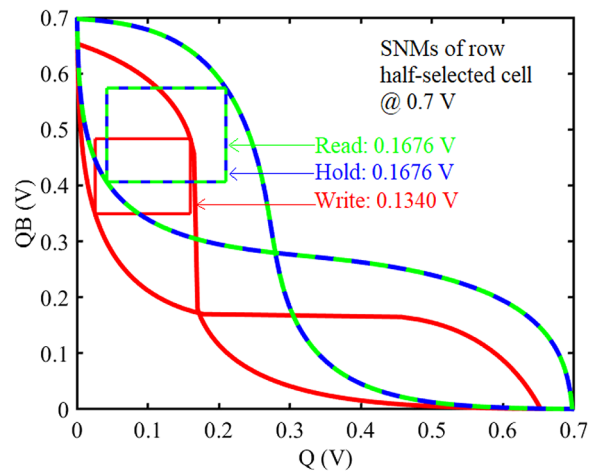**Fig. 12** The bit-interleaving architecture of the proposed RDFC9T SRAM cell

Fig. 13 Worst case voltages at node Q, QB, and QC of row-half selected cell during: **(Left)** writing '1' into Q in the selected cell and **(Right)** writing '0' into Q in the selected cell for MC = 5000 at $V_{DD} = 0.7$ V

Availability of data and material (data transparency)- The associated data will be made available on request.

Code Availability (software application or custom code)- The simulation work has been carried out using HSPICE software.

Declarations

Conflicts of interest/Competing interests- There is no conflict of interest at any stage.

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