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An innovative interconnect structure with improved Elmore delay estimation model for deep submicron technology

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Abstract
With advancements in technology, size and speed have been the important facet in VLSI interconnects. The channel length of the device reduces to tens of nanometers, as the technology is transferring to the deep submicron level. This leads to the requirement of long interconnects in VLSI chips. Interconnects are known as the basic building block that can vary from size to size. They provide a connection between two or more blocks and have scaling problems that an IC designer faces while designing. As scaling increases, the impact of interconnect in the VLSI circuits became even more important. It controls all the important electrical characteristics on the chip. With scale-down technology, interconnects not only become closer with each other but their dimensions also change which can directly impact the circuit parameters. Certain RC models have already been defined to control these parameters but in this paper, authors have proposed a new improved Elmore delay estimation model (RC) to reduce delay and power consumption in interconnect circuits. An optimized Elmore delay calculation was performed for uniform and non-uniform wires to reduce the time constant of the interconnect circuits. Further, the proposed model is estimated and verified theoretically. A new improved RC model is compared to the designed π-model that shows remarkable results. We also observed the linear relationship of power consumption and delay for both the RC models and found that in π-model, upon decreasing the length of wire the power first increases then decreases but in the proposed model, the power first increases then remain constant and then further increases upon increasing the length of wire. Our proposed model shows the remarkable values as the average percentage improvement of power is 75.167% and delay as 74.714% is achieved using a uniform distribution.

Keywords Interconnects · Delay · Power consumption · Copper · VLSI

1 Introduction

Interconnects are considered the basic building blocks of integrated circuits (IC) nowadays. These are the metal wiring which provides electrical connections among the active devices to transmit and distribute signals and power across the circuit. The rapid advancement of technology has resulted in more refined IC with minimum feature size requirements. But when the feature size of interconnecting wires scales down, the signal integrity issues start to dominate while improving the speed, power, area, and cost characteristics. As per International Technology Roadmap for Semiconductors (ITRS), future nanoscale circuits will contain more than a billion transistors and operate at a speed of over 10 GHz [1]. During the process of chip making, the individual components are fabricated on the chips after which these components are connected. But there remains no room to create all the connections, so the manufacturers build vertical layers or levels of interconnects. A complex IC can have 10 or more layers of interconnects. These multilevel metal structures not only rose higher and higher but also started to dominate the anatomy of IC. And due to this, interconnects started controlling the power, noise, timing, design functionality, and even reliability of the circuits. Interconnects can be local or global depending upon the performing function. Local interconnects are the first or the lowest level of interconnects which do not travels a long distance that is connecting two transistors within the same block. Whereas global

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interconnects are the highest level of interconnects and runs long distances. These generally include clocks, buses, power, or ground lines. With the increasing metal layers, it is important to connect the interconnect levels from one layer to the other. This connection is provided by vias which allow signals and power to be transmitted from one level to the other. Distribution of these long wires can be a challenging task as the performance parameters of high-speed IC highly depend on interconnects size and placement properties. Also, for the enhancement of performance parameters, different techniques can be approached.

Along with timing and power parameters, reduction in area is also considered to be an important factor. Also, the area is considered to obtain the approximate average length of the global interconnect. The length of interconnect depends on the area and the area depends on the geometry. Due to shrinking and high-speed requirement, interconnects constitute main problems of delay and noise because interconnects controls the design of the chips. If considered long wires, the time constant becomes quadratic concerning length. Along with the parameter degradation, many issues also arise from the layout designing. For a small size chip processing, interconnects are modeled first so that they consume less space and optimize the performance of the circuit. Still, as the feature size decreases many placement, floor planning and routing issues can occur in the circuit. To reduce these issues, different design levels and optimization techniques have been adopted. After proper wire sizing, interconnects can be modeled using different lumped interconnect models like L, π, and T-models. Generally, the π-model is preferred for distributed RC lines because of its advantages over the other two [2, 3]. When compared with L-model, π-model's delay tends to decrease by half, and when compared with T-model, though the delay is the same T-model has an extra node which complicates the delay calculations [2]. These lumped RC lines can be converted into distributed RC lines. In distributed RC lines, the long wire is divided into segments and each segment is modeled as L or π-type of RC circuit. For each segment, the total length (L) is also divided into individual segment length (Δl) according to the distribution and the value of total resistance and capacitance also gets distributed into individual segment values. These models can not only assist in determining the power consumption or delay of the system but also the crosstalk noise present in the system. The noise has also become one of the major factors in degrading the efficiency of the system. Along with the minimum noise factor, fast-speed circuits are of major significance as the technology gets improved. For today's technology, the circuit performance mostly depends on the performance of interconnects to achieve projected clock frequencies. For fast circuit designs, interconnect delay is the cognitive factor to determine circuit performance. For an RC line, the RC delay (τ) is calculated as the product of total resistance (R) and total capacitance (C). The most commonly used delay estimation model is the Elmore delay model. It provides an accurate estimation of delay in lumped models and can also be used for n-segments of a long wire.

Although Elmore delay estimation is the fastest estimation with less complexity, the only first moment of the impulse response is taken into account for delay calculations. There are other approaches in which higher-order moments are also considered for more accurate delay calculations with more analytical effort. Also, many other different models are taken into account other than the Elmore delay model for fast and accurate computation of the circuits. In [1], the authors have proposed an encoding scheme to achieve an overall reduction in power dissipation, delay, and coupling activity for on-chip buses. This encoding scheme reduces the number of overall transitions which reduces the worst-case crosstalk by reducing the coupling and switching activity. This reduction in switching activity also reduced the dynamic power dissipation of the system as compared to the initial sequence. In [3], various interconnect models and techniques adopted by different researchers to reduce the problem of crosstalk in circuits are reviewed. In [4], authors have reviewed the overall design flow of interconnect modeling in IC design including interconnect characterization, various 2D/3D field solvers, interconnect model library generation, and parameter extraction. They have also discussed statistical interconnect modeling. In [5], wire width planning has been studied for interconnects performance optimization in an interconnect-centric design flow. The authors have presented two simplified wire sizing schemes for VLSI optimization. In [6], authors have developed a set of interconnect delay estimation models with consideration of various layout optimizations including optimal wire-sizing (OWS), simultaneous driver and wire-sizing (SDWS), and simultaneous buffer insertion/sizing and wire-sizing (BISWS). In [7], a new algorithm is proposed for optimizing Elmore delay and layout design based on alphabetic trees. The alphabetic tree framework is quite general and can be used to solve routing problems such as power supply net routing. Further, they have compared different models and concluded that their algorithm runs much faster and can be used in a layout system for performance-driven interconnect design. In [8], authors have presented a 2π-model as a closed-form crosstalk structure. This approach helped them in solving layer assignment problems which further reduced the crosstalk noise. In [9], a wire sizing problem (WSP) is proposed using the Elmore delay model. In [10], the authors have analyzed the determinants of interconnect delay with the Elmore delay model. Further, the experiments are carried out at the stage of physical

circuit design. In [11], the authors provide a generalized approach to linear RLC/RC circuit response approximation. In this approach, the transient response is approximated by matching the initial boundary conditions and uses higher-order moments to construct a q-pole model which is also known as the Asymptotic Waveform Evaluation method. Although, this method can be accurate for delay estimation it also provides numerical instability. In [12], the D2M RC delay metric is proposed which is as simple and fast as the Elmore delay model but more accurate. The proposed metric behaves like the Elmore delay metric which generally overestimated delay but with consistently less error. It can be used in time-driven placements, interconnect synthesis, and global routing. In [13], authors have extended probability interpretation to circuit homogeneous response without requiring the time shift parameter. They have used gamma distribution to characterize a normalized homogeneous portion of the step response. Further, they demonstrated that when a table model is carefully constructed, the h-gamma approximation provides excellent improvement to that from model-order reduction but with run time complexity comparable to Elmore delay approximation with very little additional cost in terms of CPU time. It is probably stable for any RC mesh response. In [14], the authors have introduced a new boundary limiting the Elmore delay. This new improved Elmore delay problem is derived according to the compound interest problem of Jacob Bernoulli. In [15], the authors have presented some commonly used interconnect models and a set of interconnect designs and optimization techniques for improving interconnect performance and reliability. They have also presented a comparison of different optimization techniques in terms of their efficiency and optimization results. They have also discussed the trends and challenges of interconnect design as the technology feature size rapidly decreases to below 0.1 microns. In [16], a comparative study is done by the researchers about 3 different Elmore delay-based methodologies which provides better results as compared to the simple Elmore delay estimation model. First, the Scaled Elmore delay model which is the scaled version of the simple Elmore delay model by the factor of ln(2). Second, the effective capacitance model tries to deal with an effect that has become more evident in new technologies due to the rising of interconnect resistance. Last, the Fitted Elmore delay model is an attempt to adjust Elmore delay by adding coefficients to terms of the Elmore delay formula to get closer results with that of SPICE results. In [17], authors have presented an equivalent Elmore delay model for RLC trees. Closed-form solutions were observed for 50% delay, rise time, overshoot, and settling time of signals in RLC trees. The solutions presented have the same accuracy characteristics as compared to the Elmore delay model. In [18], a simple closed-form delay estimation interconnect structure is presented based on first and second-order moments that handle arbitrary voltages and conductance effects for a lumped and distributed line. In [19], authors have proved that the Elmore delay is an absolute upper bound on the 50% delay of an RC tree response. A lower bound on the delay is also developed using Elmore delay and the second moment of the impulse response. In [20], authors have outlined the importance of layer assignment over wire sizing and presents efficient techniques to perform concurrent buffer insertion and layer assignment to fix electrical and timing problems while maintaining speed. In [22], the author discusses the Elmore delay model which provides simplistic delay analysis that avoids time-consuming numerical integration/differential equations of RC network. In [23], the authors have proposed an improved Elmore delay model. This model is extracted by applying the Least Mean Square method on SPICE simulation results.

It is well known that circuit efficiency depends upon the performance of the system. A chip may contain many different blocks connected with each other. When one block performs its function faster, the performance of other blocks can vary due to the heat dissipation or functionality of each block. This performance variation can depend on various factors. But the major performance factors for deep sub-micron technologies depend due to the interconnects which connect these blocks. With the scaling of circuit parameters, the major issues occurring in the device depend highly on interconnects. Wires are not only used to connect these blocks with each other but also connect two or more transistors that are present inside these blocks. One of the main problems present in the circuits is a delay. The interconnect delay is calculated using resistance (R) and capacitance (C). Interconnect introduces some resistive and capacitive parasitic. These parasitic affect the performance of the circuits. Interconnect parasites increase the propagation delay of the circuit, can increase power dissipation and can add some extra noise to the circuits. One way to optimize the circuit performance is to properly design the layout of the interconnect system. The main and basic idea for the minimum delay is to keep the wire as short as possible. Although, interconnect layout design and wire sizing are two different things but both are studied altogether because wire sizing also focuses on reducing the parameters of the interconnects as small as possible. There can be different types of wire sizing uniform, non-uniform, tapered wire sizing, or continuous wire sizing [6, 6] which can enhance the speed of the system as well as solve the layer assignment problem for the circuit. π-model is also considered for layer assignment problems [8]. It not only reduces delay but can also reduce the number of layers in a chip. For simple π-RC interconnect circuits, Elmore delay

estimation is used widely which is one of the simple and accurate methods for delay calculation. But to optimize circuit performance more, this delay can be enhanced by using different techniques or methods [12, 13]. Besides Elmore delay uses the only first moment of the impulse response but it can also be calculated using higher order of the response [11]. Optimizing only delay is not sufficient to boost a circuit's performance. Power consumption and power dissipation both must be considered equally for proper functioning. Power dissipation is the maximum power that can be released without disturbing the performance of the system. It can be released in the form of heat. Power dissipation depends on the switching activity of the response. Due to more fast switching, the power also reduces which will reduce the thermal energy in the circuit thereby improving the reliability of the device. This switching can be controlled directly by using encoding methods [1]. Power consumption is also equally important while considering the total device parameters of the system. Power consumption is the power that is taken as input to drive the circuit. It depends directly on the current and voltage of the system. For lower voltages power consumption will be low i.e. power consumption can vary with the variation in voltages [18]. It is well learned that by proper wire sizing and improved Elmore delay estimation the propagation delay can be reduced. Also, by varying voltages the power consumption reduces. But the power consumption in a circuit is still unobserved if a long wire interconnect structure with different lengths is modeled with constant voltage and constant rising time.

It has been seen that Elmore delay estimation gives the accurate results of delay for monotonic step response. Also, the delay of interconnects can be improved using different techniques and can be structured differently to get maximum optimized results for the time constant. Moreover, it was seen that only delay was improving by using these techniques. Therefore, the focus of this paper is to restructure the interconnect circuit to optimize delay as well as power consumption by preserving the characteristics of the Elmore delay estimation model. In this paper, Elmore delay estimation (H-model) has been proposed for interconnects to reduce the time constant. Also, power consumption is given a priority to reduce with the decrease in interconnect length. In this research article, the authors have focused on the following:

- Wire geometry (uniform or non-uniform) along with the shrinking size of the circuits.
- Spacing between interconnects.
- Dielectric permittivity used for making interconnects.
- The resistivity of the material which is used to manufacture interconnects.

2 Proposed methodology

According to Moore's law, the number of transistors per silicon chip doubles every year. This law suggests faster, smaller, and more efficient circuits. With the advancement in technology, the size is also shrinking which increases the metal layers in the circuit. At this stage, interconnects control the timing, power, delay, noise even reliability of the circuits. This leads to the importance of interconnects. There are many reasons to stress the significance of interconnects in the circuits. Firstly, the authors have considered the wire geometry along with the shrinking size of the circuits. The main issues which are seen in the circuits are due to global interconnects. The scaling of global interconnects depends on the scaling factors. Three parameters are considered for wire sizing i.e. length (L), width (W), and thickness (T). The length of the long wires is independent of scaling and only width and thickness reduces by the factor s. Hence, the resistance of the long wires increases but the capacitance remains the same. This increase in wire resistance brings out an RC delay phenomenon. Second, the spacing issues which occur with technology, scale down. As the technology size decreases, the spacing between the interconnects also decreases. Today, the spacing between interconnects has been reduced to such an extent that the problem of coupling has started to degrade the performance of the circuits. This coupling not only introduces additional delay but also noise issues that can cause permanent circuit failure and to re-spin silicon [7]. This re-spin process is very expensive and time-consuming because if an error occurs in the design after fabrication, then the whole process must be repeated again. Third, interconnects are separated from each other by dielectric layers. The dielectric permittivity depends on the material used for making interconnects. Low-k dielectrics are preferred for wire insulation. Low-k material means materials with relatively low dielectric constant as compared to silicon-di-oxide. These materials are responsible for the continued scaling of technology. Replacing SiO_2 with low-k materials enables faster switching and low heat dissipation. SiO_2 was used as dielectric but many other materials when doped with SiO_2 gave lower dielectric constant values and are being used for better performance. The permittivity of unity that is air is also being used which is effective but produces fabrication and production cost challenges. Lastly, the resistivity of the material is used to manufacture interconnects. Previously, aluminum was used to make interconnects but later was switched to copper because copper provides better electrical conductivity as well as low resistivity. Due to this material change, some relaxation was seen in terms of power dissipation and delay but as technology further scaled down the problem of delay

persisted. Now the technology has scaled down so much that the resistivity of copper seems to be high enough to generate performance problems. To promote the better performance of the systems new materials must be tested and applied so that the circuits have faster switching and low power consumption.

The better performance also depends upon the structure used for interconnects. There can be three possible lumped models used for modeling interconnect structures that are *L*, *π,* and *T*. The *L* model is the simplest lumped model with total resistance (*R*) and total capacitance (*C*). The delay (τ) for the *L* model is computed as the product of total resistance and total capacitance (*RC*) which does not satisfy the Elmore delay estimation for long wires. So, this model is avoided. For the π-model, the capacitance is divided in half but the resistance remains the same. The delay for π-model is the product of total resistance and half of the total capacitance resulting τ as *RC*/2 which perfectly satisfies the Elmore delay estimation. Similarly, for the T model, the resistance gets divided by 2 but the capacitance remains the same. The delay for the *T* model also satisfies the Elmore delay estimation. The only difference between π and *T* model is that the *T* model has an extra node that may increase the number of calculations or make it more complex. As a result, the π-model is the popular model for a distributed RC line. Figure 1 shows the methodology used in this paper.

All these factors if computed correctly can reduce the time constant and can enhance the efficiency of the circuits. Also, power consumption must be considered because if power consumption becomes larger, circuits will tend to dissipate more heat which will ultimately cause a system failure. To evaluate delay for the circuits, the Elmore delay model is considered as it is simple and accurate for distributed RC lines. It allows us to explicitly express signal delay as a simple algebraic function of geometric parameters of interconnects so that it can be easily used for interconnect optimization [2]. Elmore delay gives results for input signal which is of a step function type. If the step response of the circuit is $h(t)$, 50% point delay of monotonic step response is the time T_d which satisfies Eq. (1) [14].

$$\int_0^{T_d} h(t)dt = 0.5 \tag{1}$$

In the Elmore delay model, T_d is approximated as the mean of the impulse response $h(t)$. If the impulse response is taken as the probability density function (pdf), the mean is defined as the first moment of the impulse response which is called τ_d is given by Eq. (2) [14].

$$\tau_d = \int_0^{\infty} th(t)dt \tag{2}$$

The first moment of the impulse response is commonly referred to as the Elmore delay. It represents the dominant time constant and a good estimate of delay in the circuit. Thus, for an *RC* ladder, the Elmore delay can be computed as given by Eq. (3) [7].

$$\tau_i = \sum_k (C_k \times R_{ik}), \tag{3}$$

where the node of interest is node *i*, C_k is the capacitance at node *k*, and R_{ik} is the sum of all the resistances in common from source to node *i* to the source to node *k*. Equation (4) illustrates the Elmore delay estimation for *n* number of segments.

$$\tau = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + - - - \\ - + (R_1 + R_2 + R_3 + - - + R_n)C_n \tag{4}$$

For long wires, the *RC* delay can be computed in terms of total wire resistance (*R*) and total wire capacitance (*C*). Figure 2 represents the *RC* ladder with *n* segments consisting of total wire length *L* and each segment of length is expressed as Δl, leading $L = n\Delta l$. The total wire resistance per unit length is expressed as *r* and total wire capacitance per unit length be *c*, then *R* is expressed as r × L, and *C* is expressed as $c \times L$ [7].

Using Elmore delay for π-model assuming n segments, the delay is calculated as:

$$\tau = (r\Delta l)(c\Delta l) + 2(r\Delta l)(c\Delta l) + 3(r\Delta l)(c\Delta l) + - - - \\ - + n(r\Delta l)(c\Delta l) \tag{5}$$

$$\tau = rc(\Delta l)^2[1 + 2 + 3 + - - - - - + n] \tag{6}$$

$$\tau = rc(\Delta l)^2\left[\frac{n(n+1)}{2}\right] \tag{7}$$

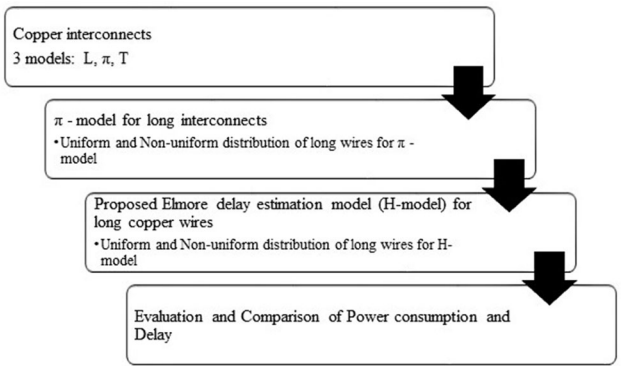


Fig. 1 Proposed Methodology

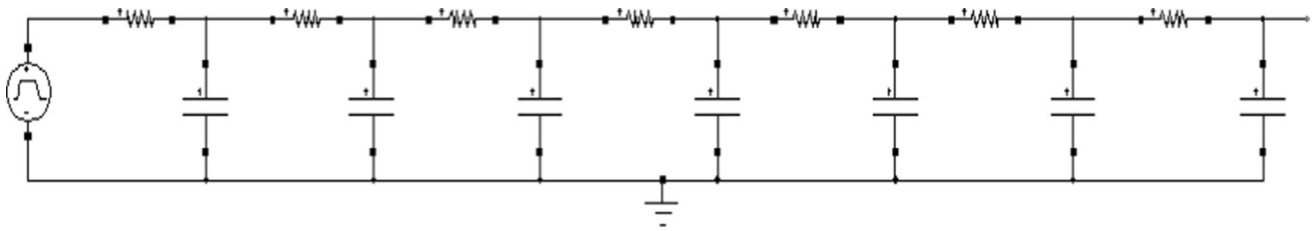


Fig. 2 RC ladder with n-segments

$$\tau = \frac{rcL^2(n+1)}{2n} \tag{8}$$

$$\tau = \frac{RC(n+1)}{2n} \tag{9}$$

For step response, n $\rightarrow \propto$

$$\tau = \frac{RC}{2} \tag{10}$$

From Eq. (8), it has been observed that for long wires the delay becomes quadratic (increases as the square of the length). To linearize this delay buffers are inserted in between the distributed RC line. The delay estimation after buffer insertion can become somewhat complex. To reduce this delay boosted by buffer insertion, the proper wire sizing is done along with buffer sizing. There are many ways in which buffer sizing can be done along with wire sizing which can be uniform or non-uniform. The distribution of long wire interconnect can be done uniformly and non-uniformly. To get the properly optimized values of power consumption, the length of the wire must be distributed uniformly. Uniform distribution of length means distributing each segment per unit length [shown in Fig. 3(a)] and for non-uniform distribution, the total number of segments are divided randomly [shown in Fig. 3(b)]. To evaluate the parameters for π-model with uniform and non-uniform distribution let's assume a 3 mm wire with a total resistance of 330 Ω and the total capacitance of 575fF. Figure 3 shows the uniform and non-uniform distribution of 3 mm wire. For uniform distribution, the wire is divided uniformly with 3 segments (n = 3). The value of each resistance is 110 Ω and the value of each capacitance is 95.83fF. For non-uniform distribution, the wire is divided into 2 segments (n = 2). The value of individual resistance is 165 Ω and individual capacitance is 143.75fF.

Although, the π-model structure is considered good for optimizing performance parameters power consumption keeps on increasing and decreasing to interconnect length. To obtain a more strict relation function of power for length authors have proposed the Elmore estimation delay model (H-model). Also, H-model linearly decreases the delay of the interconnect circuits by the factor of 4 because the total resistance of the wire is reducing by four times.

2.1 Proposed Elmore delay estimation model

From the above study, it has been revealed that π-model is considered better for the calculation of delay. The π-circuits can be further divided into 2π circuits or more to get more optimized values of power but delay remains almost constant. To get optimized values of power and delay, the authors have proposed the Elmore delay estimation model (H-model). For further optimization, the H model is divided into 2H-model. The proposed structure consists of one π-circuit which is further divided into two π-circuits. It has almost negligible complexity in structure and easy to simulate. The circuits are combined in such a way that one is combined in an upside-down position with the other one which not only substitutes the value of capacitance but of resistance also. Figure 4 shows the proposed Elmore delay Estimation model (H-model) structure.

The performance parameters are evaluated for different lengths of interconnect circuits which are considered from 1 to 10 mm. The values of total resistance and total capacitance are taken for different interconnect lengths are shown in Table 1 which are derived from Predictive

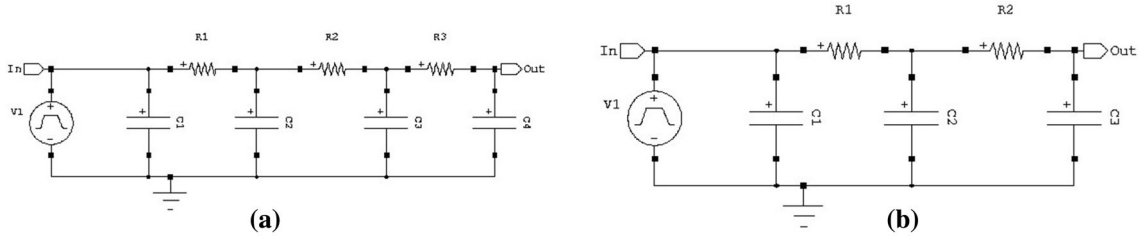


Fig. 3 **a** Uniform distribution of 3 mm wire for π-model. **b** Non-uniform distribution of 3 mm wire for π-model

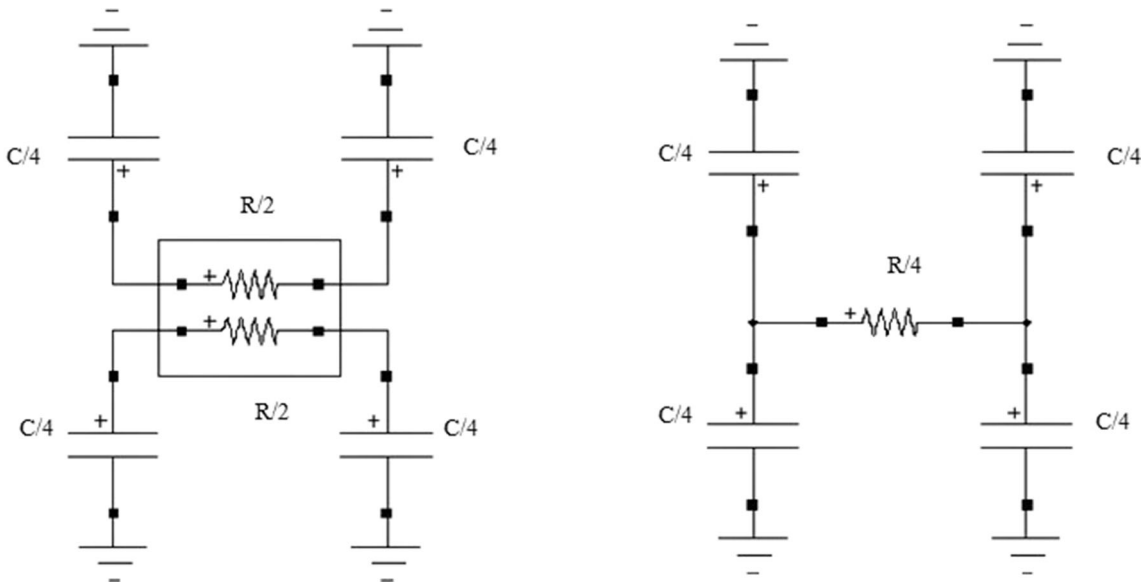


Fig. 4 H-model structure

Table 1 Different values of total resistance and capacitance for different lengths of interconnect

Length (mm)	Parameters	
	Resistance (Ω)	Capacitance (fF)
1	110	191
2	220	383
3	330	575
4	440	767
5	550	959
6	660	1150
7	770	1342
8	880	1534
9	990	1726
10	1100	1918

Technology Models (PTM) [20]. The width as 0.2 µm, thickness as 1 µm, height as 0.1 µm, spacing as 0.4 µm, and dielectric as 2 are kept the same for all the different lengths of interconnects.

When the two π-circuits are connected the resistance of the H-model is reduced by the factor of four. With the technology size decreasing, resistance plays an important role. With increased resistance, delay and power both increase because both have a direct relationship with resistance. In H-model, when the two π-circuits are connected parallel with each other, the resistance also becomes parallel with each other. As the single π-circuit is divided into two different circuits, the value of resistance gets divided among them. And, with the decrease in resistance, the performance parameters get optimized because power and delay directly depend on resistance. The total resistance of each segment of the H-model can be calculated as given by Eq. (11).

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} \tag{11}$$

Similarly for capacitance, although the total capacitance value remains the same for the circuit for each segment the value gets divided equally among them further reducing the capacitance value. Also, for long wires length remains constant only thickness and width reduces with technology scaling. This reduction results in the reduction of area. If area reduces capacitance also reduces because of the direct relationship between area and capacitance. This improves the overall speed of the circuits. The total capacitance of each segment is calculated using Eq. (12):

$$C = C_1 + C_2 \tag{12}$$

For example, for a 1 mm wire, the total resistance (R) as 110 Ω and total capacitance (C) as 191fF are considered. When the interconnect circuit is modeled using H-model, then according to Fig. 4, the resistance gets divided into two halves resulting in 55 Ω as each resistance value. The total value of resistance for the circuit is evaluated using Eq. (11) resulting in 27.5 Ω. Similarly, for capacitance, the value gets divided equally resulting47.74fFas each capacitance. Figure 5 shows the structure of interconnect with *n*-

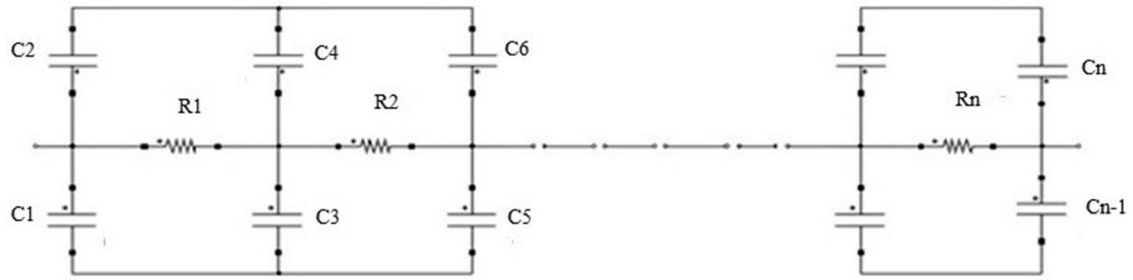


Fig. 5 Interconnect circuit using *H*-model for n-segments

segments using *the H*-model. Algorithm 1 explains the formation of the RC ladder using the proposed *H* model.

Algorithm 1: Novel Interconnect Structure for Delay and Power consumption using the proposed model.

Input: Interconnect

Output: Delay, Power consumption

Start

Step-1: Consider an interconnect length and evaluate total resistance and total capacitance for the circuit.

Step-2: Model a distributed RC line by distributing segments.

Step-3: Simulate the RC ladder using π-model for the considered length.

Step-4: Divide each π-segment into half.

Step-5: Place one π-circuit in an upside-down position with the other remaining half π-circuit in upright-position to form the alphabet H.

Step-6: Divide the value of resistance of each segment and evaluate the total resistance of each segment when connected in parallel.

Step-7: Distribute the value of total capacitance equally for each segment.

Step-8: Repeat steps 3 to 7 for all the segments in the RC ladder as shown in Fig. 5.

End

With the reduction in the total resistance of the interconnect circuit, the delay also reduces. This reduced delay does not match with the proposed Elmore delay estimation but provides the improved Elmore delay calculation. To evaluate the new improved Elmore delay, let's consider an *RC* ladder using *H*-model as shown in Fig. 3. The length (*L*) of the interconnect remains the same. For *n* segments, the length will be $L = \Delta l$. Let the total wire resistance per unit length be *r*/2 and total wire capacitance per unit length be *c*/2, then $R = rL/2$ and $C = cL/2$. This is because a segment of π-model is being divided into two parts, so the values of each segment resistance and capacitance also get divided.

Using Elmore delay assuming n-segments, the obtained equations are:

$$\tau = \left(\frac{r}{2}\Delta l\right)\left(\frac{c}{2}\Delta l\right) + 2\left(\frac{r}{2}\Delta l\right)\left(\frac{c}{2}\Delta l\right) + 3\left(\frac{r}{2}\Delta l\right)\left(\frac{c}{2}\Delta l\right) + - - - - + n\left(\frac{r}{2}\Delta l\right)\left(\frac{c}{2}\Delta l\right) \tag{13}$$

$$\tau = \frac{rc}{4}(\Delta l)^2[1 + 2 + 3 + - - - - + n] \tag{14}$$

$$\tau = \frac{rc}{4}(\Delta l)^2\left[\frac{n(n+1)}{2}\right] \tag{15}$$

$$\tau = \frac{rcL^2(n+1)}{8n} \tag{16}$$

$$\tau = \frac{RC(n+1)}{2n} \tag{17}$$

For step response, $n \to \infty$

$$\tau = \frac{RC}{8} \tag{18}$$

Thus, for an RC ladder the improved Elmore delay can be computed by Eq. (19):

$$\tau_i = \sum_k (2C_k \times R_{ik}), \tag{19}$$

where the node of interest is node *i*, $2C_k$ is the sum of all capacitances at node *k*, and R_{ik} is the sum of all the resistances in common from source to node *i* and source to node *k*. The Elmore delay estimation for *n* number of segments is given by Eq. (20).

$$\tau = R_1(C_A + C_a) + (R_1 + R_2)(C_B + C_b) + (R_1 + R_2 + R_3)(C_C + C_c) + - - - - + (R_1 + R_2 + R_3 + - - + R_n)(C_N + C_n) \tag{20}$$

The proposed model with improved Elmore delay estimation shows improvement in delay by four times as compared to existing Elmore delay calculations which help in increasing the overall speed of the interconnect circuit. Also, the reduction in resistance value by four times even when the capacitance remains the same for the circuit clearly shows the reduction in power consumption. This evidenced calculation shows the up-gradation of the

existing models. Hence, it can be said that along with the delay parameter power consumption also plays a vital role in circuit efficiency and reliability. Less power consumption will lead to less heat dissipation which will make the circuit live longer. Also, the circuit's reliability can be seen in terms of resistance and the time for which the current flows. The more the resistance and time constant more will be the heat dissipation and this resistance and delay can be made smaller with proper distribution of the wire.

H-model structures for interconnects are also divided as uniform and non-uniform distributions. To evaluate the parameters for *H*-model with uniform [shown in Fig. 6(a)] and non-uniform distribution [shown in Fig. 6(b)] let's assume a 3 mm wire again with total resistance 330 Ω and total capacitance 575fF. For uniform distribution, the wire is divided uniformly with 3 segments ($n = 3$). The value of each resistance is 27.5 Ω and the value of each capacitance is 47.915fF. For non-uniform distribution, the wire is divided into 2 segments ($n = 2$). The value of individual resistance is 41.25 Ω and individual capacitance is 71.875fF.

All the simulations were carried out in a system with Intel(R) Core(TM) i7-10700 CPU @ 2.90 GHz processor, 16.0 GB RAM using LTSPICE software. LTSPICE is software that is best suited for faster simulation of electronic circuits and power electronics. LTSPICE has good online community support. It is the widely used SW tool for simulation purposes, extremely simple to use, Light Weight, Rich in Component library, and free. It also allows adding off-the-shelf-components. Users just need to find or write the SPICE model of the respective component. LTSPICE is a whole other software tool that also uses SPICE to do its simulations but uses better algorithms, methods, and tricks to get simulations done faster with high accuracy than PSPICE.

3 Results and discussion

The long distributed wire can be converted into a lumped RC ladder structure with *n*-segments. The total resistance and total capacitance are the sums of all individual resistances and capacitances. This distribution can be done randomly that is whether the distribution to be done is uniform or non-uniform. To get the properly optimized values of power consumption, the length of the wire must be distributed uniformly.

3.1 Results of π-model

The distribution of long wire interconnect can be done uniformly and non-uniformly to obtain the properly optimized values of power consumption and delay. Uniform distribution of length means distributing each segment per unit length and for non-uniform distribution; the total number of segments is divided randomly. To evaluate the performance parameters for π-model with uniform and non-uniform distribution different lengths of interconnects are tabulated in Table 2. Uniform distribution is done by dividing values of resistance and capacitance per unit length. Non-uniform distribution is done randomly into segments. The interconnect circuits with these different lengths for both distributions are modeled and simulated in the SPICE tool. Further, the performance parameters are evaluated for both the distributions and are tabulated in Table 3.

According to Table 3 with SPICE calculations, in uniform distribution, power value first increases then decreases, and delay increases with an increase in length. But in non-uniform distribution, the power varies according to the number of segments done although delay remains almost the same as compared to the uniform distribution. When the interconnect circuit for 3 mm wire is simulated with

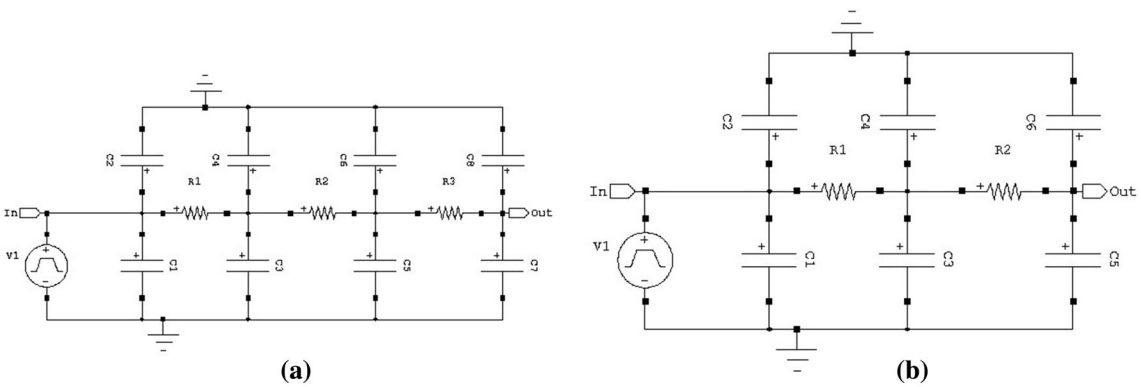


Fig. 6 **a** Uniform distribution of 3 mm wire for H-model. **b** Non-uniform distribution of 3 mm wire for H-model

Table 2 Uniform and non-uniform distribution of interconnect lengths for π-model

Length (mm)	Uniform distribution (No. of segments)	Non-uniform distribution (No. of segments)
2	2	1
3	3	2
6	6	3
7	7	4
7	7	3
10	10	6

Table 3 Performance parameters values for different interconnect lengths using π-model

Length (mm)	Uniform		Non-uniform	
	Power (W)	Delay	Power (W)	Delay
2	4.58×10^{-7}	42.10 ps	1.46×10^{-5}	84.26 ps
3	4.60×10^{-7}	94.87 ps	1.55×10^{-6}	94.87 ps
6	4.72×10^{-7}	379.36 ps	3.77×10^{-6}	379.46 ps
7	4.73×10^{-7}	516.26 ps	2.53×10^{-6}	516.28 ps
7 (with different number of the segment)	4.73×10^{-7}	516.26 ps	6.00×10^{-6}	515.96 ps
10	4.51×10^{-7}	1.03 ns	3.60×10^{-6}	1.03 ns

Table 4 Different lengths with individual resistance and capacitance values for π-model

Lengths (mm)	Total resistance (Ω)	Total capacitance (fF)	Individual resistance (Ω)	Individual capacitance (fF)
1	110	191	110	95.5
2	220	383	110	95.75
3	330	575	110	95.83
4	440	767	110	95.875
5	550	959	110	95.9
6	660	1150	110	95.83
7	770	1342	110	95.85
8	880	1534	110	95.875
9	990	1726	110	95.88
10	1100	1918	110	95.9

uniform distribution the observed delay is 94.87 ps and power consumed is 4.60×10^{-7} W while for non-uniform distribution the delay and power are 94.87 ps and 1.55×10^{-6} W respectively. It is noticed that for uniform distribution more optimized values are obtained in comparison to non-uniform distribution. The power consumed for 7 mm length when 3-segments are done is observed to be 6.00×10^{-6} W and delay to be 515.96 ps. It is presumed that the more the number of segments less will be the power consumed.

Considering uniform distribution, different lengths along with each segment resistance and capacitance values used for estimation of performance parameters for π-model are shown in Table 4. The total values of resistance and capacitance are derived from Predictive Technology Models (PTM) [21]. The individual values of resistance and capacitance can be obtained by dividing equal values to each resistance and capacitance. For example, for 2 mm wire total resistance is 220 Ω, and the total capacitance value is 383fF. Considering uniform distribution, the individual resistance (R/2) value will be 110 Ω and the individual capacitance (C/4) value will be 95.75fF because the total capacitance value gets divided among all the capacitances equally.

The simulations were performed and the performance parameters for each length are tabulated in Table 5. The structures are modeled considering values calculated in Table 4 along with the Elmore delay estimation.

Further for the π-model, the performance parameters are calculated theoretically using Elmore delay calculation which agrees with the simulated results. The collaborated results that are simulated and theoretical values of performance parameters are shown in Table 6.

Table 6 tabulates the delay percentage improvement of theoretical and simulated values. Percentage increase or

Table 5 Results for π-model

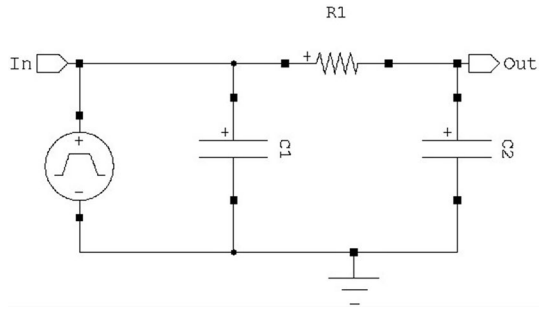
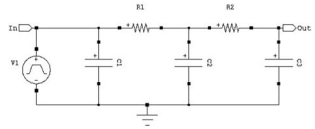
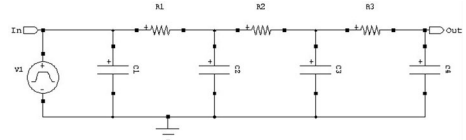
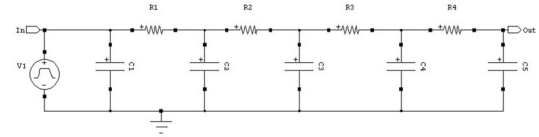
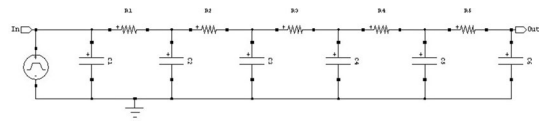
Length (mm)	Equation	Diagram	Power (W)	Delay
1	$\tau = \frac{RC}{2} = R_1C_2 = 10.5\,\text{ps}$		4.52×10^{-7}	10.66 ps
2	$\tau = \frac{RC}{2} = R_1C_2 + (R_1 + R_2)C_3 = 42.13\,\text{ps}$		4.58×10^{-7}	42.10 ps
3	$\tau = \frac{RC}{2} = R_1C_2 + (R_1 + R_2)C_3 + (R_1 + R_2 + R_3)C_4 = 94.87\,\text{ps}$		4.60×10^{-7}	94.87 ps
4	$\tau = \frac{RC}{2} = R_1C_2 + (R_1 + R_2)C_3 + (R_1 + R_2 + R_3)C_4 + (R_1 + R_2 + R_3 + R_4)C_5 = 168.74\,\text{ps}$		4.63×10^{-7}	168.71 ps
5	$\tau = \frac{RC}{2} = R_1C_2 + (R_1 + R_2)C_3 + (R_1 + R_2 + R_3)C_4 + (R_1 + R_2 + R_3 + R_4)C_5 + +(R_1 + R_2 + R_3 + R_4 + R_5)C_6 = 263.72\,\text{ps}$		4.68×10^{-7}	263.72 ps

Table 5 (continued)

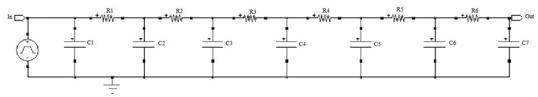
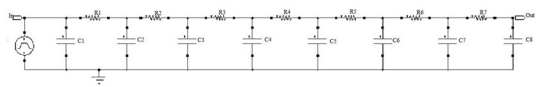
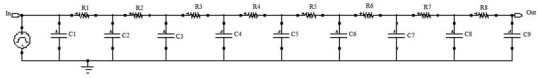
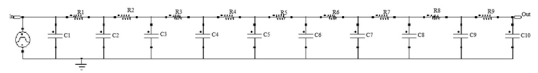
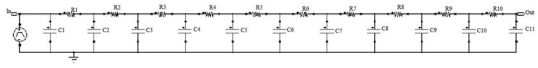
Length (mm)	Equation	Diagram	Power (W)	Delay
6	$\tau = \frac{RC}{2} = R_1C_2 + (R_1 + R_2)C_3 + (R_1 + R_2 + R_3)C_4 + (R_1 + R_2 + R_3 + R_4)C_5 + (R_1 + R_2 + R_3 + R_4 + R_5)C_6 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6)C_7 = 379.48\,\text{ps}$		4.72×10^{-7}	379.45 ps
7	$\tau = \frac{RC}{2} = R_1C_2 + (R_1 + R_2)C_3 + (R_1 + R_2 + R_3)C_4 + (R_1 + R_2 + R_3 + R_4)C_5 + (R_1 + R_2 + R_3 + R_4 + R_5)C_6 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6)C_7 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7)C_8 = 516.63\,\text{ps}$		4.73×10^{-7}	516.26 ps
8	$\tau = \frac{RC}{2} = R_1C_2 + (R_1 + R_2)C_3 + (R_1 + R_2 + R_3)C_4 + (R_1 + R_2 + R_3 + R_4)C_5 + + (R_1 + R_2 + R_3 + R_4 + R_5)C_6 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6)C_7 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7)C_8 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8)C_9 = 674.96\,\text{ps}$		4.71×10^{-7}	672.90 ps
9	$\tau = \frac{RC}{2} = R_1C_2 + (R_1 + R_2)C_3 + (R_1 + R_2 + R_3)C_4 + (R_1 + R_2 + R_3 + R_4)C_5 + (R_1 + R_2 + R_3 + R_4 + R_5)C_6 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6)C_7 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7)C_8 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8)C_9 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8 + R_9)C_{10} = 854.29\,\text{ps}$		4.63×10^{-7}	847.35 ps
10	$\tau = \frac{RC}{2} = R_1C_2 + (R_1 + R_2)C_3 + (R_1 + R_2 + R_3)C_4 + (R_1 + R_2 + R_3 + R_4)C_5 + (R_1 + R_2 + R_3 + R_4 + R_5)C_6 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6)C_7 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7)C_8 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8)C_9 + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8 + R_9)C_{10} + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8 + R_9 + R_{10})C_{11} = 1.05\,\text{ns}$		4.51×10^{-7}	1.03 ns

Table 6 Combined results of performance parameters for π-model

Length (mm)	Delay		Percentage improvement (%)
	Elmore estimation (Theoretical)	Simulated result	
1	10.5 ps	10.66 ps	1.5
2	42.13 ps	42.10 ps	0.07
3	94.87 ps	94.87 ps	0
4	168.74 ps	168.71 ps	0.01
5	263.72 ps	263.72 ps	0
6	379.48 ps	379.45 ps	0.007
7	516.63 ps	516.26 ps	0.07
8	674.96 ps	672.90 ps	0.3
9	854.29 ps	847.35 ps	0.8
10	1.05 ns	1.03 ns	1.9

decrease refers to the change in percent value to the extent to which a variable loses magnitude or value. The simulated values show the better computation of the interconnect circuits with less delay as compared to the calculated ones, though both the values are somewhat similar. Also, from the evaluated values, the performance parameters can be varied according to the lengths of interconnects. Figure 7 shows the variations of power concerning interconnect length and delay concerning interconnect length.

The power and delay graphs represent the linear relationship of power and delay with the increase in interconnect length. For the power consumption graph, the value first increases steadily with the increase in length and then steadily decreases as the length increases. For the delay graph, the value keeps on increasing with the

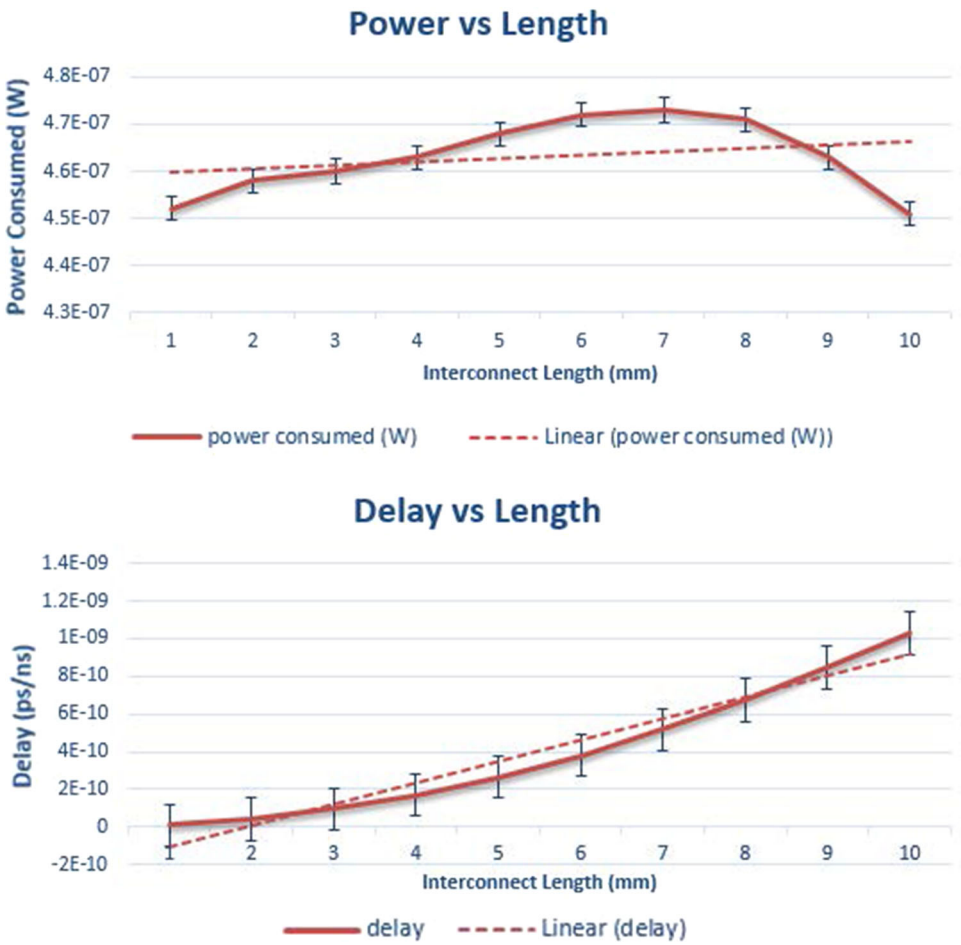


Fig. 7 Power and delay vs length graphs

Table 7 Performance parameters values for different interconnect lengths using H-model

Length (mm)	Uniform		Non-uniform	
	Power (W)	Delay (ps)	Power (W)	Delay (ps)
2	1.13×10^{-7}	10.75	9.09×10^{-7}	10.69
3	1.14×10^{-7}	23.68	3.86×10^{-7}	23.69
6	1.15×10^{-7}	94.87	8.26×10^{-6}	94.87
6 (with different number of the segment)	1.15×10^{-7}	94.87	1.98×10^{-7}	94.88
7	1.15×10^{-7}	129.15	6.18×10^{-7}	129.16
10	1.17×10^{-7}	263.72	5.42×10^{-7}	263.68

Table 8 Different lengths with individual resistance and capacitance values for H-model

Lengths (mm)	Total resistance (Ω)	Total capacitance (fF)	Individual resistance (Ω)	Individual capacitance (fF)
1	110	191	27.5	47.75
2	220	383	27.5	47.875
3	330	575	27.5	47.915
4	440	767	27.5	47.9375
5	550	959	27.5	47.95
6	660	1150	27.5	47.915
7	770	1342	27.5	47.925
8	880	1534	27.5	47.9375
9	990	1726	27.5	47.94
10	1100	1918	27.5	47.95

increase in length. Also, the linear relationship represents in the graphs shows a positive slope. The delay can be seen strictly increasing with the increase in length which clearly shows the monotonic nature of the response leading to the proposal of the H-model. In this paper, different lengths of interconnects are modeled and simulated using the proposed H-model for global interconnects.

3.2 Results of proposed H-model

For H-model, the distribution can also be done uniformly as well as non-uniformly. To evaluate the performance parameters for H-model with uniform and non-uniform distribution, different lengths of interconnects are considered the same as π-model (shown in Table 2). Uniform distribution is done by dividing values of resistance and capacitance per unit length. Non-uniform distribution is done randomly into segments.

The interconnect circuits with these different lengths for both distributions are modeled and simulated in the SPICE tool. Further, the performance parameters are evaluated for both the distributions and are shown in Table 7.

When the interconnect circuit for 3 mm wire is simulated using SPICE tool with uniform distribution the delay observed is 23.68 ps and power consumed to be 1.14×10^{-7} W. While when simulated with non-uniform distribution the delay and power observed are 23.69 ps and 3.86×10^{-7} W respectively. It is noticed that with uniform distribution more optimized values are obtained as compared to non-uniform distribution. From Table 7 it has been inferred that for uniform distribution, power consumption and delay increases with an increase in length but for non-uniform distribution, the power varies according to the number of segments done although delay remains almost the same as compared to the uniform distribution. Using H-model, the values for delay remain almost constant but the power consumption plays an important role. The power consumed for 6 mm length when 5-segments are done is observed to be 1.98×10^{-7} W and delay to be 94.88 ps. Hence, it is confirmed that the more the number of segments less will be the power consumed and delay values.

With uniform distribution, of H-model an optimized value of power consumption and delay is obtained. It has been observed that power consumption is increasing linearly with an increase in interconnect length. And, in comparison with the π-model, a more optimized value of power consumption and delay is obtained for the proposed H-model. In this paper, a new Elmore delay calculation is done to confirm the theoretical aspect of the circuit design. Equations (18) and (20) show the computation of Elmore delay for H-model structures and found the most popular

Table 9 Performance evaluation for H-model<colspec colnum="4" colname="c4" align="left""/>

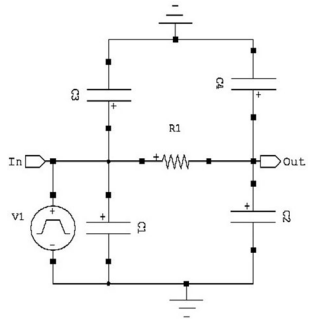
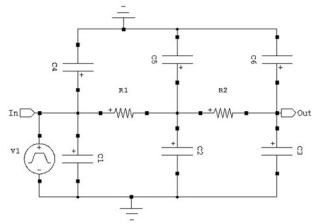
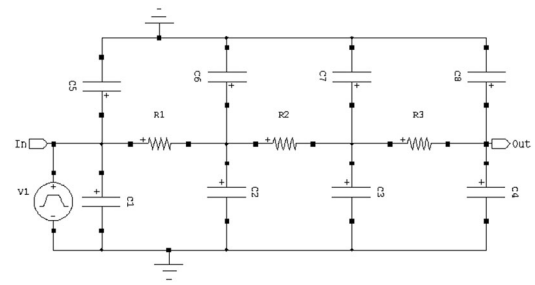
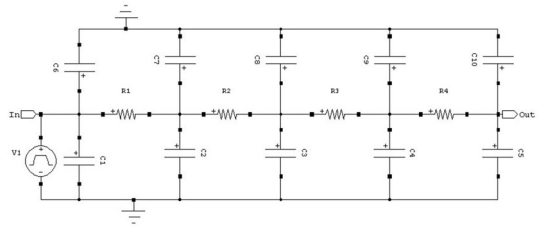
Length (mm)	Equation	Diagram	Power (W)	Delay (ps)
1	$\tau = \frac{RC}{8} = R_1(C_2 + C_4) = 2.62\,\text{ps}$		1.13×10^{-7}	2.82
2	$\tau = \frac{RC}{8} = R_1(C_2 + C_5) + (R_1 + R_2)(C_3 + C_6) = 10.53\,\text{ps}$		1.13×10^{-7}	10.75
3	$\tau = \frac{RC}{8} = R_1(C_2 + C_6) + (R_1 + R_2)(C_3 + C_7) + (R_1 + R_2 + R_3)(C_4 + C_8) = 23.71\,\text{ps}$		1.14×10^{-7}	23.68
4	$\tau = \frac{RC}{8} = R_1(C_2 + C_7) + (R_1 + R_2)(C_3 + C_8) + (R_1 + R_2 + R_3)(C_4 + C_9) + (R_1 + R_2 + R_3 + R_4)(C_5 + C_{10}) = 41.22\,\text{ps}$		1.15×10^{-7}	42.14

Table 9 (continued)

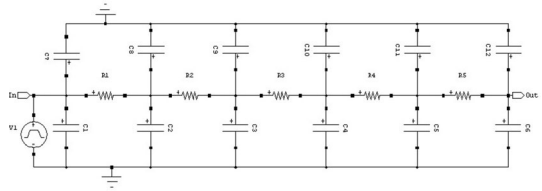
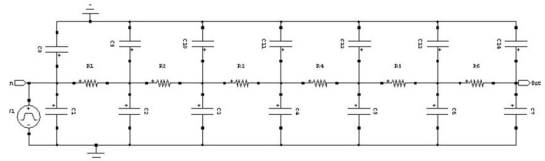
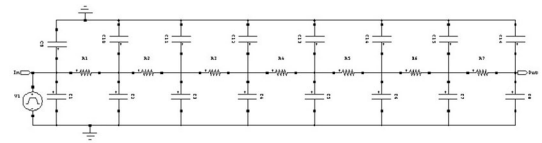
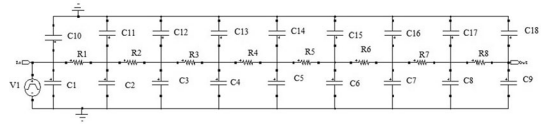
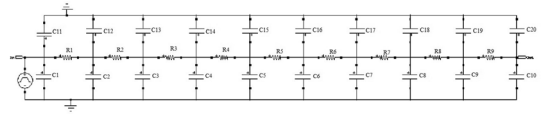
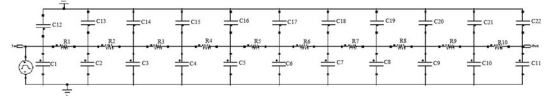
Length (mm)	Equation	Diagram	Power (W)	Delay (ps)
5	$\tau = \frac{RC}{8} = R_1(C_2 + C_8) + (R_1 + R_2)(C_3 + C_9) + (R_1 + R_2 + R_3)(C_4 + C_{10}) + (R_1 + R_2 + R_3 + R_4)(C_5 + C_{11}) + (R_1 + R_2 + R_3 + R_4 + R_5)(C_6 + C_{12}) = 63.05\,\text{ps}$		1.15×10^{-7}	65.91
6	$\tau = \frac{RC}{8} = R_1(C_2 + C_9) + (R_1 + R_2)(C_3 + C_{10}) + (R_1 + R_2 + R_3)(C_4 + C_{11}) + (R_1 + R_2 + R_3 + R_4)(C_5 + C_{12}) + (R_1 + R_2 + R_3 + R_4 + R_5)(C_6 + C_{13}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6)(C_7 + C_{14}) = 94.87\,\text{ps}$		1.15×10^{-7}	94.87
7	$\tau = \frac{RC}{8} = R_1(C_2 + C_{10}) + (R_1 + R_2)(C_3 + C_{11}) + (R_1 + R_2 + R_3)(C_4 + C_{12}) + (R_1 + R_2 + R_3 + R_4)(C_5 + C_{13}) + (R_1 + R_2 + R_3 + R_4 + R_5)(C_6 + C_{14}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6)(C_7 + C_{15}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7)(C_8 + C_{16}) = 121.90\,\text{ps}$		1.15×10^{-7}	129.15
8	$\tau = \frac{RC}{8} = R_1(C_2 + C_{11}) + (R_1 + R_2)(C_3 + C_{12}) + (R_1 + R_2 + R_3)(C_4 + C_{13}) + (R_1 + R_2 + R_3 + R_4)(C_5 + C_{14}) + (R_1 + R_2 + R_3 + R_4 + R_5)(C_6 + C_{15}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6)(C_7 + C_{16}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7)(C_8 + C_{17}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8)(C_9 + C_{18}) = 168.74\,\text{ps}$		1.15×10^{-7}	168.70
9	$\tau = \frac{RC}{8} = R_1(C_2 + C_{12}) + (R_1 + R_2)(C_3 + C_{13}) + (R_1 + R_2 + R_3)(C_4 + C_{14}) + (R_1 + R_2 + R_3 + R_4)(C_5 + C_{15}) + (R_1 + R_2 + R_3 + R_4 + R_5)(C_6 + C_{16}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6)(C_7 + C_{17}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7)(C_8 + C_{18}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8)(C_9 + C_{19}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8 + R_9)(C_{10} + C_{20}) = 203.02\,\text{ps}$		1.16×10^{-7}	213.55
10	$\tau = \frac{RC}{8} = R_1(C_2 + C_{13}) + (R_1 + R_2)(C_3 + C_{14}) + (R_1 + R_2 + R_3)(C_4 + C_{15}) + (R_1 + R_2 + R_3 + R_4)(C_5 + C_{16}) + (R_1 + R_2 + R_3 + R_4 + R_5)(C_6 + C_{17}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6)(C_7 + C_{18}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7)(C_8 + C_{19}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8)(C_9 + C_{20}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8 + R_9)(C_{10} + C_{21}) + (R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + R_7 + R_8 + R_9 + R_{10})(C_{11} + C_{22}) = 263.72\,\text{ps}$		1.17×10^{-7}	263.72

Table 10 Combined results of performance parameters for H-model

Length (mm)	Delay (ps)		Percentage improvement (%)
	Elmore estimation (Theoretical)	Simulated result	
1	2.62	2.82	7.6
2	10.53	10.75	2
3	23.71	23.68	0.8
4	41.22	42.14	2.2
5	63.05	65.91	4.5
6	94.87	94.87	0
7	121.90	129.15	5.9
8	168.74	168.70	0.02
9	203.02	213.55	5.1
10	263.72	263.72	0

form of delay calculation for RC ladder circuits. It is a type of RC model in which the total capacitance value remains the same though individual capacitance gets divided into half. The time constant produced by this model is RC/8 and can be used as another model for optimization purposes. Considering uniform distribution, different lengths along with each segment resistance and capacitance values used for estimation of performance parameters for the H-model are shown in Table 8.

The simulations were performed and the performance parameters for each length are tabulated in Table 9. The structures are modeled considering values calculated in Table 8 along with the Elmore delay estimation.

Further for H-model, the performance parameters are calculated theoretically using Elmore delay calculation which agrees with the simulated results. The collaborated results that are simulated and theoretical values of performance parameters are shown in Table 10.

Table 10 tabulates the delay percentage improvement. Percentage increase or decrease refers to the change in percent value to the extent to which a variable loses magnitude or value. The calculated values using Elmore delay estimation show the better computation of the interconnect circuits with less delay as compared to the calculated ones, though both the values are somewhat similar. Also, from the evaluated values, the performance parameters can be varied according to the lengths of interconnects. Figure 8 shows the variations of power to interconnect length and delay to interconnect length.

These two graphs also represent the linear relationship of power and delay with the increase in interconnect length. For the power consumption graph, the value first remains constant for 1 mm and 2 mm lengths then increase from 3 to 4 mm then further remains constant from 4 to 8 mm length, and lastly increases for 9 mm and 10 mm lengths. The power consumption increases steadily with the variation of lengths. For the delay graph, the value strictly increases with the increase in length. Also, the linear relationship represented in the graphs shows a positive slope. A strictly linear increase of delay verifies the monotonic nature of the impulse response again. For power consumption, the power becomes constant from 4 to 8 mm wire which means that the function becomes a constant and the slope becomes 0. Also, the interconnect circuits can be considered to be in series and it is known that the current in series remains constant. The power consumption will depend upon the voltage drop across each resistor. It can be concluded that for a particular range of length (4–8 mm), there is a constant voltage drop which makes the value of power consumption constant. Power consumption is directly proportional to the length of the interconnect. The longer the wire more will be the power consumption which can also be observed from Fig. 8. It is observed that the delay and power consumption varies with the increase in the length of interconnects. Also, an expression for new improved Elmore delay is evaluated and verified theoretically. Further, a comparison is done between both models.

3.3 Comparison

The comparison of power and delay for π-model and the proposed model are tabulated in Tables 11 and 12 respectively and it has been observed that the proposed model shows remarkable results in comparison to the existing one.

From Tables 11 and 12, it has been interpreted that the proposed model functions better as compared to the previous model. Also, the average percentage improvement of power is 75.167% and delay is 74.714% signifies that our proposed result shows remarkable values.

Lastly, a comparison of the proposed model is done with the other state of art techniques and is tabulated in Table 13.

The maximum length of the proposed H-model is considered for the comparison of delay and power values with other state of art techniques. For the proposed *H*-model the

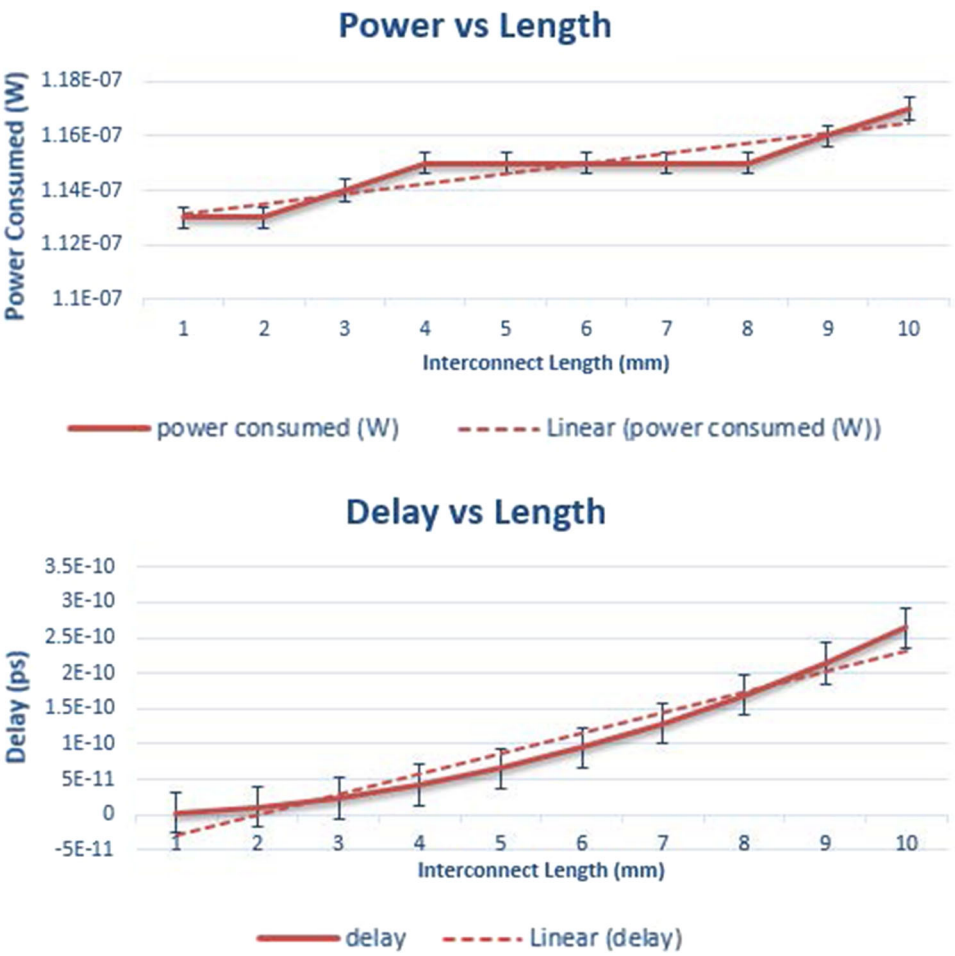


Fig. 8 Power and delay vs length graphs

input voltage is kept constant to 5 V with a rising time of 5 ns. When compared with the novel interconnect model as mentioned in [18] with second-order moments, more optimized values were observed from the Proposed H-model. Although, the authors in [18] have simulated their model on different voltages still our proposed model shows better results. Also with [18], when compared with RC lumped model, the proposed model shows 74.05% improvement in power and 98.69% improvement in terms of delay. When compared with distributed model 78.57% improvement is seen in terms of power and 99.38% improvement in terms of delay. In [19], authors have evaluated delay at 5 ns rising time for different nodes in the RC interconnect circuit. Though authors of the proposed model have not calculated at each node but for the end node, our model shows more speed in comparison to Gupta [19] with the same rising time, and 82.17% improvement has been observed. Also, the proposed model shows better efficiency and four times less power consumption of the interconnect circuits in comparison to the π-model.

4 Conclusion

In this paper, the authors have studied the existing RC models for long wires consisting of L, π, and T. Among all three of these πmodel reduces delay by 50% and does not have any extra node for modeling of the circuits. In this paper, an innovative Elmore delay estimation model was simulated which was compared to the π-model. Further, Elmore delay calculations for long wires with step response have been observed for uniform and non-uniform distribution segments for different lengths of interconnect. It was concluded that the circuit power was optimized when per unit length distribution of segments was done for different lengths of interconnects though there was not much difference in the delay values. An optimized Elmore delay calculation was performed to reduce the time constant of the interconnect circuits. Apart from delay, power consumption was also of major concern which was seen to be optimized while using an enhanced RC model. A linear relationship of power consumption and delay for both the

Table 11 Power comparison of both models

Length (mm)	π-model	Proposed model	Percentage improvement
1	4.52×10^{-7}	1.13×10^{-7}	75
2	4.58×10^{-7}	1.13×10^{-7}	75.32
3	4.60×10^{-7}	1.14×10^{-7}	75.21
4	4.63×10^{-7}	1.15×10^{-7}	75.16
5	4.68×10^{-7}	1.15×10^{-7}	75.42
6	4.72×10^{-7}	1.15×10^{-7}	75.63
7	4.73×10^{-7}	1.15×10^{-7}	75.68
8	4.71×10^{-7}	1.15×10^{-7}	75.58
9	4.63×10^{-7}	1.16×10^{-7}	74.94
10	4.51×10^{-7}	1.17×10^{-7}	73.73

Table 12 Delay comparison of both models

Length (mm)	π-model delay (ps/ns)	H-model delay (ps)	Percentage improvement
1	10.66 ps	2.82	73.54
2	42.10 ps	10.72	74.53
3	94.87 ps	23.68	75
4	168.71 ps	42.14	75
5	263.72 ps	65.91	75
6	379.45 ps	94.87	74.99
7	516.26 ps	129.15	74.98
8	672.90 ps	168.70	74.92
9	847.35 ps	213.55	74.79
10	1.03 ns	263.72	74.39

Table 13 Comparison of proposed model with other state of art technique

Models/Technique	Power (μW)	Delay
Propsoed H-model (for max L = 10 mm) (for 5 V and 5 ns rise time)	0.117	263.72 ps
Ramadass et al. [18] (for 5 V)		
RC Lumped	0.451	20.138 ns
RC Distributed	0.546	42.564 ns
Gupta [19] (for 5 ns rise time)		
At node A	–	0.018 ns
At node B	–	1.06 ns
At node C	–	1.48 ns

RC models was observed and it has been observed that the proposed model results in 75.167% improvement for power consumption and 74.714% improvement for the delay. Also, 71.25% improvement in delay has been observed with the existing research papers. Further, for future aspects, different materials can be used to evaluate the performance parameters for the circuits and a comparison can be done with copper material. Also, as the delay and power are estimated for global interconnects buffer insertion problems can be observed.

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