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# A Novel Reliability Assessment Scheme for Nano Resistive Random Access Memory (RRAM) Testing

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**Abstract**
To restore the traditional memories like Static RAM, Dynamic RAM and Flash memory in future computers, various semiconductor nano memories are introduced such as PCRAM, STTRAM, STTMRAM, Ferroelectric FET Memory and RRAM. Among them, RRAM is the most prominent candidate to fulfill future generation desires. Due to nanoscale miniaturizing it comes with a number of faults that directly affect the performance and reliability of the system. Previously there are many testing methods proposed for RRAM testing but there is no reliability assessment scheme specifically intended for testing algorithms. Hence an optimized march algorithm is formulated using self-verification write method and also a novel reliability assessment scheme is proposed in this article by means of queuing theory parameters. More particularly, the reliability curve is plotted for various testing methods (traditional testing method, row reading and optimized March algorithm – March 2n) which confer a clear idea about the probability of memristor cell waits in the test queue, idle time of the test server and test server utilization. Thus the proposed reliability assessment scheme paves a new dimension in quality and reliability assessment of nano RRAM testing.

**Keywords** RRAM · Self verification · Number of waiting memrister cell · Test server utilization · Reliability assessment · Quality of service

## 1 Introduction

The core memory for an entire computer is Random Access Memory. At present, flash memory technology is employed to transmit data between digital systems and computers which is efficient than DRAM and SRAM. Though it is an efficient replacement, it comes with very slow writing speed and constrained endurance. As a consequence, every electronic industry wants to find an alternative for flash technology [19], [20] to attain faster writing & reading capability, good scalability, maximized memory performance and higher endurance with compact cell size. Therefore memories with better data storing capacity were introduced such as PCRAM, STTRAM, STTMRAM, Ferroelectric FET Memory and RRAM. Amid RRAM is capable of replacing the conventional memory in future computers by incorporating nanotechnology core intrinsic properties which has most promising features like easy cell structure, express speed for program/erase (P/E), exceptional scalability, very less utility of operational power, fine compatibility with standard CMOS process [26], [27], [28], [29], 30], [31], [46] and high data retention i.e., ability to save its own data till the lifetime without any corruption in it [10], [22], [51]. Various device structures and storage materials (shown in Table 1) were proposed [12], [13], [13], [25], [33], [34], [36], [37], [38], [39] to build RRAM. Hence it is used in numerous trending applications like parallel computing (data storage and computation can be done in single device hence it reduces the data traffic) [9], neural network [21], [30], [49], [52] mixed-signal computing [24]. To avoid data shuttling problem in logic computation, all memristor cell in the crossbar array is assigned as input, output, assistance, and memory element at different stages [5], [6] which is used to transmit data between the processing unit and primary memory [47].

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**Table 1** Various material for RRAM and its outstanding properties

| Material | Properties | Application |
|---|---|---|
| $TiO_2$ | High stability, low cost, non- toxicity, realistic surface modification and non-corrosiveness | RRAM fabrication |
| NiO | Huge band gap (3.6 eV to 3.8 eV), an antiferromagnetic TMO semiconductor with exceptional electrochemical permanence, highly transparent and it lows down the material cost. | p-type semiconductor |
| ZnO | Cost-effective (due to the natural resource), high quantum efficiency, better bandgap (3.2–3.37 eV) and non-toxic effects | Wurtzite structured n-type semiconductor |
| $TaX_2$ | Less utility of operating voltage, fastest switching process, excellent thermal stability, unique retention ability, admirable homogeneity and extremely good endurance paves the way for reliable storage application. | 3D vertical RRAM |
| $HfO_2$ | Vertical switching capability and cost-effective | 3D Crossbar array |

## 2 General structure & operational conditions of RRAM

According to the array structure, RRAM is categorized into two types: (i) 1T1R RRAM (ii) Crossbar RRAM. In 1T1R structure, each cell consists of a keen MOSFET transistor which is used to avoid interrupts during RRAM operation. But, these transistors will make a rise in cell area that leads to further expenses. To defeat this hitch, Crossbar RRAM is proposed [1] which has a good density with accurate performance compared to 1T1R RRAM. Moreover, in crossbar RRAM structure, all cells are interconnected to each other and the memristor is directly attached between word-line and bit-line without any access transistor [15], [17] thus it occupies 4F2 area (F-feature size). In addition, several layers of the crossbar can be stacked by 3D integration technology that results in high density due to its nonlinear characteristics [7], [8], [11] that form an array structure [44]. While coming for operational conditions, an established connection between the top electrode (TE) and bottom electrode (BE) by means of the conductive filament (CF) is called as forming operation (shown in Fig. 1).

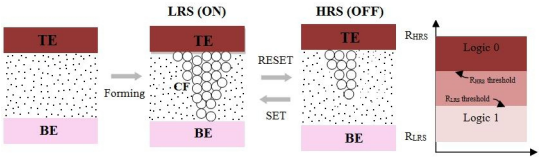



**Fig. 1** RRAM basic operations

In bipolar RRAM, the resistance of dielectric varies by applied voltage at when the functional voltage goes beyond the threshold voltage that will result in SET operation (transition from HRS - logic 0 to LRS - logic 1 / OFF state to ON state) which is responsible for a write operation. Similarly, detachment of CF between the (BE) & (TE) layer results in RESET operation (transition from LRS - logic 1 to HRS - logic 0 / ON state to OFF state). In 3D crossbar RRAM to avoid sneak current problem, RESET and read operation is performed concurrently along with entire row of cells, to read the data both (BE) & (TE) are applied with small amount of voltage difference for little span of time, the conducted current is sensed and measured by a sense-amplifier to find whether the cell's state is in low resistance (logic 1) or high-resistance (logic 0) which is known as read operation.

## 3 RRAM Testing Methods

RRAM inherits a lot of defects due to its non-deterministic character and nanoscale fabrication. Classification and definition of defects were proposed in [16]. Physics-based investigation of the memristor such as physical form and its fault models are studied in [18], [50] that symbolize all possible defects and extensive fault models. To find open defects and Undefined State Fault (USF) a Design-For-Test (DFT) approach is proposed in [23] and a fast march algorithm was proposed in [35] that speed-up the testing process (approximately 70%) with reduced energy consumption (approximately 40%). In the divide and conquer technique [4] all kinds of stuck-at faults are detected by measuring the summation of individual memristor current. New-fangled fault models such as Over-Forming (OF) fault and the Read-One-Disturb (R1D) faults are precise to RRAM which is described in [3], [14] and a customized testing approach is introduced based on the March algorithm [45]. Traditional March algorithms are used in most of the memory testing schemes shown in Table 2. Its write and read actions are done through unchangeable patterns which thoroughly check the memory with certain sort of faults in a series manner.

All test algorithms suffer by reading operation than the write operation since the read circuit requires several subcircuits to carry the intended operation which automatically increases the test complexity & time (shown in Fig. 2). So based on the number of operations, the efficiency of test algorithms is assessed by test complexity and test time [48] (shown in Fig. 3). Moreover, for every read operation certain amount of voltage/current (based on the reading scheme) is applied to the target cell, such external influence will affect the system functionality and lead to

**Table 2** Traditional March algorithms with testing sequence

| March algorithm | Marching Sequence |
|---|---|
| March 1/0 | {↕(w0);↑(r0,w1,r1); ↓(r1,w0,r0); ↕(w1);↑(r1,w0,r0); |
| MATS | ↓(r0,w1,r1);} |
| March A | {↕(w0);↕(r0,w1);↕(r1);} |
| March B | {↕(w0);↑(r0,w1,w0,w1); ↑(r1,w0,w1); |
| March C | ↓(r1,w0,w1,w0);↓(r0,w1,r0);} |
| MATS+ | {↕(w0);↑(r0,w1,r1,w0,r0,w1); ↑(r1,w0,w1); |
| March C- | ↓(r1,w0,w1,w0);↓(r0,w1,r0);} |
| MATS++ | {↕(w0);↑(r0,w1);↑(r1,w0);↕ (r0);↓(r0,w1);↓(r1,w0 |
| March AB | );↕(r0);} |
| March AB1 | {↕(w0);↑(r0,w1);↓(r1,w0);} |
| March MSL | {↕(w0);↑(r0,w1);↑(r1,w0);↓(r0,w1);↓(r1,w0);↕(r0);} |
| March-12n | {↕(w0);↑(r0,w1); ↓(r1,w0,r0);} |
| March AB2 | {↕(w1);↓(r1w0r0w0r0); |
| March C* | ↓(r0w1r1w1r1);↑(r1w0r0w0r0); ↑(r0w1r1w1r1); |
| | ↕(r1);} |
| | {↕(w0);↕(w1r1w1r1r1); ↕(w0r0w0r0r0);} |
| | {↕(w0);↑(r0,w1,w1,r1,r1,w0); ↑(r0,w0); ↑(r0);↑( |
| | r0,w1); ↑(r1,w0,w0,r0,r0,w1); ↑(r1,w1); |
| | ↑(r1);↓(r1,w0);} |
| | {↕(w0);↑(r0,w1,r1); ↑(r1,w0,r0); ↓(r0,w1); |
| | ↑(r1,w0);↕(r0);} |
| | {↕(w1);↕(w1r1w0r0w1r1);} |
| | {↑(r0,w1);↑(r1,r1,w0);↓(r0,w1);↓(r1,w0);↑(r0);} |

performance failure. Hence an optimized test method and reliability assessment scheme is required to enhance the testing process.

## 4 Optimized Test Algorithm

A self-verification write scheme is adopted in this paper consequently, the accuracy of every write operation is verified at the end of each write cycle by means of a write complete signal. It results in a combined "write & read" ("wr") operation, that will detect faulty write operation and avoid the read disturbance and corruption in memory elements. Here low power adaptive write circuit is used due to its attractive features such as fast operation, less power utility and higher accuracy of write operation than different write schemes like Fixed-Length Pulse (FLP) [40], Adaptive 1T1R [41], Adaptive Single Cell [42] and High Precision Tuning [43]. For example, the test complexity of the March 1/0 algorithm is 14n (shown in Fig. 4) and it is reduced to 10n by the self-checking method. Thus the write operation is verified devoid of a separate read circuit.

For March 1/0 algorithm self-check method is applied and test complexity is optimized, but it is ideal (i.e., no optimization in operational function) for MATS, MATS + and March C* algorithms (shown in Fig. 5.represented as a,b,c and a*,b*,c*). To rise above this consequence a novel march algorithm with 'wr' element is used without separate read operation by March WR test algorithm and the test complexity is also reduced (shown in Fig. 5.represented as a*,b*,c*) to 2n ({↕(wr0), ↕(wr1);}) which is very less compared to all other existing testing algorithms. Hence it is mentioned as March 2n. '.

Pseudo code for the algorithm.

for (i = 0; i←(n-1); i++).

{m(i) = 0;}

for (i = 0; i←(n-1); i++).

{if (m(i) = 0) (m(i) = 1);}

else {return WDF & RDF;}

Step 1: Initially write '0' operation is performed (w0) it is checked by inherited read '0' (r0) using write verification signal.

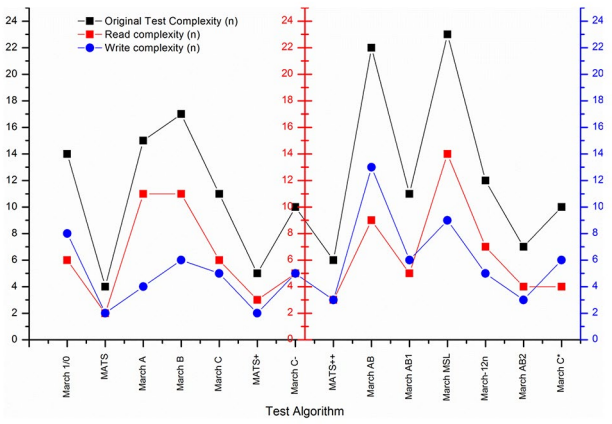



**Fig. 2** Effect of read and write operation to the original test complexity

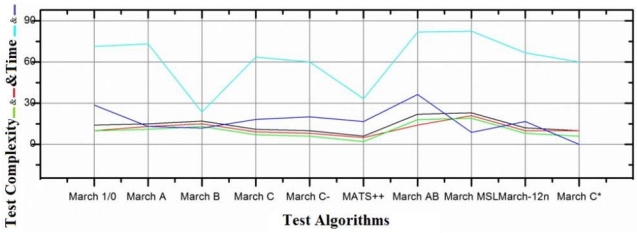



**Fig. 3** Test complexity and test time of various testing algorithms

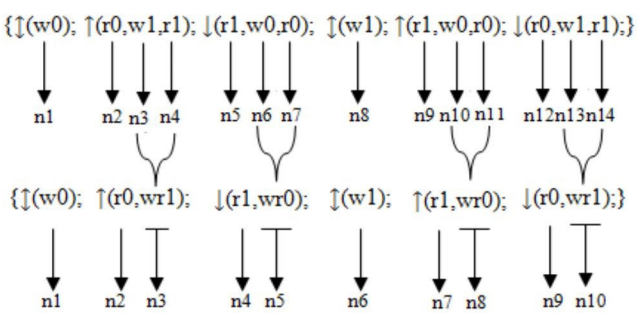



**Fig. 4** Application of self check method to March 1/0 algorithm

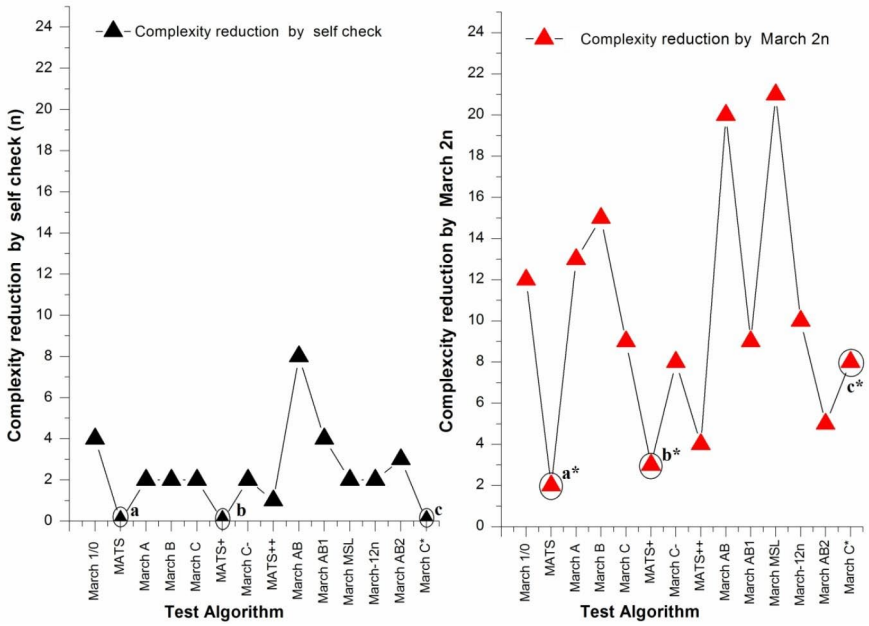



**Fig. 5** Complexity reductions by self check method and march 2n

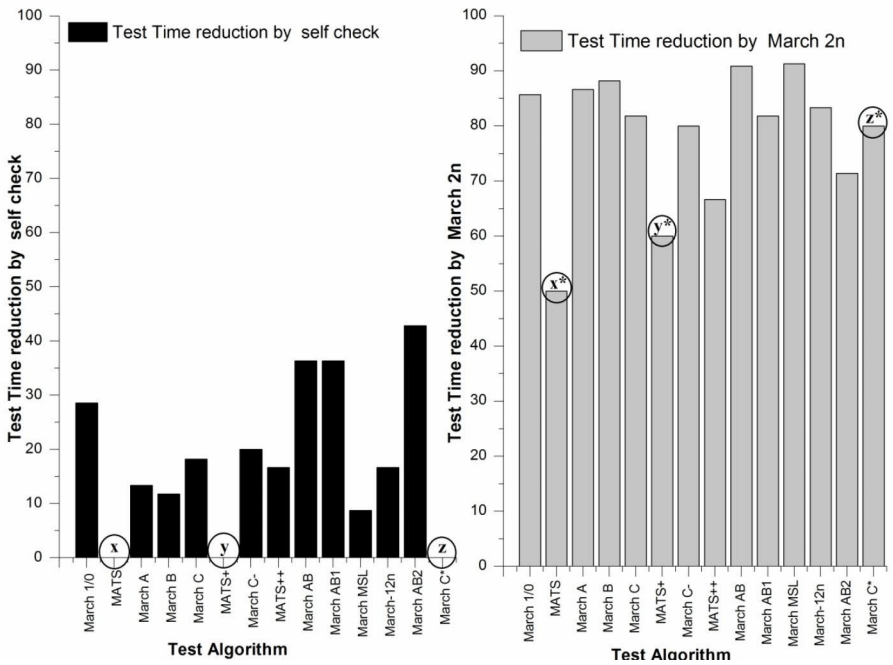



**Fig. 6** Test time reduction by self check method and March 2n

Step 2: Similarly write '1' operation is performed (w1) it is checked by inherited read '1' (r1) using write verification signal.

Self-check method reduces the test complexity for various existing test algorithms although there is no optimization for a few test algorithms such as MATS, MATS + and March C* algorithms (marked as a, b and c) shown in Fig. 5. Whereas in the March 2n test algorithm, there is noticeable test complexity optimization for the same algorithms (marked as a*, b* and c*). Similarly, the effect of test time reduction is shown in Fig. 6. There is no optimization in test time for the above-mentioned algorithms using self-check method (marked as x, y and z) while using March 2n it is well optimized (marked as x*, y* and z*).

## 5 Proposed Reliability Assessment Scheme for RRAM Testing

A range of testing algorithms was introduced to check the intended functionality of the memory device still, there is a research gap in reliability analysis. In most of the testing,

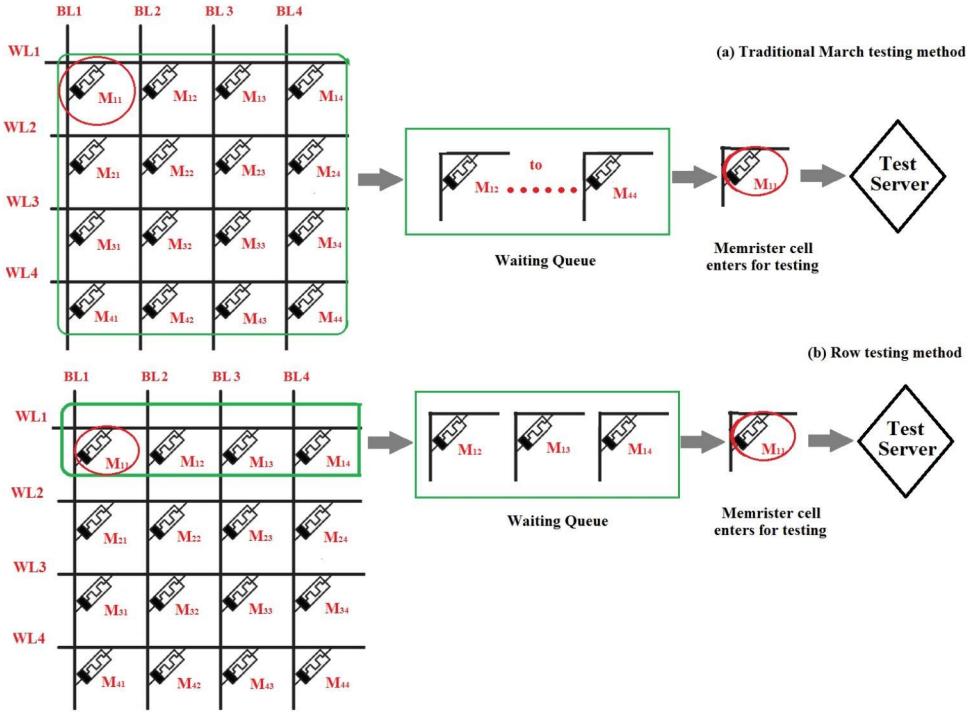



**Fig. 7** (a) Traditional march algorithm (b) Row reading method

efficiency is measured by the testing parameters like complexity of the test algorithm, test time, fault coverage, fault escape and false fault detection are made in the account. But it is equally important to check the reliability (quality of test over time) of the test server. Hence a novel reliability assessment scheme is proposed in this article using queuing theory. Here two parameters are considered (i) the number of cells under testing at a particular time (ii) the number of waiting for cells for testing. In the traditional march method, entire array is taken for the testing process and a single memristor cell, remaining memristor cell waits in test queue i.e., (n2 - (n2–1)) memristor cells are tested and (n2–1) cells waits in the test queue. For example, in 4*4 crossbar RRAM out of 16 memristor cells single memristor cell is tested (4*4 crossbar - shown in Fig. 7a, red circle) and the remaining 15 cells in the array waits for the testing process (shown in Fig. 7a - green box). This results in a higher probability of waiting cells in the test queue and the least server utilization. Whereas in row reading method [32] at a time single cell is tested in a particular row i.e., (n - (n − 1)) and (n – 1) cells waits in the test queue, thus for taken example single memristor cell in a row is tested (shown in Fig. 7b, red circle) and the remaining 3 cells wait for the testing process (shown in Fig. 7b, green box). But in the March 2n method at a time, single memristor cell is tested devoid of any waiting cells by auto write verification without separate read operation. Hence the number of waiting cells is completely avoided by this method.

## 6 Reliability Assessment Parameter & Reliability Curve

Queuing theory parameters (average waiting time, probability of a memristor cell waiting in the test queue, test server idle time, test server utilization) are calculated for various testing methods (shown in Table 3) and the reliability assessment curve is plotted for various RRAM (4*4 crossbar array) testing methods (shown in Fig. 8).

The reliability assessment curve (shown in Fig. 8) clearly shows that the March 2n test for crossbar RRAM is highly reliable than traditional and row reading testing methods. When the RRAM crossbar size increases, the number of waiting cells also increases (crossbar size 4*4 to 64*64 is shown in Fig. 9a) which has a direct impact on various parameters like service rate, service interruption and quality of service (shown in Fig. 9b).

To derive the quality of service, (i) service interruption which results in server breakdown (ii) server utilization is taken in account. A higher probability of service interruption directly affects the quality of service. As a consequence lower service interruption and high quality of service result in good reliability. In March 2n test method, test server is utilized to the fullest (shown in Fig. 8). Where the memristor cells are tested irrespective of the remaining cells in the crossbar array (i.e., no waiting cell) and so there is no service interruption. Thus it results in good quality of service (shown in fig 0.10).

**Table 3** Reliability assessment parameters for various testing methods

| Reliability assessment parameters | Traditional march method | Row testing method | Optimized March 2n |
|---|---|---|---|
| **Average waiting time (ns)**<br>Average waiting time of a particular memristor cell in the test queue (Wq).<br>Wq == $\lambda/\mu(\mu-\lambda)$Where $\lambda$ is the arrival rate (number of memristor cell that arrives for the testing process at a particular time) and $\mu$ is the service rate (number of memristor cell tested). | 6.6 | 3.3 | 0 |
| **Probability of a memristor cell waiting in the test queue (%)**<br>The probability of a memristor cell waiting in the test queue is the ratio between the numbers of waiting for cell to the total number of cells. | 93 | 18 | 0 |
| **Test server Idle time (ns)**<br>The Proportion of time the test server is idle in row testing method = 1- ρ,<br>where $\rho = \lambda/\mu$ | 0.9375 | 0.75 | 0 |
| **Test server utilization (%)**<br>Server utilization (ρ) is the ratio between the number of memristor cell that arrives for the testing process and the number of memristor cell tested i.e., $\rho = \lambda/\mu$ | 6.25 | 25 | 100 |

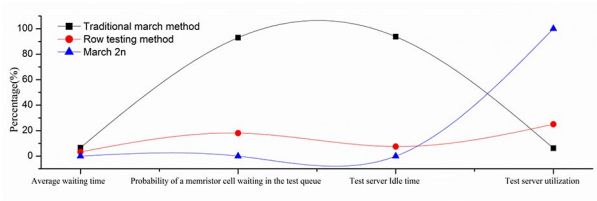



**Fig. 8** Reliability assessment curve by queuing theory

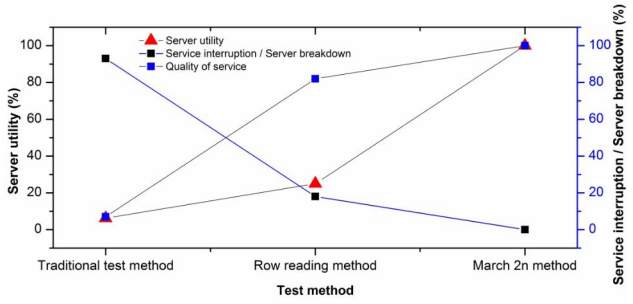
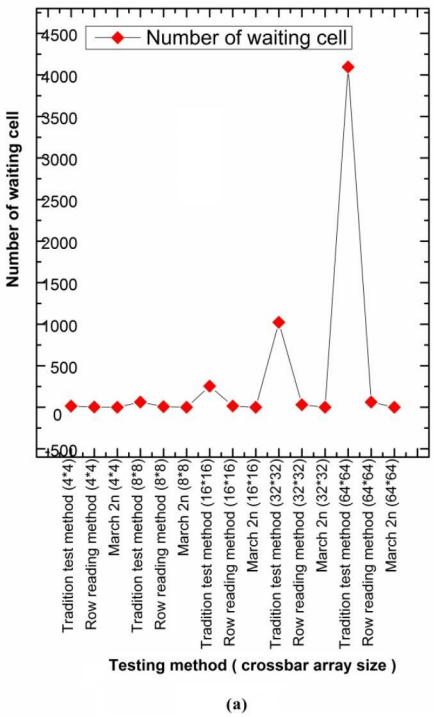
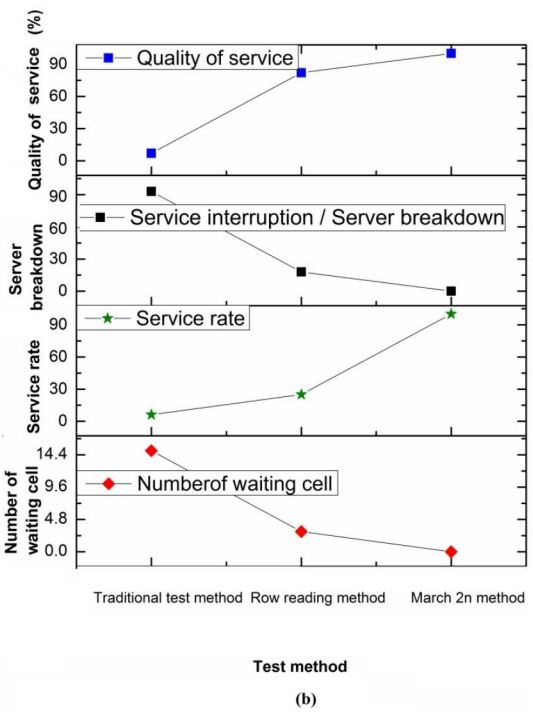



**Fig. 10** Quality of service for RRAM testing methods (with respect to server utility & server breakdown)

**Fig. 9** Relationship between number of waiting cell & test quality parameters



## Conclusion

This article addresses the reliability issues of memory testing algorithms. Here various memory testing algorithms are taken and the reliability is analyzed in a mathematical way using queuing theory parameters such as average waiting time, probability of a memristor cell waiting in the test queue, idle time of the test server and test server utilization. This is completely a new dimension in the memory testing field to analyze the nano memory testing algorithm with a reliability curve by the above parameters rather than conventional methods. In addition, the quality of service is assessed by server utility & server breakdown along with above mentioned queuing parameters. Hence the proposed novel reliability assessment scheme paves a new way to the nano memory testing field.

**Supplementary Information** The online version contains supplementary material available at https://doi.org/10.1007/s10470-022-02007-0.

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