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A picowatt, 3.88 ppm/°C, 0.011%/V subthreshold CMOS voltage reference biased by GSCC current source

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Abstract

This paper presents a picowatt-level power consumption CMOS voltage reference which is appropriate for low power applications. A gate-to-source connected cascode current source which is consisted of two transistors operating in the subthreshold region is used to generate bias current of proposed voltage reference, so resistors and MOSFETs operating in deep triode region are saved. The proposed circuit is implemented in the standard 0.18-um process. Simulation results of proposed voltage reference show that the minimum supply voltage is 0.45 V, consuming only 83pW at room temperature. The value of proposed voltage reference is 209.2 mV and temperature coefficient is 3.88 ppm/°C with a temperature range of −20–125 °C. PSR of proposed voltage reference is −65.54 dB at 100 Hz, and the LS is reduced to 0.011%/V by utilizing the cascode structure when the supply voltage changes from 0.45 to 1.8 V. In addition, the active area is only 0.0029 mm^2.

Keywords Low power · Low supply voltage · Subthreshold CMOS · Voltage reference · Low temperature coefficient

1 Introduction

Low-power and miniaturized integrated circuits (ICs) have gained continuous attention due to the high demand of next-generation power-aware applications such as biomedical devices [1], Internet of Things (IoT) [2] and energy harvesting systems [3]. The power supply of these applications whose energy source is micro-batteries or surrounding natural energy is not sufficient, and these applications must work for a long time. Therefore, the voltage reference circuit, as an indispensable component in any mixed-signal ICs, is required to generate a reference voltage while consuming low power. Simultaneously, the voltage reference is expected to remain robustness as the process, voltage and temperature are changed. In this research, a low-power, small-area, low-temperature coefficient (TC) and low-line sensitivity (LS) voltage reference is presented.

Conventional voltage references are generated by bandgap voltage references (BGRs). Bipolar transistors (BJTs) and resistors are essential of BGRs, and they dissipate much power and occupy large area. BGRs consist of two parts, one is complementary-to-absolute-temperature (CTAT) unit generated by the base-emitter junction voltage of the bipolar transistor, and the other is a proportional-to-absolute-temperature (PTAT) cell which is produced with the difference of two base-emitter junctions [4]. The reference voltage generated by BGRs varies very little with the variation of process. Some of them achieve very low temperature coefficients by temperature compensation, for example, second-order, high-order or curvature compensation [4–9]. Power Supply Rejection (PSR) could be reduced dramatically [10] with amplifiers. However, they hardly operate properly when the supply voltage is lower than 0.8 V because of the presence of BJTs. Thus, they are not superior in low power and low voltage applications. In order to generate reference voltages at low supply voltages, MOSFETs are required to operate in the subthreshold region. Their power consumption is much lower than conventional BGRs, so they have become a favorable alternative to conventional BGRs. Some nanowatt or picowatt reference voltages have been proposed [11–16] in

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Table 1 Size of transistors for core circuit of proposed voltage reference without start-up circuit

Transistor	Size(W/L) (um)	Transistor	Size(W/L) (um)
M1	5 x 10/5	M2	6 x 10
M3/M4	5/10	M5	10/10
M6	8.78/10	M7	5/10
M8	5/10	M9	2 x 5/10
M10/M11	8/10	M12/M13	¼

recent years. In [11], Zhan et al. presented a voltage and a current reference which have an amplifier and two types of resistors. Though the MOSFETs are all operated in the subthreshold region, resistors in [11] occupy large area and dissipate a lot of power compared to the core circuit of the voltage reference. The bias current in [14] is generated by the bulk-driven current generator. The threshold voltage of an NMOS is reduced by raising its substrate voltage. And there is a designed voltage to make it operate in deep triode region. Similarly, there are transistors operating in deep triode region to act as resistors in [15, 16]. Hence, a specific gate voltage is required which needs an extra block to generate. In [17], there are two voltage references and a self-biased current generator for both voltage references. The difference of two voltage references in [17] is active load. One is compensated by the threshold voltage difference of different transistors and thermal voltage (V_T), and the other is a diode implemented through a transistor which is a CTAT unit and compensated by the voltage difference of the gate-to-source with a positive temperature coefficient. The power of voltage references implemented in [12, 13] are picowatt-level. None of them requires an additional gate voltage. The bias current is generated by self-biased in [12, 13]. Although the power of these works is low, other performances such as TC and PSR are not as attractive as power.

In this work, a picowatt CMOS subthreshold voltage reference is proposed. A new biasing which is formed with two transistors is proposed. One is gate-to-source connected (GSC) NMOS, and the other is a cascode transistor. Firstly, the gate and source of GSC NMOS are connected to flow a picoampere level bias current and resistor is replaced by GSC NMOS to reduce area of layout. Meanwhile, the gate and source of GSC NMOS are connected to GND, which is the same as the substrate. Hence, there is no need to consider the back-gate effect of GSC NMOS unlike [18] and the bias current generated in this way is more robustness. Secondly, a cascode transistor is added to increase the resistance of the bias current source and shield the variation from the supply voltage to make it more ideal. The drain-induced-barrier-lowering (DIBL) effect of GSC NMOS is also eliminated by this method. Moreover, the gate of the cascode NMOS is connected to voltage reference, the smaller variation with PVT is more beneficial for the robustness of the bias current and reference voltage than in [12] where the gate is connected at other notes in [12] though they are both self-biased. Hence, all MOSFETs operate in the subthreshold region. The specific gate voltage for MOSFETs which is operating in deep triode region is also eliminated by this method. This method decreases LS and low-frequency PSR without increasing minimum supply voltage in contrast to [12, 18]. As the results show, the voltage reference circuit proposed in this paper has a distinct reduction in power and area. Compared with subthreshold voltage references proposed in recent years, though the temperature range (−20–125 °C) is smaller than −40–125 °C which is because carrier mobility reduced too much in lower temperature, the power, area, and TC of the proposed voltage reference are more competitive.

The rest of this paper is organized as follows. Section 2 presents the circuit and operation principle of the voltage reference proposed in this paper; Sect. 3 details the primary design considerations of the circuit and presents the size of transistors; Sect. 4 shows the simulation results of the circuit and gives the comparison of obtained results with other voltage references reported recently. Finally, the paper is concluded in Sect. 5.

2 Proposed design and operation principle

2.1 MOSFET subthreshold current model

The transistors in the voltage reference circuit proposed in this paper all operate in the subthreshold region, as a result, an appropriate MOSFET current model must be required. It is obtained from the MOSFET subthreshold current model (MSCM) [19] that the drain current of a MOSFET is composed of a forward (I_F) and a reverse current (I_R), which is as the following equations:

$$I_D = I_F - I_R = I_S\left(i_f - i_r\right) \quad (1)$$

$$I_S = SI_{SQ} \quad (2)$$

where i_f and i_r are the forward and reverse inversion coefficients, and S is called the aspect ratio W/L of transistors. W and L are the width and length of channels, respectively. I_{SQ} is the process-related sheet normalization current that is described as:

$$I_{SQ} = \frac{1}{2}\mu\eta C_{ox}V_T^2 \quad (3)$$

where μ is the carrier mobility, $\eta = 1 + C_d/C_{OX}$ is the

subthreshold slope factor where C_d is the depletion capacitance and C_{ox} is the gate capacitance per unit area that is dependent on the gate oxide thickness. C_d, which is a part of the subthreshold slope factor, is temperature-dependent. But compared with the threshold voltage of the transistor, the effect of temperature changes on it could be negligible. $V_T = k_BT/q$ is thermal voltage which relies on Boltzmann's constant (k_B = 1.38 × 10^-23 J/K), electron charge (q = 1.6 × 10^-19C) and the absolute temperature (T). The thermal voltage is approximately 26 mV at room temperature (T = 300 K). The correlation between normalized current ($i_{f(r)}$) and voltage is as the following equation:

$$\frac{V_G - V_{TH} - \eta V_{S(D)}}{\eta V_T} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \quad (4)$$

where V_G, V_S and V_D are gate, source and drain voltages of the MOSFET with respect to the voltage of the substrate respectively. V_{TH} is the threshold voltage.

From Eq. (1) and Eq. (4), when an NMOS is operated in the weak inverse region ($i_f < < 1$), the drain current (I_D) can be expressed by the following:

$$I_D = 2eI_S \exp\left(\frac{V_G - V_{TH}}{\eta V_T}\right)\left[\exp\left(\frac{-V_S}{V_T}\right) - \exp\left(\frac{-V_D}{V_T}\right)\right] \quad (5)$$

in which, e is the Euler number ($e \approx 2.7178$), a constant in mathematics and I_D is almost independent of the drain voltage (V_D) when V_D is much larger than V_T (i.e. $V_D \geq 4V_T$).

2.2 Circuit description

The complete circuit of proposed voltage reference in this paper is shown in Fig. 1, consisting of four parts: start-up circuit, CGCS bias circuit, an amplifier and the active load.

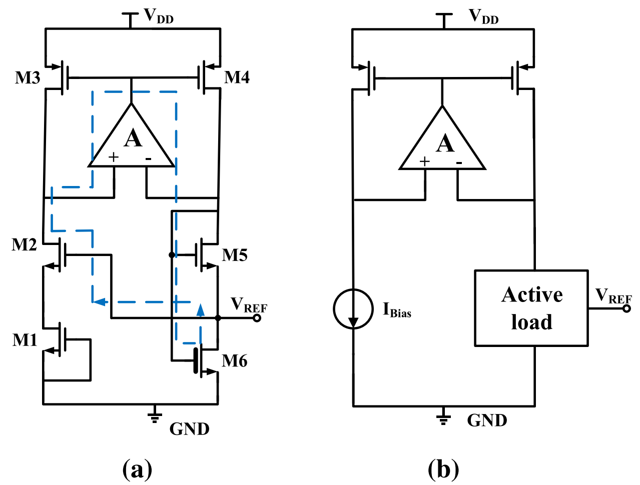

Fig. 2 Schematic of the proposed voltage reference: **a** Core circuit **b** Simplified structure

Transistors M1-M5 and devices in the amplifier are standard PMOS and NMOS devices (1.8 V), and M6 is a high threshold-voltage transistor (3.3 V).

The core circuit of proposed picowatt-voltage reference is shown in Fig. 2(a). And it can be simplified to the structure shown in Fig. 2(b). M1 and M2 in Fig. 1 are the gate-to-source connected cascode (GSCC) current source to generate bias current. The active load is composed of M5 and M6.

Voltage reference proposed in this paper is generated by the branches composed of M5 and M6 that operate in the subthreshold region, and the current flowing through M5 and M6 is equal which is generated by GSCC current source. Reference voltage is generated by two branches rather than three branches in [12], one is bias current and the other is active load. There is a similar bias current proposed in [18], but DIBL effect on threshold voltage of cut-off transistor is out of consideration in [18]. Hence, its LS and PSR are poor. In proposed voltage reference, M2 in

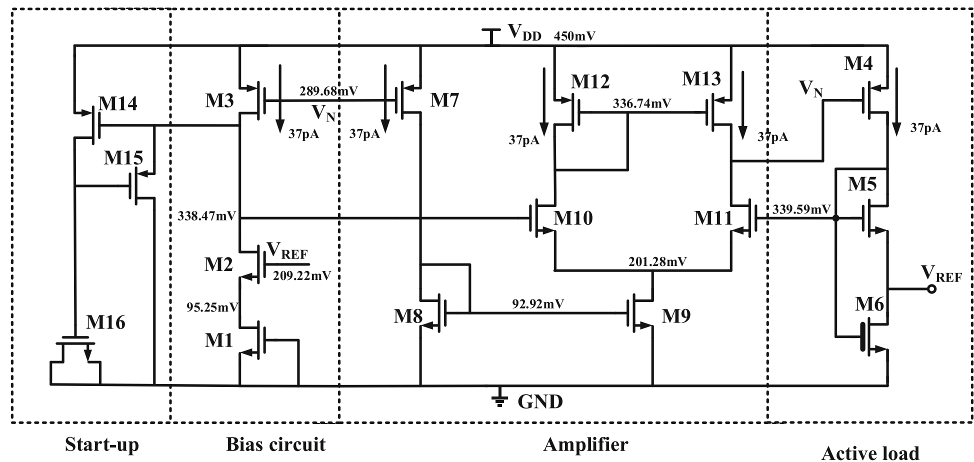

Fig. 1 The complete circuit of the proposed voltage reference

Fig. 2(a) is designed to increase resistance of the bias current and shield the variation from the supply voltage. In the meantime, there is an amplifier in proposed design. Though there are some additional power due to amplifier, the operation principle of the voltage reference is not affected by the amplifier, meanwhile, the value of voltage reference and temperature coefficient (TC) are not influenced by the amplifier. Then, because of the introduction of the amplifier, a negative feedback loop (as shown in Fig. 2(a)) is introduced in the circuit to make the circuit more robustness. Therefore, the LS and PSR of the voltage reference have been effectively improved.

2.3 Proposed voltage reference

The equivalent resistance of M1 is large (GΩ), as shown in Fig. 3, so the drain voltage is much larger than V_T. Hence, the biased current generated by GSC-NMOS is:

$$I_{D1} = 2eS_1 I_{SQ} \exp\left(\frac{-V_{TH1}}{\eta_1 V_T}\right) \tag{6}$$

Since M5 and M6 operate in the weak inverse region, and their drain voltages are larger than $4V_T$, the following two equations can be obtained:

$$I_{D5} = 2eS_5 I_{SQ} \exp\left(\frac{V_{G5} - V_{TH5} - \eta_5 V_{REF}}{\eta_5 V_T}\right) \tag{7}$$

$$I_{D6} = 2eS_6 I_{SQ} \exp\left(\frac{V_{G6} - V_{TH6}}{\eta_6 V_T}\right) \tag{8}$$

For the reason that $I_{D5} = I_{D6} = I_{D1}$ and $V_{G5} = V_{G6}$, the voltage reference (V_{REF}) in Fig. 1 can be expressed as:

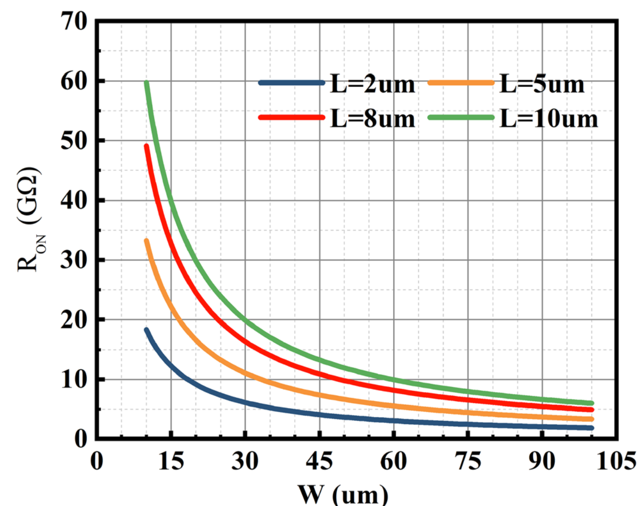

Fig. 3 The equivalent resistance of M1 with different L at V_{DS} = 250 mV

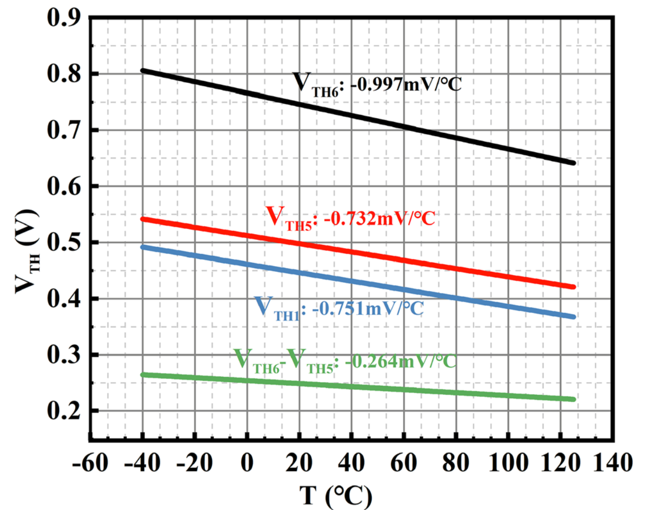

Fig. 4 Simulation results: V_{TH} of M1, M5 and M6 with temperature

$$V_{REF} = \frac{V_{TH6} - V_{TH5}}{\eta_5} + \frac{\eta_5 - \eta_6}{\eta_1 \eta_5} V_{TH1} + \frac{\eta_6}{\eta_5} V_T \ln\left(\frac{S_1 I_{SQ1}}{S_6 I_{SQ6}}\right) - V_T \ln\left(\frac{S_1 I_{SQ1}}{S_5 I_{SQ5}}\right) \tag{9}$$

Threshold voltage of MOSFETs can be approximated by an equation that has a linear negative dependence on temperature and it is expressed as [20]:

$$V_{TH}(T) = V_{TH}(T_0) + k(T - T_0) \tag{10}$$

where $V_{TH}(T_0)$ is threshold voltage at room temperature and k, which is negative, is the first-order temperature coefficient of threshold voltage. The temperature dependencies of M1, M5 and M6 are shown in Fig. 4. It can be seen that the absolute value of the slope of M5 is smaller than that of M6 so the gap of the threshold voltages is still a

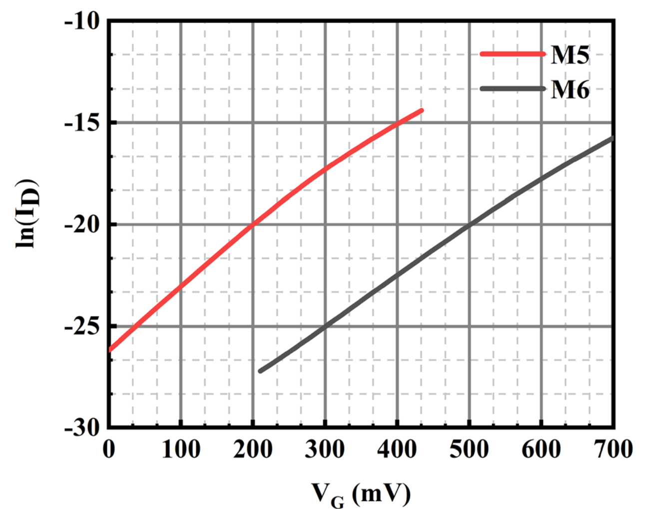

Fig. 5 V_G vs. ln (I_D) at V_S = 0 mV

CTAT voltage, but the absolute value of the slope decreases obviously.

Since η_5 and η_6 depend on the device and vary little with temperature changes. Moreover, it is known from Eq. (5) that when transistors operate in the subthreshold region, making V_S is 0 V and V_D is much larger than the thermal voltage, V_G and ln (I_D) are linearly related with a slope of $1/\eta V_T$, and the result is obtained by simulation as shown in Fig. 5, the slopes are similar, so η_5 and η_6 can be regarded as equal at room temperature. Hence, Eq. (9) approximated as:

$$V_{REF} = \frac{V_{TH6} - V_{TH5}}{\eta_5} + V_T \ln\left(\frac{S_5}{S_6}\right) \tag{11}$$

It can be seen that the source of M5 is not connected to GND, so reference voltage is affected by the back-gate effect of M5, the relationship between threshold voltage of the transistor and the substrate voltage can be approximated as [21]:

$$V_{TH}(T) = V_{TH0} + \alpha V_{SB} \tag{12}$$

in which α is positive and V_{TH0} is threshold voltage when there is no back-gate effect. From Eq. (10) to (12), the temperature coefficient (TC) of the reference voltage can be obtained as:

$$V_{REF} = \frac{V_{TH6} - V_{TH5}}{\eta_5 + \alpha} + \frac{\eta_5}{\eta_5 + \alpha} V_T \ln\left(\frac{S_5}{S_6}\right) \tag{13}$$

Setting $\frac{\partial V_{REF}}{\partial T} = 0$, the optimal ratio of S5 and S6 can be expressed as:

$$\left(\frac{S_5}{S_6}\right)_{OPT} = \frac{\eta_5}{\eta_5 + \alpha}\left[\frac{k_6 - k_5}{\eta_5} + \frac{k_B}{q}\ln\left(\frac{S_5}{S_6}\right)\right] \tag{14}$$

However, the back-gate effect of M5 has little effect on the voltage reference proposed in this paper, for example, the point when temperature coefficient is zero remains unchanged. It is deserving to pay attention that for Eq. (14), $\mu_1 = \mu_5 = \mu_6$ is assumed, so that the temperature characteristics of I_{SQ} are neglected during the analytical process.

3 Design considerations

The performances of voltage references are not only temperature coefficient (TC) and power, but also LS, PSR and so on. In order to get superior performances, these aspects and some trade-offs need to be considered in the design of the circuit.

3.1 Verification of MOSFET subthreshold current model (MSCM) of M1

A precise voltage reference is requested for a lot of next-generation power-aware applications, so it is crucial to use the proper model during the design of the circuit. All transistors proposed in this paper operate in the subthreshold region, so MOSFET subthreshold current model (MSCM) is employed. However, the case where the gate and source are connected to GND, which means that the gate and source are zero voltage with respect to the substrate voltage (V_G = V_S = 0 in Eq. (5)), was not taken into consideration of MSCM proposed in [19]. It is required to be verified whether M1 is suitable for MSCM, hence a set of simulation results, which is the curve of the drain current (I_D) of M1 versus V_D when V_G = V_S = 0 at T = 27 °C, is presented in Fig. 6. Simultaneously, V_G = V_S = 0 is substituted into Eq. (5), and the other parameters in Eq. (5) such as threshold voltage are accessed from the standard 0.18-um process. The drain current vs. V_D is plotted by MATLAB.

The graph plotted by MATLAB is compared with the simulation result and it can be seen that the error is minor. Because the drain voltage of M1 increases directly during the simulation, a continuous change in threshold voltage of M1 caused by the DIBL effect. However, the threshold voltage variation is not taken into consideration in the plotted curve by MATLAB. The maximum error is 4% and is reduced to 1.3% with the cascode transistor (M2) which is illustrated in Part 3.2 of Sect. 3, so that the error is able to ignore. Therefore, the drain current equation in the MSCM, i.e., Eq. (5), remains applicable when the gate and source of the transistor are connected to GND.

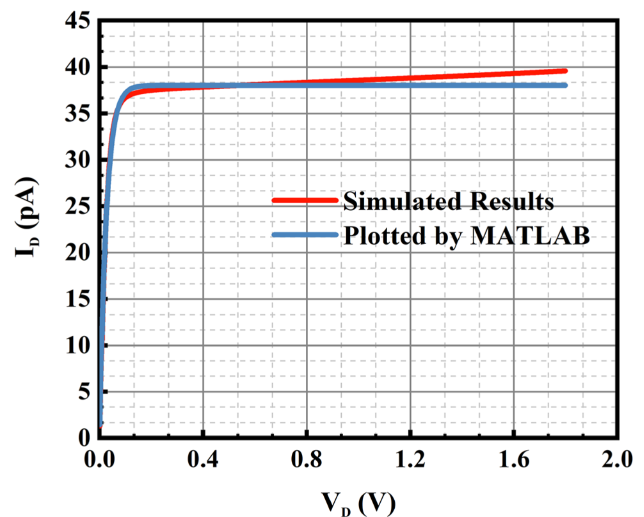

Fig. 6 the drain current of M1 vs. V_D at T = 27°C

3.2 Supply voltage sensitivity

The dependence of voltage references on supply voltage is expressed by the line sensitivity (LS). The LS is given by:

$$\mathrm{LS} = \frac{\Delta V_{REF}}{\Delta V_{DD} \times V_{REFm}} \times 100\% \quad (15)$$

where ΔV_{DD} means the range of V_{DD} and ΔV_{REF} means the variation value of the voltage reference, which is equal to $V_{REF,max}$–$V_{REF,min}$. V_{REFm} is the average value of V_{REF} within ΔV_{DD}. ΔV_{REF} plays a determinative role in Eq. (15), and it is obtained from Eq. (9) that the parameter affected by the change in V_{DD} is mainly the threshold voltage of the transistor because of DIBL effect. Temperature coefficient is put firstly in the derivation of Eqs. (9–14). As the supply voltage varies, the vary of V_{th1} plays the most significant role for the LS results, but it is not a decisive factor in the derivation of the temperature coefficient, so V_{th1} is neglected in the derivation because the coefficient is small with other factors.

The influence of the DIBL effect on threshold voltage can be expressed as [22]:

$$V_{TH} = V_{TH0} - \lambda V_{\mathrm{DS}} \quad (16)$$

in which V_{TH0} represents the threshold voltage when the drain-to-source voltage is zero and λ is the DIBL effect factor, which is same when the length of transistors is equal [13]. Hence, the length of M5 and M6 is equal. Accordingly, V_{TH1} is the most responsible factor for the LS results. Utilizing the shielding feature of cascode, the addition of M2 shields the influence of variation of V_{DD} on threshold voltage of M1, and the trend of V_{TH} variation is significantly weakened when the circuit reaches stability, as shown in Fig. 7. As a result, LS and low-frequency PSR are decreased by this method.

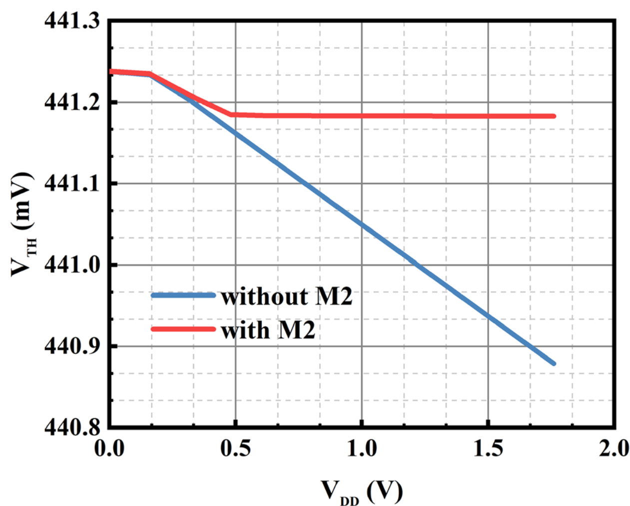

Fig. 7 V_{TH} of M1 versus V_{DD}

MOSFETs are generally immune to the channel length modulation effect when they operate in the subthreshold region, but DIBL effect makes the threshold voltage shift. To reduce the impact of DIBL effect on this design, the high-impedance transistors proposed in this paper are designed with large L.

3.3 Minimum supply voltage

The minimum value of the supply voltage must be determined to ensure that all transistors of the circuit are operated in the correct region. The saturation condition in the subthreshold region is satisfied when the drain-to-source voltage of the transistor is greater than 4 times thermal voltage. Therefore, from Fig. 1, the theoretical minimum supply voltage is expressed as:

$$\begin{aligned} V_{DDMIN} &= \max\{V_{DS1} + V_{DS2} + V_{DS3}, V_{REF} + V_{DS5} + V_{DS4}\} \\ &= \max\{12V_T, V_{REF} + 8V_T\} = V_{REF} + 8V_T \end{aligned} \quad (17)$$

The value of V_{REF} is designed to exceed 200 mV that is able to calculated by Eq. (13), so V_{DDMIN} depends on the value of V_{REF} because the value of V_T is 26 mV. And it can be seen from Eq. (13) that V_{REF} is determined by threshold voltage and the aspect ratio of M5 and M6. Thus, the closer V_{TH} of M5 and M6 is expected to reduce V_{DDMIN}. The simulation results show that V_{REF} is stable when the supply voltage is larger than 0.4 V, which is consistent with the analysis results obtained from Eq. (17).

3.4 Process Variations

From Eq. (13), the value of voltage reference proposed in this paper is related to the subthreshold slope factor (η) and the threshold voltage (V_{TH}) of transistors. Therefore, careful layout and large size devices are applied in order to reduce the effect of process variations on the reference voltage value. Figure 8 shows the Monte Carlo simulation results of the reference voltages and TCs obtained under the assumption that the mismatch and error of the process model used satisfy a Gaussian distribution. The average value of the reference voltage obtained at the end of 1000 simulations is 209.3 mV with a standard deviation of 0.45 mV. The Monte Carlo simulation of TC is illustrated in Fig. 8(b), where the mean value is 4.53 ppm/°C of 1000 simulations, the standard deviation is 0.9 ppm/°C, and the maximum value is 8.49 ppm/°C. The results obtained by Monte Carlo simulation and simulation of different process corners show that the PVT characteristics of the voltage reference proposed in this paper are quite good.

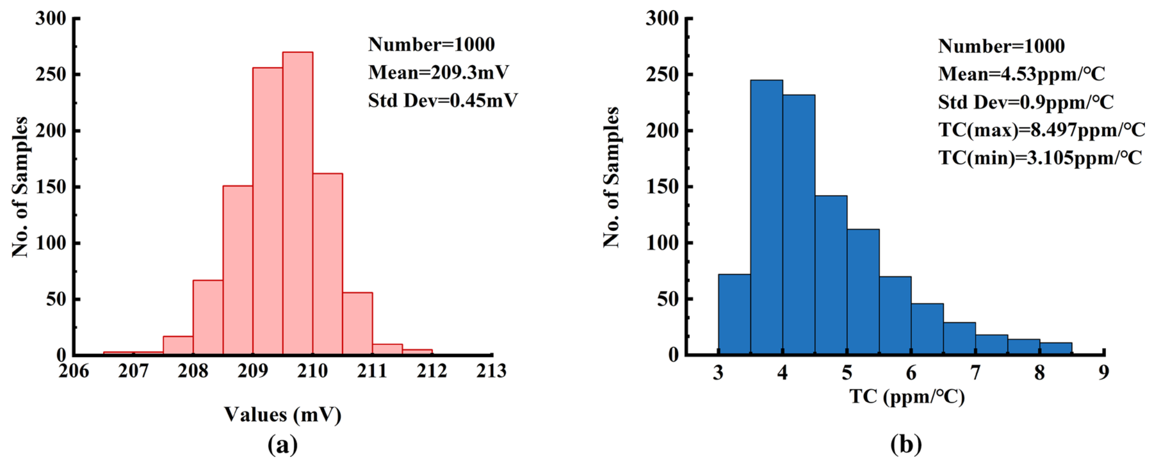

Fig.8 Monte Carlo simulation: **a** Voltage reference **b** Temperature coefficient

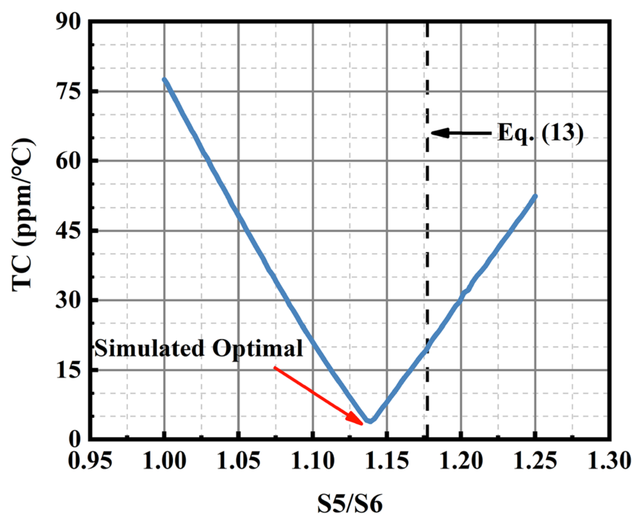

Fig. 9 Simulated aspect ratio of transistors for optimal TC

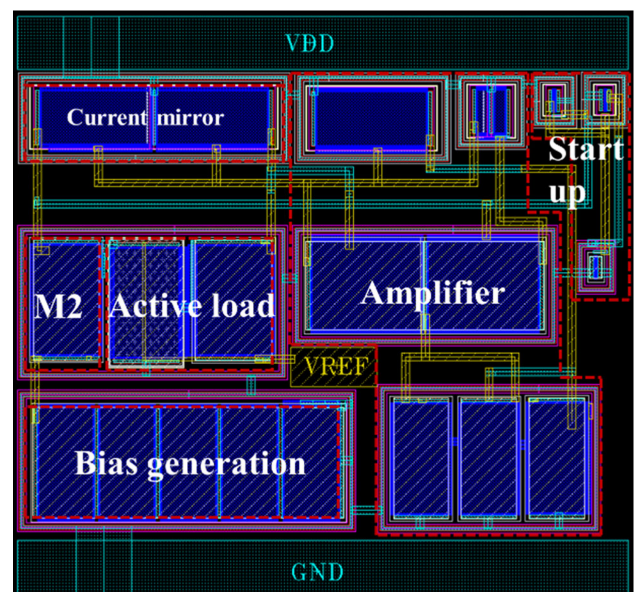

Fig. 10 Layout of the proposed voltage reference

3.5 Optimal aspect ratio for temperature coefficient

The aspect ratio of M5 and M6 at zero temperature coefficient is calculated from Eq. (14) to be about 1.18. Figure 9 shows the temperature coefficient of proposed voltage reference versus S5/S6. The simulation is obtained by holding the size of the transistors except M6 and altering width of M6. As a result of the simulation, it is observed that the temperature coefficient is smallest when S5/S6 is 1.14 approximately.

Taking the above design considerations into account, the size of transistors in the voltage reference circuit proposed in this paper is shown in Table 1.

4 Simulation results

The proposed voltage reference based on GSCC current source is implemented in a standard 0.18-um CMOS process. To analyze the performance parameters of the circuit, post simulations including Monte Carlo are achieved on the Cadence Virtuoso platform. The layout of the reference circuit is shown in Fig. 10 with the active area of 2943 (55.19 um * 52.33 um) um^2.

The variation tendency of proposed reference voltage with temperature when the supply voltage is 0.45 V is shown in Fig. 11, where the temperature range is −20–125 °C. From Fig. 11(a), it is obtained that the temperature coefficient (TC) is 3.88 ppm/°C. In this paper, TCs of five different process corners are simulated as shown in Fig. 11(b), and the corresponding temperature

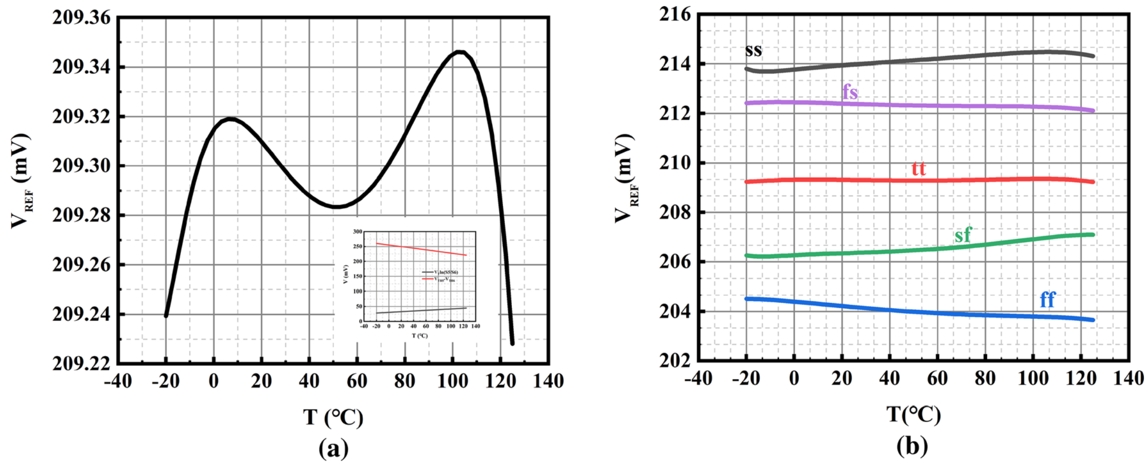

Fig. 11 Voltage reference as a function of temperature when V_{DD} = 0.45 V

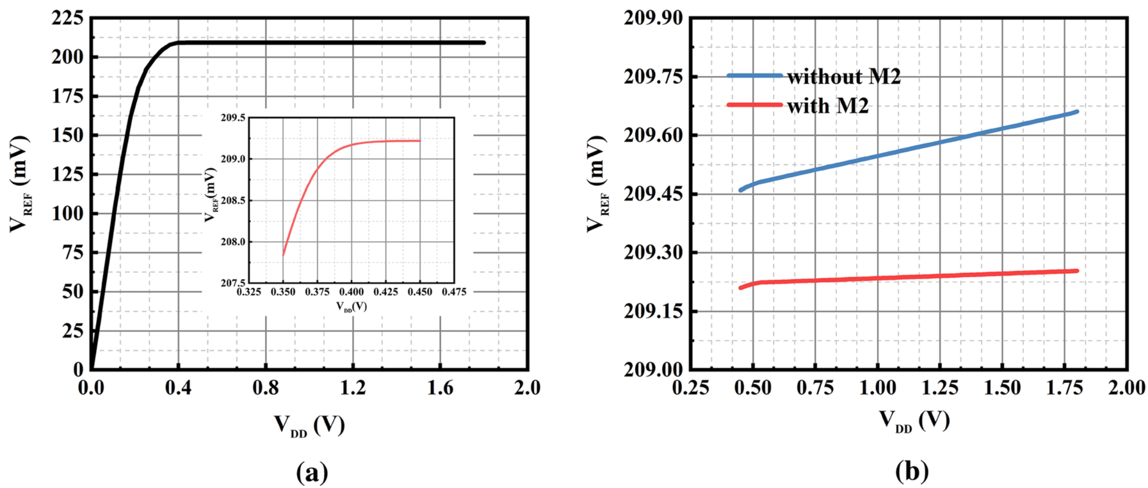

Fig. 12 Voltage reference variation with supply voltage at 27°C: **a** 0–1.8 V **b** 0.45–1.8 V

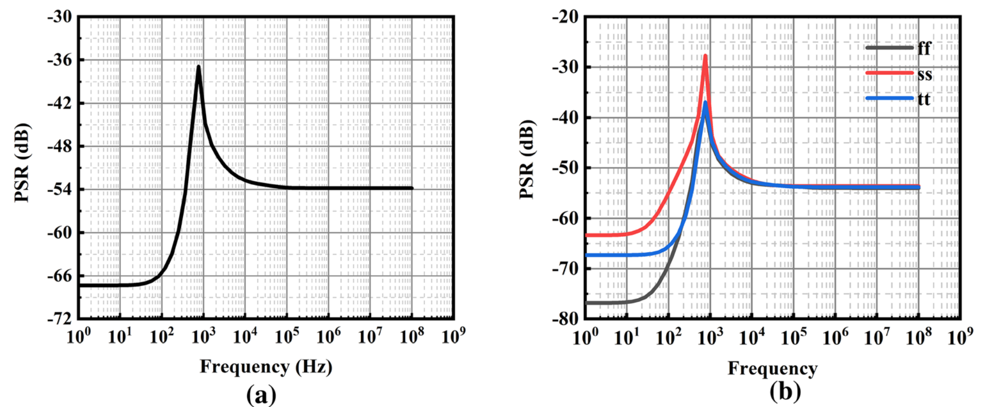

Fig. 13 PSR simulation results at 27 °C when supply voltage is 0.45 V

coefficients are 25.09, 25.61, 11.14 and 29.04 ppm/°C for ss, sf, fs and ff, respectively. Therefore, when considering the influence of PVT, the proposed circuit can still provide a voltage reference with low temperature coefficient.

The variation curve of the voltage reference with supply voltage at room temperature (27 °C) is shown in Fig. 12. It can be seen from Fig. 12(a), that the voltage reference reaches stability when the supply voltage exceeds 0.4 V, which is consistent with the description in Part 3.3 of

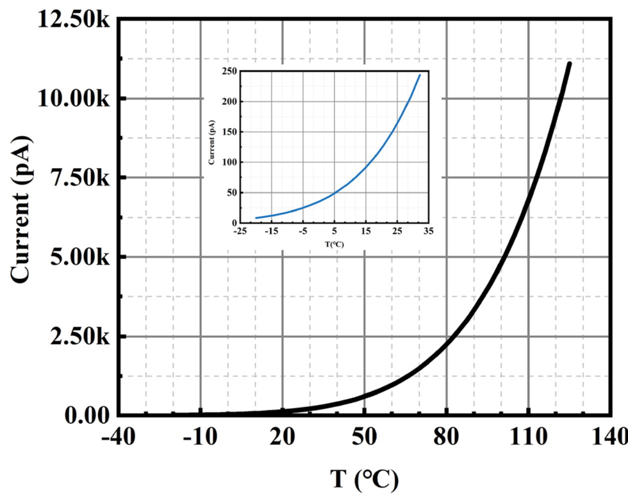

Fig. 14 Current consumption variation with temperature at 0.45 V

Sect. 3. Meanwhile, Fig. 12(b) shows that when the supply voltage changes from 0.45 to 1.8 V in the case of no cascode transistor (M2), the reference voltage increases by 0.21 mV with the LS of 0.078%/V. In comparison, with the addition of M2, the reference voltage increases by 0.05 mV, and LS is reduced to 0.011%/V.

The PSR of the voltage reference demonstrates the extent to which it is affected by the supply voltage ripple. As analyzed, Fig. 13(a) displays the PSRs when the supply voltage is 0.45 V at 10 Hz and 100 Hz are −67.34 dB and −65.54 dB, respectively. The PSRs at different process corners is also simulated. They are −53.29 and −67.56 dB at 100 Hz, as shown in Fig. 13(b), when process corners are ss and ff.

The current consumption variation versus temperature when supply voltage is 0.45 V obtained from the simulation is given in Fig. 14. It can be seen that the current consumption at room temperature (27 °C) is 185 pA approximately when the supply voltage is 0.45 V. Hence, power of proposed voltage reference is 83 pW.

For the reason that the performance of voltage references is quantified by many parameters, a Figure of Merit (FoM) is provided to present the overall performance of a proposed circuit. A FoM which takes temperature range, TC, power and active area of voltage references into account is defined as [12]:

$$FoM = \frac{(T_{MAX} - T_{MIN})^2}{TC \times Power \times Area} \quad (18)$$

Table 2 summarizes the performance of the GSCC-biased voltage reference proposed in this paper compared with other low-power subthreshold CMOS voltage references. The lower power consumption and smaller temperature coefficient of the proposed circuit in this paper are concluded, while the circuit utilizes no resistors or operational amplifiers which occupy large active area, so FoM of proposed design is excellent.

5 Conclusion

This paper presents an 83-pW subthreshold CMOS voltage reference implemented in a 0.18-um process. A GSC-NMOS is used to act as a large resistor (GΩ) and generate the bias current for the proposed circuit. Meantime, a self-biased transistor is added to make current source more ideal and eliminate DIBL effect of GSC-NMOS. Therefore, there is no need for resistors, which occupy large active area, or MOS transistors operating in deep triode region where a specific gate voltage is required to be concerned. The voltage reference proposed in this paper obtains a TC

Table 2 Summary of performance and comparison with other works

	This work	[12]* Tcas-I 2017	[14]* Tcas-II 2015	[23] MEJ 2020	[24]* Tcas-II 2019	[25]* JSSC 2017	[26] Analog 2020	[19]* JSSC 2012	[27] MEJ 2021
Technology [nm]	180	180	180	180	180	180	180	180	180
Power	83pW	147pW	14.6nW	21nW	1nW	24pW	2.4nW	5.5pW	196pW
Temp [°C]	−20–125	0–120	−40–125	−40–120	−40–125	0–100	−20–80	25–80	−20–120
TC [ppm/°C]	3.88	72.4	63.6	66.38	89.83	53	88	54.1	13.2
V_{REF} [mV]	209.2	256.6	118.46	147	151	1250	773	326.8	755.6
Supply [V]	0.45–1.8	0.45–3.3	0.4–1.8	0.7–1.8	0.4–1.8	1.4–3.6	0.95–2.2	0.5–3.6	1.0–1.8
LS [%/V]	0.011	0.15	1.01	0.76	0.163	0.31	0.073	0.044	0.0013
PSR [dB] @100 Hz	−65.54	−43.9	−44.2	−65	−49.6	−41	−41	−49	−56
Area [um^2]	2943	2000	12,000	10,000	500	2500	31,600	1425	6825
FoM** [$°C^3$/W x mm^2]	22.51	1.26	0.0024	0.0018	0.061	3.14	0.0015	26.001	1.1

*: Measurement results **: 10^{21}

of 3.88 ppm/°C and a LS of 0.011%/V. Simulation result show that the proposed reference voltage generator is suitable for IoT and biomedical devices due to its low power feature.

Appendix

Derivation of Eqs. (4) and (5) is shown below:

Firstly, only the forward inversion coefficient related to the source voltage is considered and Eq. (19) is obtained as:

$$\frac{V_G - V_{TH} - \eta V_S}{\eta V_T} = \sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right) \quad (19)$$

For the reason that $i_f \ll 1$, so Eq. (19) is expressed as:

$$\exp\left(\frac{V_G - V_{TH} - \eta V_S}{\eta V_T} + 1\right) = \sqrt{1+i_f} - 1 \quad (20)$$

The right side of Eq. (20) is expanded with Taylor series at $i_f = 0$ to get Eq. (21):

$$\sqrt{1+i_f} - 1 = 0 + \frac{i_f}{2} - \frac{(i_f)^2}{8} - \frac{(i_f)^3}{16} + R_3(i_f) \quad (21)$$

where $R_3(i_f)$ is the third-order Taylor residual term. Since $i_f \ll 1$, higher-order terms and Taylor residual term are ignored, formula (21) can be simplified to:

$$\sqrt{1+i_f} - 1 \approx \frac{1}{2} i_f \quad (22)$$

From Eqs. (20) to (22), it is obtained that:

$$i_f = 2e \exp\left(\frac{V_G - V_{TH} - \eta V_S}{\eta V_T}\right) \quad (23)$$

Similarly, it is obtained that:

$$i_r = 2e \exp\left(\frac{V_G - V_{TH} - \eta V_D}{\eta V_T}\right) \quad (24)$$

Hence, Eq. (5) can be obtained from Eqs. (1), (22) to (23):

$$\begin{aligned} I_D &= I_F - I_R \\ &= 2eI_S \exp\left(\frac{V_G - V_{TH}}{\eta V_T}\right)\left[\exp\left(\frac{-V_S}{V_T}\right) - \exp\left(\frac{-V_D}{V_T}\right)\right] \end{aligned} \quad (25)$$

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References

1. Mohan, R., Zaliasl, S., Gielen, G. G. E., Van Hoof, C., Yazicioglu, R. F., & Van Helleputte, N. (2017). A 0 6-V, 0 015-mm2, time-based ECG readout for ambulatory applications in 40-nm CMOS. *IEEE Journal of Solid-State Circuits, 52*(1), 298–308.
2. Feng, L., Zhao, Y., Guo, S., Qiu, X., Li, W., & Yu, P. (2021). *Blockchain-based asynchronous federated learning for internet of things*. Advance online publication.
3. Kim, H., Maeng, J., Park, I., Jeon, J., Lim, D., & Kim, C. (2021). A 90 2% peak efficiency multi-input single-inductor multi-output energy harvesting interface with double-conversion rejection technique and buck-based dual-conversion mode. *IEEE Journal of Solid-State Circuits, 56*(3), 961–971.
4. Ma, B., & Yu, F. (2014). A novel 1.2–V 4.5-ppm/°C curvature-compensated CMOS bandgap reference. *IEEE Transactions on Circuits and Systems I: Regular Papers, 61*(4), 1026–1035.
5. Chen, H., Lee, C., Jheng, S., Chen, W., & Lee, B. (2017). A Sub-1 ppm/°C precision bandgap reference with adjusted-temperature-curvature compensation. *IEEE Transactions on Circuits and Systems I: Regular Papers, 64*(6), 1308–1317.
6. Lee, K. K., Lande, T. S., & Häfliger, P. D. (2015). A Sub-µW bandgap reference circuit with an inherent curvature-compensation property. *IEEE Transactions on Circuits and Systems I: Regular Papers, 62*(1), 1–9.
7. Liu, L., Liao, X., & Mu, J. (2019). A 3.6 µ Vrms noise, 3 ppm/°C TC bandgap reference with offset/noise suppression and five-piece linear compensation. *IEEE Transactions on Circuits and Systems I: Regular Papers, 66*(10), 3786–3796.
8. Liang, J., et al. (2020). A −80 dB PSRR 4.99 ppm/°C TC bandgap reference with nonlinear compensation. *Microelectronics Journal, 95*, 0026–2692.
9. Ming, X., Hu, L., Xin, Y., Zhang, X., Gao, D., & Zhang, B. (2018). A high-precision resistor-less CMOS compensated bandgap reference based on successive voltage-step compensation. *IEEE Transactions on Circuits and Systems I: Regular Papers, 65*(12), 4086–4096.
10. Wang L., Zhan C., Tang J., Liu Y., and Li G. (2018). A 0 9-V 3 37-ppm/°C 85-nW sub-bandgap voltage reference consisting of subthreshold MOSFETs and single BJT. IEEE Transaction on Very Large Scale Integration (VLSI) Systems, 26(10), 2190–2194.
11. Wang, L., & Zhan, C. (2019). A 0.7-V 28-nW CMOS subthreshold voltage and current reference in one simple circuit. *IEEE Transactions on Circuits and Systems I: Regular Papers, 66*(9), 3457–3466.
12. de Oliveira, A. C., Cordova, D., Klimach, H., & Bampi, S. (2017). Picowatt, 0.45–0.6 V Self-biased subthreshold cmos voltage reference. *IEEE Transactions on Circuits and Systems I: Regular Papers, 64*(12), 3036–3046.
13. Wang, Y., Sun, Q., Luo, H., Wang, X., Zhang, R., & Zhang, H. (2020). A 48 pW, 0.34 V, 0.019%/V line sensitivity self-biased subthreshold voltage reference with DIBL effect compensation. *IEEE Transactions on Circuits and Systems I: Regular Papers, 67*(2), 611–621.
14. Wang, Y., Zhu, Z., Yao, J., & Yang, Y. (2015). A 0.45-V, 14.6-nW CMOS subthreshold voltage reference with no resistors and No BJTs. *IEEE Transactions on Circuits and Systems II: Express Briefs, 62*(7), 621–625.
15. Huang, Y., Zhu, L., Kong, F. P., Chun, C., & Najafizadeh, L. (2017). BiCMOS-based compensation: toward fully curvature-corrected bandgap reference circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers, 65*(4), 1–14.
16. Osaki Y., Hirose T., Kuroki N. and Numa M. (2013). 1.2-V Supply, 100-nW, 1.09-V Bandgap and 0.7-V Supply, 52.5-nW, 0.55-V Sub-bandgap Reference Circuits for Nanowatt CMOS LSIs. *IEEE Journal of Solid-State Circuits, 48*(6), 1530–1538.
17. Prasannakumar, A., Abraham, N. T., & Dhanaraj, K. (2020). MOSFETs-only sub-1-V voltage references for ultra-low-power

applications. *Analog Integrated Circuits and Signal Processing, 103*, 355–365.
18. Pereira-Rial Ó., Carrillo J.M., López P., Cabello D. (2021). A 0.6V, ultra-low power, 1060 μm^2 self-biased PTAT voltage generator for implantable biomedical devices. AEU–International Journal of Electronics and Communications, 137.
19. Schneider, M. C., & Galup-Montoro, C. (2010). *CMOS analog design using all-region MOSFET Modeling* (1st ed.). Cambridge Univ. Press.
20. Tsividis, Y. (1987). *Operation and modeling of the MOS transistor*. McGraw-Hill.
21. Luo, H., Han, Y., Cheung, R. C. C., Liang, G., & Zhu, D. (2012). Subthreshold CMOS voltage reference circuit with body bias compensation for process variation. *IET Circuits, Devices and Systems, 6*(3), 198–203.
22. Chamberlain, S. G., & Ramanan, S. (1986). Drain-induced barrier-lowering analysis in VSLI MOSFET devices using two-dimensional numerical simulations. *IEEE Transactions on Electron Devices, 33*(11), 1745–1753.
23. Aminzadeh H., Valinezhad M. M. (2020). 0.7-V supply, 21-nW All–MOS voltage reference using a MOS-Only current-driven reference core in digital CMOS. *Microelectronics Journal, 102*.
24. Lin, J., Wang, L., Zhan, C., & Lu, Y. (2019). A 1-nW ultra-low voltage subthreshold CMOS voltage reference with 0.0154%/V line sensitivity. *IEEE Transactions on Circuits and Systems II: Express Briefs, 66*(10), 1653–1657.
25. Lee, I., Sylvester, D., & Blaauw, D. (2017). A subthreshold voltage reference with scalable output voltage for low-power IoT systems. *IEEE Journal of Solid-State Circuits, 52*(5), 1443–1449.
26. Seok, M., Kim, G., Blaauw, D., & Sylvester, D. (2012). A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V. *IEEE Journal of Solid-State Circuits, 47*(10), 2534–2545.
27. Hu, J. L., Xu, H. C., Wang, J., Liang, K., Lu, C., & Li, G. F. (2021). A 26-ppm/°C, 13.2-ppm/V, 0.11%-inaccuracy picowatt voltage reference with PVT compensation and fast startup. *Microelectronics Journal, 115*, 0026–2692.

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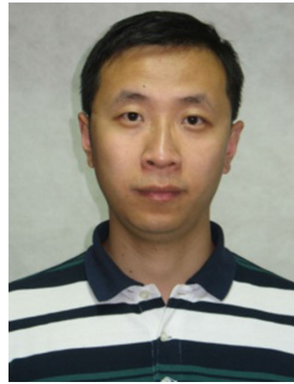

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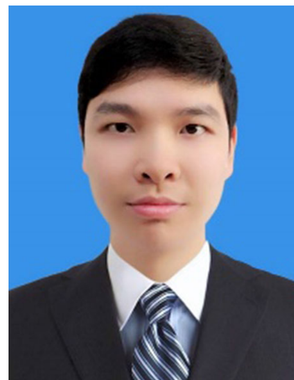

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