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New grounded passive elements-based external multiplier-less memelement emulator to realize the floating meminductor and memristor

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Abstract
A novel memelement emulator configuration has been reported in the presented work. This proposed configuration can be used to realize the function of a floating meminductor as well as the memristor element through proper selection of employed passive elements. The presented emulator circuit is based on MVDCC (modified VDCC) and OTA, which are CMOS implemented electronically tunable ABBs (Active Building Blocks). The designed circuit employs only two ABBs and three grounded passive elements. As per the knowledge of the authors, no such emulation configuration with a floating architecture has been reported so far, which can realize the behaviour of two mem-elements without the use of any external multiplier IC/circuitry, passive inductor or mutation through any externally employed memelement. It can be considered as a notable design feature along with its other advantages like electronically/resistively tunable emulated response and use of only grounded passive elements. Moreover, proposed circuit has been investigated for the consideration of non-idealities and different port parasitics of employed blocks. For the verification purpose, PSPICE simulation environment with CMOS 0.18 μm TSMC technology parameters, has been selected. The functioning of the realized meminductive and memristive behaviour has also been verified through the application example circuits designed using developed emulator circuit. Afterwards, the commercial IC based realization of the proposed emulator circuit has been shown and experimental results are discussed.

Keywords Memelement emulator · Memristor · Meminductor · MVDCC

1 Introduction

Among the three memelements, memristor has been considered as the fourth fundamental element by various researchers unlike to the meminductor and memcapacitor. It is due to the fact that it was proposed for the relationship of charge and flux, which are the two of the basic electrical quantities [1]. And also, the notion of other of two memelements was motivated from the concept of memristor only, which were defined to relate the associated quantities corresponding to the conventional inductor and capacitor [2]. Nevertheless, these two new memelements have also been considered to be useful just like the memristor due to the hysteresis property, they exhibit in their related transient characteristics, which gives rise to the storage ability in these elements. Some, mathematical works can be found, which focus on the theoretical aspects of memcapacitors and meminductors [3, 4].

Now, the realization of the memristor element based on electronic circuit designing (as well as through material-based implementations), has been a popular research area since the last decade (some popular memristor emulator circuits have been reported in [5–20] and the references cited there in). But there are only limited number of articles in the open literature available on the realization of meminductor and memcapacitor [21–51]. These papers [21–51] only include the analogue circuit-based implementations as the physical architecture-based realizations of these two memelements have not been proposed so far.

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The emulation configurations suggested in [21–51] are based on different active elements like; First generation current conveyor (CCI) [33–41], Second Generation Current Conveyor (CCII) [33, 38, 41, 48], Operational Amplifier(OA) [15, 34, 39–41, 43, 45, 46, 49], Operational Transconductance Amplifier (OTA) [32, 36, 37, 48], Current Buffered Transconductance Amplifier (CBTA) [35], Voltage differencing Transconductance Amplifier (VDTA) [32–42], Differential Voltage Current Controlled Transconductance Amplifier(DVCCTA) [29] and some others.

Most of the emulators presented in [15, 21–51] are dedicated to the realization of only single memelement (memcapacitor or meminductor) with grounded or floating architectures. These also include some emulators (like those are reported in [15, 21, 22, 33, 35, 41, 47, 48, 50]), which can realize the function of any two or all the three memelements just like the proposed memelement emulator circuit. These reported circuits are not preferrable as compared to the proposed memelement emulator and as these are based upon a greater number of active and passive elements also offers no provision of electronic/resistance control facility. The use of analog multiplier IC in some of these circuits [21, 35, 41, 47] make these emulators even bulkier as compared to the circuits which are based upon multiplier-IC less structure like the proposed one.

The main claim of this work is the compact floating meminductor emulator designed using MVDCC and OTA. The realizability of the memristor can be seen as an additional advantage of the proposed circuit. The comparison has been shown in Table 1, which highlights the different design and performance related aspects of the previously reported meminductor emulators only [15, 32–51] and shows the superiority of the proposed one.

Based on the various parameters compared in Table 1, the meminductors reported in [15, 32–51] are found to be suffering from one or more of the following major issues like; emulation of only grounded architecture, use of more than two ABBs, use of external multiplier IC/ICs, no facility of tuning, use of floating passive elements, exhibition of very low operating bandwidth (few KHzs), realization through mutation using external memristor emulator, use of passive inductor and requirement of matched parameter/component values. On the other end, the proposed circuit is free from such disadvantages and realizes a floating meminductor emulator using a MVDCC and an OTA with three grounded passive elements only.

Now, as far as the performance of any memelement emulator is concerned it is generally measured by the aspects like; frequency dependency of the ϕ–i curves (pinched hysteresis loops (PHLs), symmetry of the PHL lobes, maximum frequency up to which satisfactory loop can be obtained, availability of electronic tuning and presence of non-volatility in the realized memelement. There are following performance related shortcomings with the previously reported meminductor emulators [15, 32–51] as compared to the proposed one:

1. In some of the meminductor emulators reported previously [33–35, 39, 43, 45, 47, 49], there was lack of symmetry in the PHL characteristics presented, while proposed circuit offers satisfactory symmetry in both the opposite quadrants.
2. The maximum operating frequency offered by some emulators [15, 33–41, 43–47, 49] is less than 100 kHz, while presented circuit provides the maximum operating frequency up to 300 kHz.
3. The works discussed in [15, 33–35, 37–41, 43–47, 49, 50] have not investigated the non-volatility property of the realized meminductor emulator, while presented simulation results clearly validates the non-volatility of the proposed memelement emulator.
4. In the meminductor emulator given in any kind of tunability feature is not present [15, 33, 35, 37–43, 45–50], while our circuit is tunable through biasing voltage as well as the external resistance.
5. The meminductor emulators given in [33, 34, 38, 43] do not show ideal behaviour on varying the applied signal frequency. While, this frequency dependency of the proposed meminductor emulator can be clearly witnessed from the presented simulation results.

Along with these advantages offered by the realized meminductor, its ability to exhibit the ideal memristor behaviour can also be considered as an additional remarkable benefit. Although, the main contribution of the work is the proposed compact floating meminductor, but still some of the advantages of the memristor emulation configuration over some of the previously reported memristor emulators [5–20] cannot be ignored. Like the floating memristor emulators described in [5, 6, 9, 12, 14–17] use two or more active elements and/or are based upon the large number of passive elements (more than three), whereas the proposed circuit is based on just two MVDCCs and three grounded passive elements. Also, the realized memristor emulator does not require any external voltage multiplier, which can be considered as an advantage over previously reported multiplier based memristor emulators [5, 6, 10, 14, 16, 17]. Furthermore, some of those configurations, claimed as floating memristor, are not fully floating [6, 13, 14] (i.e. two terminals cannot be used interchangeably when used as a floating element), while proposed memristor emulator simulates a fully floating memristor, which is an attractive feature of floating topology. While, memristor emulators reported in [18, 19] realize only grounded memristor emulator.

Table 1 Overview of the different design related details of the previously reported meminductor emulators in [15, 32–51]

S. no.	Fig. no. of reported emulator	Type of memr-istor (F^1/G^2)	No. of active elements	No. of ext Multi-plier IC	Avail-ability of elect-ronic Tuna-bility (Y^3/N^4)	No. of passive elements	Maximum operating frequency (HZs)	Need of muta-tion using memristor (Y(F/G)N(F/G)/	Use of Pass-ive Ind-uctor	Need of com-pon-ent Mat-ching cond-ition
[15]	Fig. 1a	F	4AD844s, 1 Op-Amp, 1 Varactor Diode	NIL	N	4F&2G	22 kHz	N	N	Y
[32]	Fig. 1	G	1 VDTA, 1 OTA	NIL	Y	2G	–	N	N	N
[33]	Fig. 1a and Fig. 2a	F/F	4 CCII/2CCI	NIL/NIL	N	1F&1G/ 1F&1G	Not sh-own	Y(F)/Y(G)	N	N/N
[34]	Fig. 2/Fig. 3	F/F	2 integrators, 2 inverting gain amps., multiplier, adder/2 inverting amps., 2 adders, multiplier	NIL	N	Not shown	20 kHz	N	N	Not shown
[35]	Fig. 3c	F	2 CBTA	1	N	1G	200 kHz	Y(G)	N	N
[36]	Fig. 2	G	1 OTA, 1 MO-OTA	1	Y	2F&2G	10 kHz	N	N	N
[37]	Fig. 3	G	1 OTA, 1 VS	NIL	N	2G&1F	500 Hz	N	Y	N
[38]	Fig. 3	G	1 CCII, 3 OP-AMPS	1	N	4F	400 Hz	Y(G)	N	N
[39]	Fig. 6	G	5 OP-AMPS	NIL	N	7F&1G	10 kHz	N	N	Y
[40]	Fig. 2a	G	3 OP-AMPS, 12 MOS	1	N	2F&3G	300 Hz	N	Y	Y
[41]	Fig. 2	F/G	5 CCII, 1 OP-AMP/3CCII	1/1	N	1F&6G/ 5G	5 kHz	N/N	N	N/N
[42]	Fig. 3/Fig. 5 /Fig. 6	G/G/F	2VDTA/2VDTA/2VDTA	1/NIL/ NIL	Y	2G/2G/3G	600 kHz	N/N/N	N	Y
[43]	Figure 1	G	6 OP-AMPS	2	N	14F	100 Hz	N	N	N
[44]	Fig. 1	F	3 AD844, 1 CA3080, 1 LM13700	1	Y	5F/3G	5 kHz	N	N	Y
[45]	Fig. 3b	G	7 OP-AMPS	1	N	16F	300 Hz	N	N	N
[46]	Fig. 3	G	6 OP-AMPS	3	N	11F	300 Hz	N	N	Y
[47]	Fig. 11	F	5 AD844s	1	N	5F/3G	100 kHz	N	N	N
[48]	Fig. 5	G	2 CCIIs, 1 OTA	NIL	N	4G	400 kHz	N	N	N
[49]	Fig. 2a, b, c, d, e, f	G/G/G/ G/G/ G	2 Op-Amps (each circuit)	NIL(each circuit)	N(each circuit)	3F/1G (each circuit)	2 MHz (each circuit)	Y(F)/Y(G)/ Y(F)/Y(F)/ Y(F)/Y(F)	N (each circuit)	Y(each circuit)
[50]	Fig. 3	F	2 VDCC	NIL	N	2G	0.7 MHz	Y(G)	N	Y
[51]	Fig. 4	F	2VDTA	NIL	Y	2G	1.5 MHz	N	N	N
Proposed	Fig. 4	F	1MVDCC, 1 OTA	NIL	Y	3G	300 kHz	N	N	N

F^1 = Floating, G^2 = Grounded, Y^3 = Yes, N^4 = No

In the following discussion, we have mentioned the basic relationships of voltage-controlled and flux-controlled memristor and meminductor respectively, which are the basis for the realization of these memelements.

1.1 Memristor and meminductor

It is important to understand that all the three memelements actually relate only those quantities, which are associated to their conventional counterpart. Like, the memristor, which basically links only the current/voltage to the voltage/current (just like a resistor), but its flux/charge-dependent conductance/resistance makes all the difference.

Below, the current(i)-voltage(v) relationship of voltage controlled memristor has been given in Eq. 1, with the equivalent memductance represented as G_M.

$$i(t) = G_M\left(\int_0^t v(t)\mathrm{d}t\right)v(t) \tag{1}$$

The memductance G_M given in Eq. 1, is generally realized by using the expression given in Eq. 2, which is the function of integration of voltage i.e. flux ϕ.

$$G_M = (a_0 + a_1\varphi) \tag{2}$$

(The a_0 and a_1 are memristor coefficients)

Similarly, it was argued in [2] that the capacitance and inductance, whose values depend upon the integration of charge/flux, (which are the quantities associated to conventional capacitor/inductor) can be considered as memcapacitor and meminductor, if these elements also relate the basic capacitive and inductive quantities. It is important to emphasize that it is the dependency upon the integration of the electrical quantity, that provides the storage feature in these memelements. Now, the current–voltage relationship of meminductor element is represented by the following equation;

$$i(t) = L_M^{-1}\left(\int_0^t \varphi\mathrm{d}t\right)\varphi \tag{3}$$

where φ is the flux, given by $\varphi(t) = \int_0^t v(t)\mathrm{d}t$ and $\mathrm{L_M}^{-1}$ represents the inverse meminductance, which is generally taken as Eq. 4 for the circuit-based realization of meminductor emulators.

$$L_M^{-1} = (a_0 + a_1\rho) \tag{4}$$

(The a_0 and a_1 are meminductor coefficients)

where

$$\rho(t) = \int_0^t \varphi dt = \int_0^t\int_0^t v(t)\mathrm{d}t\mathrm{d}t \tag{5}$$

2 Proposed configuration

Based on the discussion presented in the previous section, we have designed the memelement emulator to realize the relationship given in Eqs. 1 and 3. The proposed realization is based on the MVDCC and OTA blocks. The MVDCC is an extension of the VDCC Voltage Differencing Current Conveyor) concept, which is explained below.

2.1 MVDCC (modified VDCC)

The notion of VDCC was first proposed in the seminal paper authored by Biolek et al. in 2008 [52]. Later, it was found to be applicable in several types of analog signal processing/generation circuits [53–55] and still remains popular among analog circuit designers. In the VDCC active element, the Z port provides the current output of input transconductance stage and developed potential at the Z terminal is transferred to the X port. The CMOS implementation of VDCC was first reported in [56]. Now, authors have realized that having a dual Z ports (with both negative and positive current output) and proportional (to this differential Z input) current at the $\mathrm{W_P}$ and $\mathrm{W_N}$ ports, the versatility of the VDCC can be improved. And, with these modifications in the CMOS implementation given in [56], the VDCC can be transformed into MVDCC (modified VDCC). The CMOS implementation of MVDCC and its symbolic representation can be given as Figs. 1 and 2 respectively. In [57], the application of MVDCC as a floating memristor and its CMOS implementation were first suggested. Also, the ports' relationships of MVDCC are described in Eq. 6.

$$\begin{bmatrix} I_P \\ I_N \\ I_{Z+} \\ I_{Z-} \\ V_X \\ I_{W_P} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ -g_m & g_m & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_{Z+} \\ V_{Z-} \\ I_X \end{bmatrix} \tag{6}$$

The symbol g_m in Eq. 7, represents the transconductance of the input stage of MVDCC, which can be controlled by the applied bias voltage $\mathrm{V_{B1}}$ as the relationship given in Eq. 7 suggests,

$$g_m = k(V_{B1} - V_t - V_{SS}) \tag{7}$$

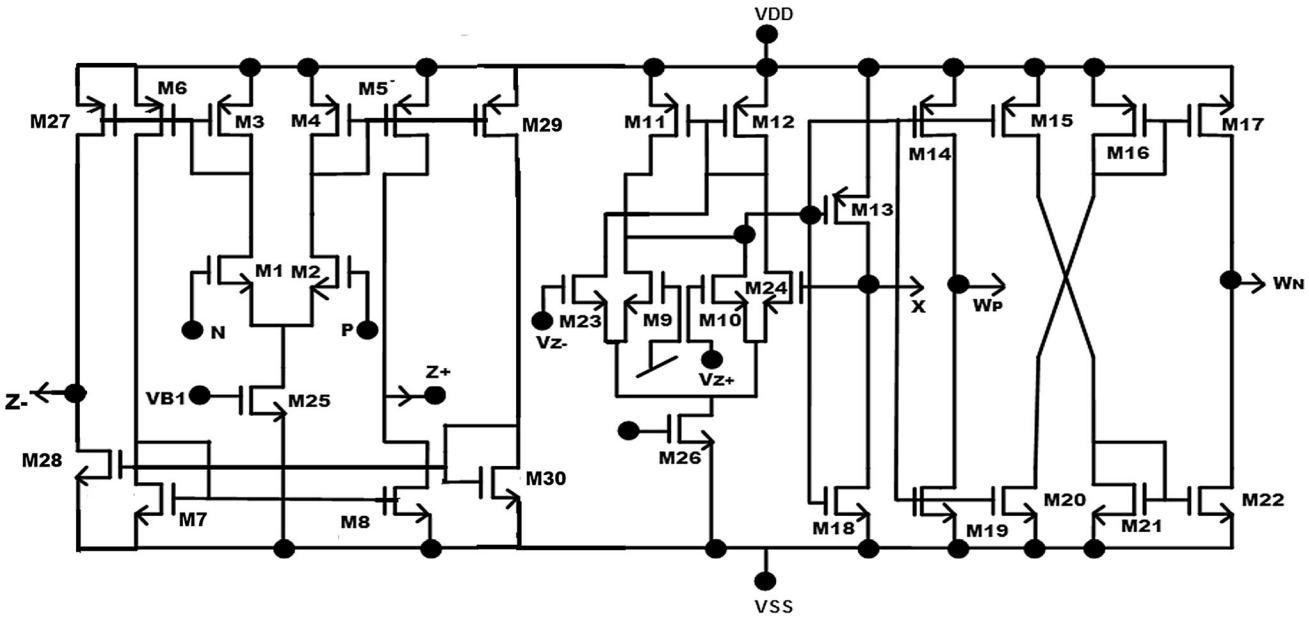

Fig. 1 CMOS realization of MVDCC

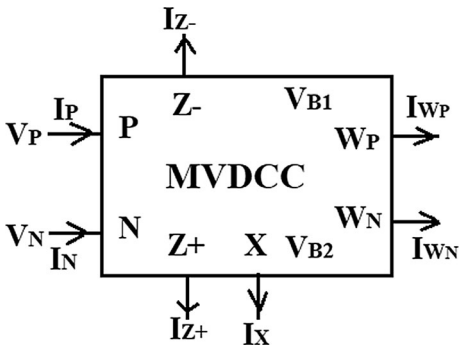

Fig. 2 Representation of modified VDCC(MVDCC)

Along with VDCC, we have also used the OTA block in the realization of presented memelement emulator. The OTA is a conventional and popular active element used as a transconductance amplifier. The employed CMOS implementation of OTA is shown in Fig. 3. For OTA, the output current is $I_Z = g_{m0}\ (V_P - V_N)$ with g_{m0} being the transconductance gain, depends upon biasing voltage V_B.

2.2 Proposed memelement emulator using MVDCC and OTA

Finally, the proposed circuit emulator to realize the behaviour of a floating meminductor and memristor is presented in Fig. 4. The suggested configuration is based on MVDCC and OTA and three grounded elements. The impedance Z_1 present in the designed circuit can be used to select the functioning of this memelement emulator as meminductor and memristor respectively.

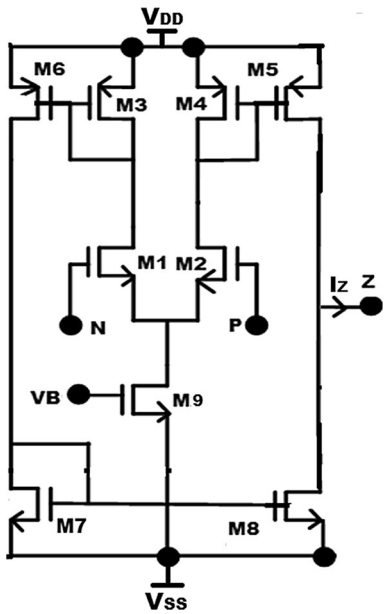

Fig. 3 CMOS based implementation of OTA

Case-1 Meminductor (When Z_1 is selected as capacitance C_1)

In this condition, the expression for the generated input current for the circuit given in Fig. 4 is computed as following.

For routine circuital analysis (using Eq. 6) and through application of Kirchhoff's laws, the input currents I_1 and I_2 are found to be equal and opposite for the depicted circuit;

$$I_1 = -I_2 = I_{in} \tag{8}$$

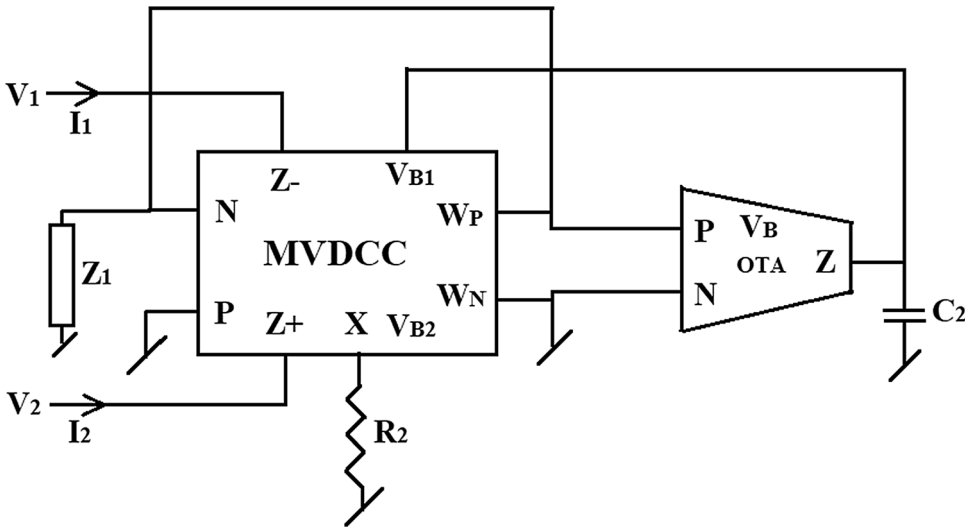

Fig. 4 Proposed MVDCC and OTA based architecture of memelement emulator

Now this I_{in} shown in Eq. 8, can be computed using Eqs. 6 and 7 as;

$$I_{in} = k\frac{1}{C_1R_2}\left(\frac{g_{m0}}{R_2C_1C_2}\int_0^t\int_0^t (V_2 - V_1)\mathrm{d}t\mathrm{d}t - V_{SS} - V_t\right)\int_0^t (V_2 - V_1)\mathrm{d}t \tag{9}$$

where $\int_0^t (V_2 - V_1)\mathrm{d}t$ is the input voltage flux φ and $\int_0^t\int_0^t (V_2 - V_1)\mathrm{d}t\mathrm{d}t$ is flux density ρ as explained in Eqs. 4 and 5. Also the g_{m0} is the transconductance of employed OTA.

From Eq. 9, it can be clearly observed that this relationship is associated to a meminductor function with the equivalent inverse meminductance can be found by comparing Eq. 9 with 3 as;

$$L^{-1} = k_1\frac{1}{C_1R_2}\left(\frac{g_{m0}}{R_2C_1C_2}\rho - V_{SS} - V_t\right) \tag{10}$$

Case-2 Memristor (when Z_1 is selected as resistance R_1)

Similarly, the circuit will act as a memristor emulator, if Z_1 is chosen as the resistance R_1. Now, by using Eqs. 6 and 7, the admittance matrix of the memristor emulator relating the voltages V_1, V_2 to I_1 and I_2 can be evaluated as;

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = k\frac{R_1}{R_2}\left(\frac{g_{m0}R_1}{R_2C_2}\int (V_2 - V_1)\mathrm{d}t - V_{SS} - V_t\right)\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{11}$$

From Eq. 11, it can be clearly observed that the circuit presented in Fig. 4 realizes the behavior of a floating memristor with memductance G_M equals to;

$$G_M = k\frac{R_1}{R_2}\left(\frac{g_{m0}R_1}{R_2C_2}\int (V_2 - V_1)\mathrm{d}t - V_{SS} - V_t\right) \tag{12}$$

It can be observed from the expressions given in Eqs. 10 and 12, the behavior of the realized meminductance and memductance, can be controlled electronically by varying transconductance of employed OTA g_{m0}, which depends upon biasing voltage V_B. And most importantly, to achieve the multiplication of analog voltages/fluxes shown in the current expressions, the designed circuit does not use any external analog multiplier which is the major advantage of the proposed memelement emulator.

3 Effect of non-ideal gains and terminal parasitics of MVDCC and OTA

Now, we have investigated the effect of non-ideal gains and terminal parasitics of VDCC and OTA on the realized function of proposed memelement emulator. In Eq. 13, we have shown the matrix of VDCC with non-ideal gains, and Eq. 14 shows the current–voltage relationship of an OTA with non-ideality factor α_0.

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ V_X \\ I_{W_P} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \beta g_m & -\beta g_m & 0 & 0 \\ 0 & 0 & k' & 0 \\ 0 & 0 & 0 & \gamma \\ 0 & 0 & 0 & -\gamma \end{bmatrix}\begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix} \tag{13}$$

$$I_o = \alpha_0 g_{mo}(V_P - V_N) \tag{14}$$

Furthermore, the parasitic model of VDCC is shown in Fig. 5, with different parasitic resistances and capacitances connected at the terminals in different configurations. This parasitic model was discussed in [54]. Similarly, the parasitic effect in the OTA can be considered as a grounded resistance R_0 connected at the output terminal.

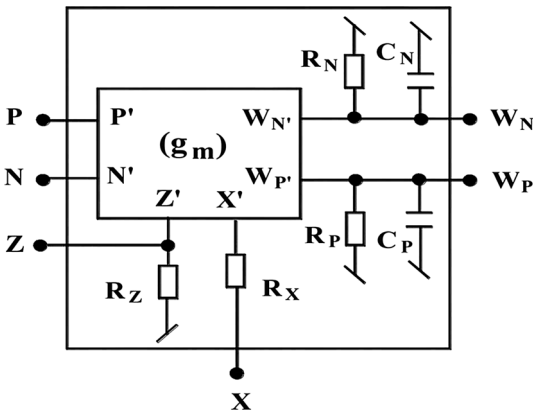

Fig. 5 VDCC parasitic model given in [54]

The Fig. 6 demonstrates the circuit of proposed emulator with port parasitics of VDCC and OTA.

In this circuit, the voltage $V_{in} = V_1 - V_2$ is applied as the input to the circuit. Due to symmetry property, we can assume, $V_{in}/2$ and $-V_{in}/2$ is applied at both the terminals of the emulator circuit respectively. For, $R_{Z-} = R_{Z+} = R_Z$, we can compute that;

$$I_{IN} = I_1 = -I_2 \tag{15}$$

On further calculation, the I_{IN} is calculated as;

$$I_{IN} = \beta k\left(\frac{k'\gamma V_{in}}{R_X + R_2}\right)\left(\frac{Z1||R'}{1 + sC'Z1||R'}\right)\left(\alpha_0 g_{m0}\left(\frac{k'\gamma V_{in}}{R_X + R_2}\right)\left(\frac{Z1||R'}{1 + sC'Z1||R'}\right)\left(\frac{R_0}{1 + sR_0C_2}\right) - V_{SS} - V_t\right) + V_{in}/(R_Z/2) \tag{16}$$

When Z_1 is chosen as R_1 (the case of memristor),

$$I_{IN} = \beta k\left(\frac{k'\gamma V_{in}}{R_X + R_2}\right)\left(\frac{R_1||R'}{1 + sC'R_1||R'}\right)\left(\alpha_0 g_{m0}\left(\frac{k'\gamma V_{in}}{R_X + R_2}\right)\left(\frac{R_1||R'}{1 + sC'R_1||R'}\right)\left(\frac{R_0}{1 + sR_0C_2}\right) - V_{SS} - V_t\right) + V_{in}/(R_Z/2) \tag{17}$$

When Z_1 is chosen as C_1 (the case of meminductor),

$$I_{IN} = \beta k\left(\frac{k'\gamma V_{in}}{R_X + R_2}\right)\left(\frac{R'}{1 + s(C_1 + C')R'}\right)\left(\alpha_0 g_{m0}\left(\frac{k'\gamma V_{in}}{R_X + R_2}\right)\left(\frac{R'}{1 + s(C_1 + C')R'}\right)\left(\frac{R_0}{1 + sR_0C_2}\right) - V_{SS} - V_t\right) + V_{in}/(R_Z/2) \tag{18}$$

From Eq. 17, it can be observed that under the effects of parasitics, the memristor may show the behavior of a meminductor element. And from Eq. 18, we can see that at operating frequencies significant high, we can assume; $s(C_1 + C')R' \gg 1$ and also $sR_0C_2 \gg 1$ and the circuit will act can act as considerable meminductor with some non-ideal gains.

4 Simulation results

For the purpose of validation of the proposed mem-element emulator, we have performed the simulation using PSPICE environment for the CMOS implementation (depicted in

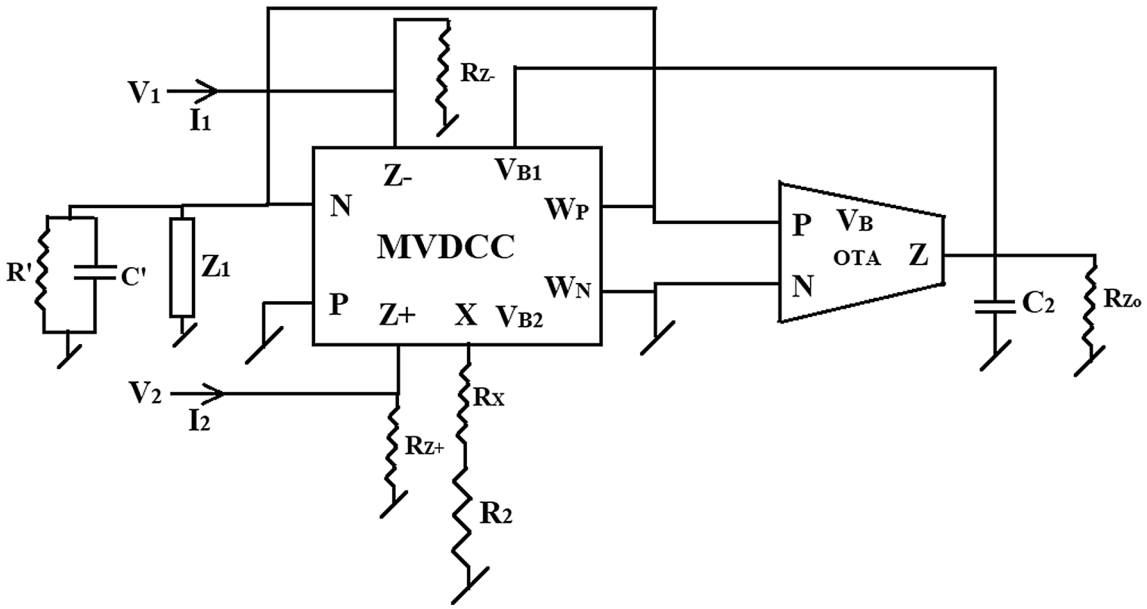

Fig. 6 Proposed floating memelement emulator with port parasitics of MVDCC and OTA

Table 2 W/L ratios of CMOS transistors employed in circuit shown in Fig. 2

Transistors	W/L ratio (μm/μm)
M1-M4	3.6/1.8
M5-M6, M27, M29	7.2/1.8
M7-M8, M28, M30	2.4/1.8
M9-M10, M23-M24	3.06/0.72
M11-M12	9/0.72
M13-M17	14.4/0.72
M18-M22	0.72/0.72
M25	3.6/1.8
M26	3.06/0.72

Table 3 W/L ratios of CMOS transistors employed in the OTA (Fig. 3)

Transistors	W/L ratio (μm/μm)
M1-M4	3.6/1.8
M5-M6	7.2/1.8
M7-M8	2.4/1.8
M9	3.6/1.8

Figs. 2 and 3) of MVDCC and OTA. The selected aspect ratios of the MOS transistors used in Figs. 2 and 3 are shown in Tables 2 and 3 respectively. The power supply value is taken as $V_{DD,\ SS} = \pm 0.9$ V. And the.

Initially, we have executed the simulations for realized meminductor by selecting the Z_1 as capacitance C_1 in the proposed design shown in Fig. 4. Now, upon application of a sinusoidal excitation, the obtained Pinched Hysteresis Loops (PHLs) are depicted from Figs. 7, 8 and 9. These hysteresis loops are plotted between the generated input current I_{in} and capacitance voltage V_{CI}(volts). Ideally, we should be plotting the curve between I_{in} and flux of the input voltage, φ. But, as in PSPICE, x-axis variable cannot be selected as the integration of the input voltage (i.e. φ), we had to choose the capacitance voltage V_{CI}, which is the potential value proportional to the integration of input voltage (as per the configuration of the proposed circuit), which serves our purpose as the desired x-axis variable. It is important to clarify that product term ($1/R_2C_1$) along with the integration of input voltage, remains constant during the simulation and does not influence the ideal nature of the plotted hysteresis curves. These φ-i curves are plotted for the selected parameters as; $C_1 = 2$ pF, $C_2 = 3$ pF, and $R_2 = 1$ K at input signal frequency as $F_{in} = 200$ kHz. Moreover, the peak value of the sinusoidal signal is taken as $V_P = 0.05$ V and the biasing voltages are kept at $V_{BS2} = 0.45$ V and $V_{BS} = 0.4$ V (biasing voltage of second stage of MVDCC and OTA respectively applied at the biasing terminals with respect to source supply V_{SS}).

The plots shown in Figs. 7 and 8 illustrate the tuning facility available in the developed emulator configuration.

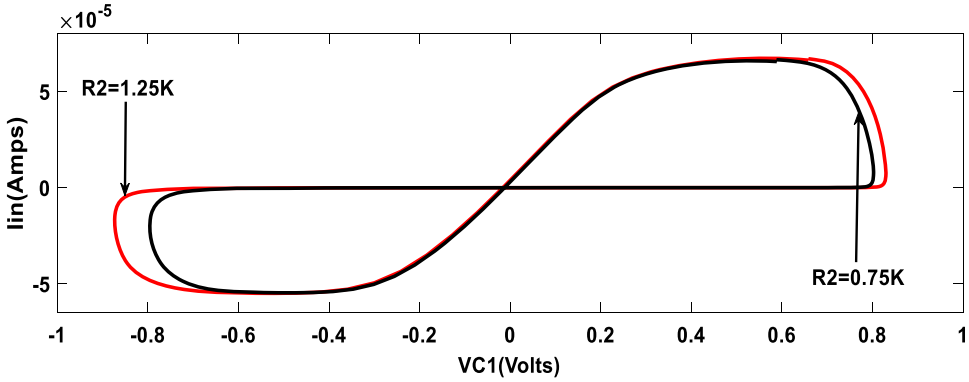

Fig. 7 Plots showing the tunable nature of realized meminductor through resistance R_2

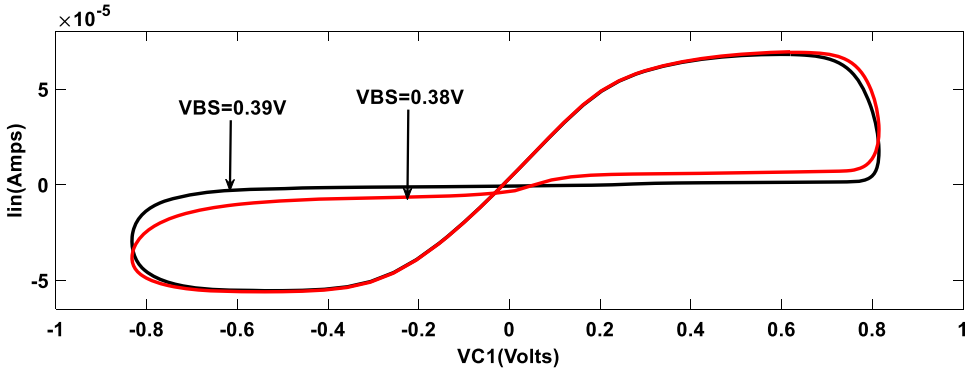

Fig. 8 Demonstration of electronic tunability feature through biasing voltage V_{BS}

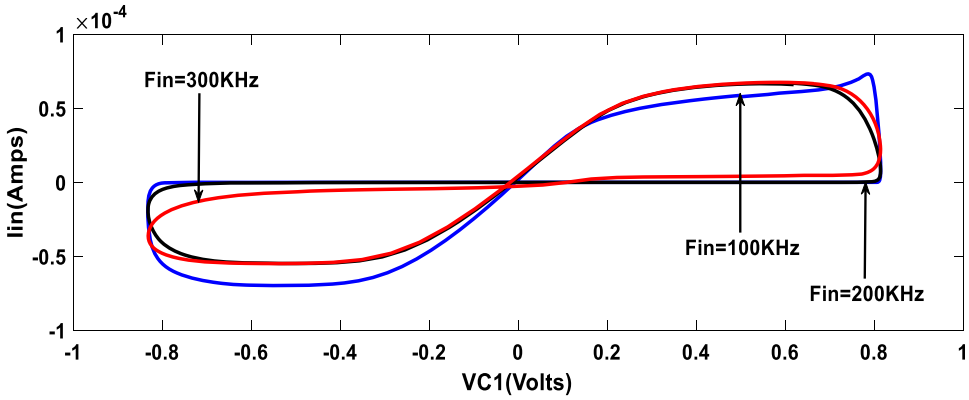

Fig. 9 Hysteresis curves plotted at different values of operating frequency

These curves have been plotted by keeping all other parameters fixed except the resistance R_2 and biasing voltage V_{BS} respectively. It can be observed from the plot shown in Fig. 7 that emulated hysteresis behaviour in φ-i plane can be varied with the help of employed resistance R_2. And also, as depicted by the plots given in Fig. 8, that realized meminductor behaviour can also be controlled using biasing voltage V_{BS}. Next, we have plotted the transient characteristics of the realized meminductor at different values of the operating signal frequencies. These φ-i curves are shown in Fig. 9, which clearly demonstrate the change in the enclosed area of the contours with respect to variation in the applied signal frequency.

As already discussed, that potential across the capacitance C_1, is proportional to the input flux ϕ, hence, transient response of the V_{C1} can be plotted to show the response of ϕ. So, it has been plotted in Fig. 10(a) and also, the corresponding current behavior of the meminductor is also plotted and shown in Fig. 10(b). We can observe that there is a non-symmetry appearing in the two adjacent quarter cycles of the current both in positive and negative directions. This unsymmetric behaviour is indicating the hysteresis nature of the meminductor found the transient φ-i curves. Similarly, we have traced the transient variation of the input inverse meminductance of the developed emulator circuit, which has been plotted in Fig. 11. The presence of the peaks in the response may be associated to the

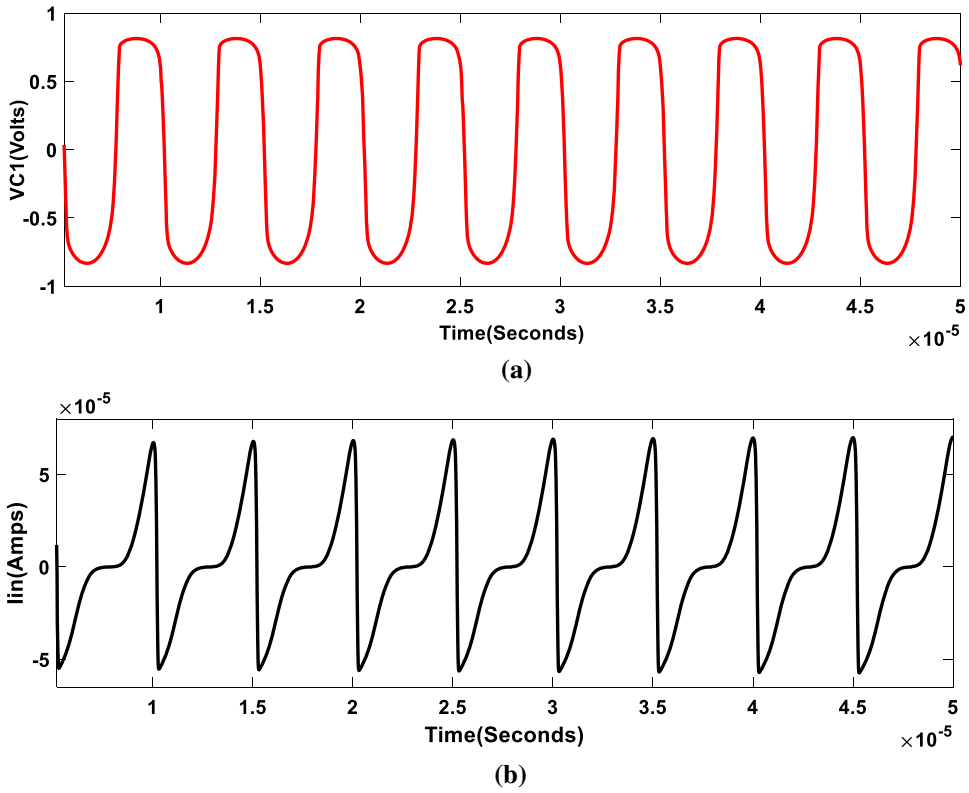

Fig. 10 Plotted response of instantaneous flux (illustrated through V_{C1}) and generated current at 200 kHz

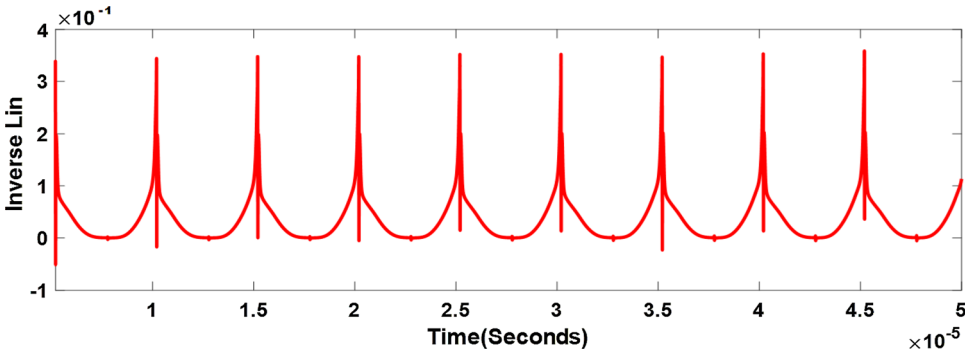

Fig. 11 Simulated response of inverse meminductance with time at F_{in} = 200 kHz

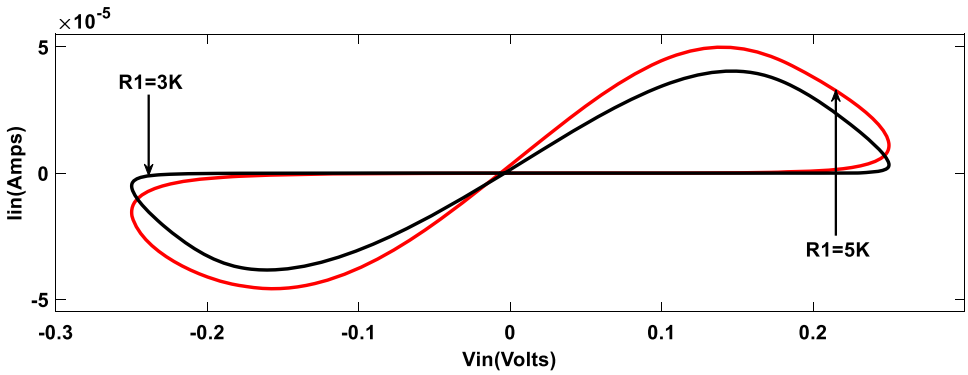

Fig. 12 Change in hysteresis behaviour of the memristor with variation in R_1

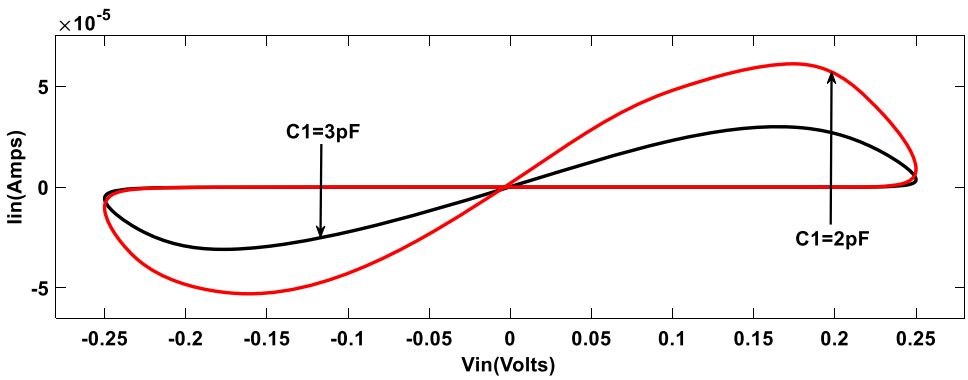

Fig. 13 Effect of employed capacitance C_2 on transient charactersitics

extreme parts of the transient φ-i curves, where the current show steep decline and rise. From Fig. 11, we can find the max. and min. value of inverse meminductance. From which, the range of the meminductance can be calculated as; 2.85H to almost 10H. (Here, we are not considering the notches of the curve, which are corresponding to the transient behavior observed at the edges of the PHLs, at which meminductance approaches to infinite for a small time period.)

Furthermore, the operation of the realized memristor element can be demonstrated through the presented simulation results. The memristor response can be achieved by choosing the grounded impedance Z_1 as resistance R_1. The simulations have been executed for the selected parameters as; R_1 = 4 K, R_2 = 2 K and C_2 = 2.5 pF with peak input value as V_P = 0.25 V at F_{in} = 150 K. And the biasing voltages are chosen as; V_{BS2} = 0.45 V and V_{BS} = 0.4 V. Firstly, we have run the simulations to investigate the impact of passive elements and biasing voltage on the emulated memristive behaviour. These transient v-i curves have been illustrated in Figs. 12, 13 and 14, which have been obtained for different values of R_1, C_2 and biasing voltage V_{BS} respectively. From the three plots, it can be easily determined that realized memristor function is controllable through grounded passive elements as well as the biasing voltage. Next, the frequency dependence response of the enclosed area under contour curves is studied and simulation plots are shown in Fig. 15. From the plots given

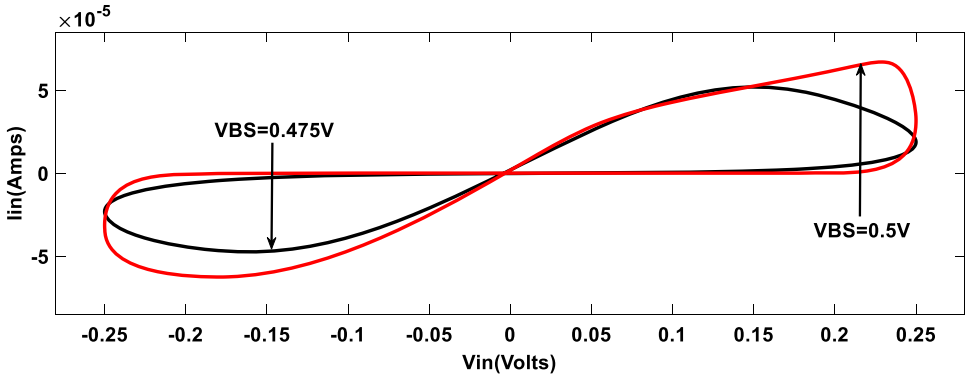

Fig. 14 Electronically tunable response of the realized memductance via voltage V_{BS}

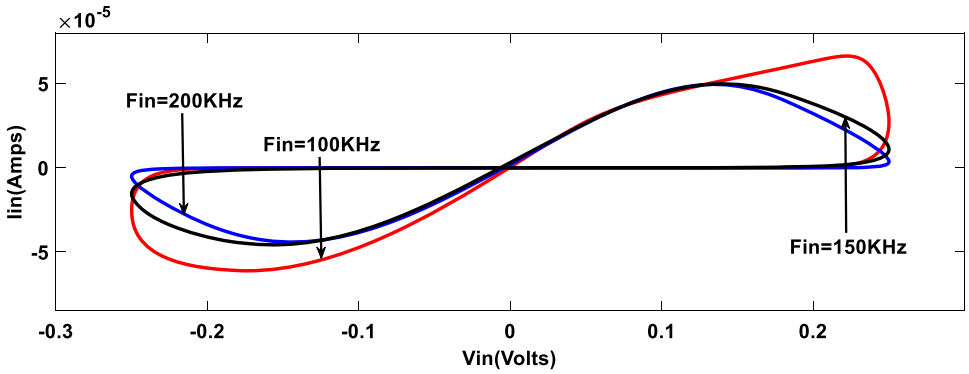

Fig. 15 Frequency dependent nature of realized floating memristor emulator with sinusoidal excitation

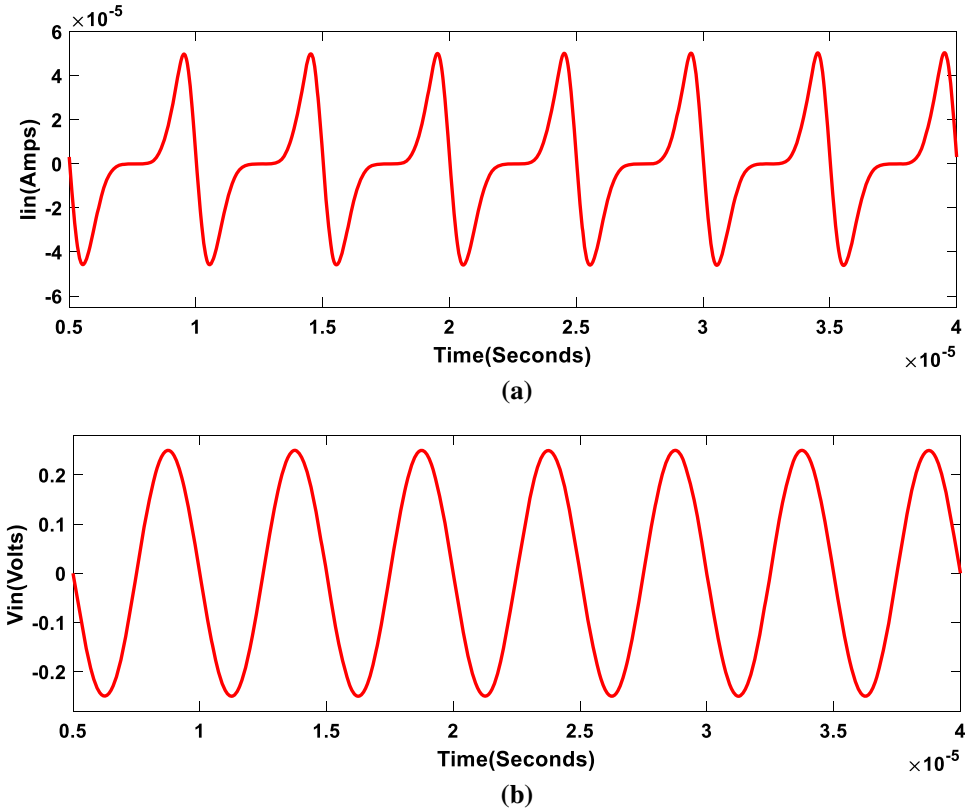

Fig. 16 Transient response of generated memristor current at 200 kHz (**a**) for applied voltage shown in (**b**)

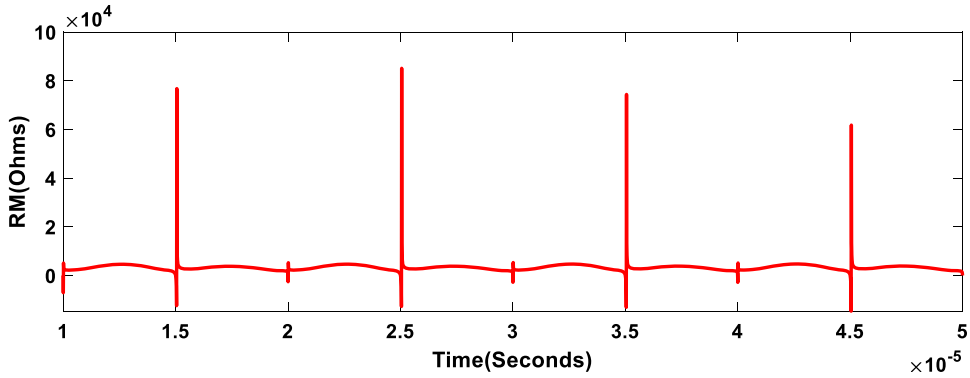

Fig. 17 Behavior of the memristance of the realized memristor plotted at 100 kHz

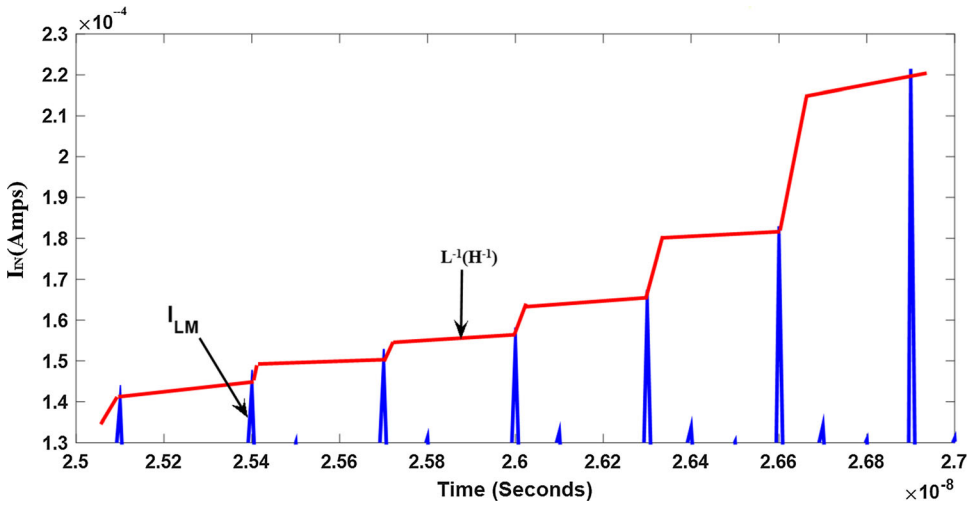

Fig. 18 Transient current response of realized meminductor element on applying pulse flux signal and deduced variation of inverse meminductacne ($L^{-1}(H^{-1})$)

in Fig. 15, it can be witnessed that area versus frequency behaviour is found to be satisfactory, which is as per the fingerprint of the memristor. The response of the input voltage and current has also been generated as shown in Fig. 16(a, b). In the current response, the zero crossing is observed only at the similar phase angles as appearing in the input voltage variation (in Fig. 16(a)), it depicts the inherent resistive nature of the realized memristor. Moreover, we have presented the transient response of the input memristance of the memristor in Fig. 17. The curve exhibits a sharp peak during a cycle of the applied signal, it may be present due to the abrupt turning of transient *v-i* contours at the extreme points (as can be observed in plots given in Figs. 12, 13 and 14). Moreover, from Fig. 17, the max. and min. value of memristance can be calculated as; 1 KΩ and 77 KΩ respectively.

The simulation result shown in Fig. 18 is generated for applying a pulse signal of peak value $V_P = 0.01$ V, $T_W = 0.01$ ns and $T_P = 0.1$ ns. It can be noted that a high period valued voltage signal applied to the emulator circuit, will result in a capacitance voltage response having spikes present periodically, which can be considered as the desired flux variation. For such flux response, the meminductor current I_{IN} has been measured as given in Fig. 18 and the nature of amplitude variations of each current spikes depicts the nature of inverse meminductance (L^{-1}) variation, which is shown through red colored staircase response. It can be understood that in the absence of current output the L^{-1} must be at hold because the current value is found to be increased in every upcoming on-duration of the input, which is confirming its non-volatility property. Similarly, the pulse signal of parameters $V_P = 0.01$ V, $T_W = 0.01$ ns and $T_P = 0.1$ ns, has been applied to the memristor to check its non-volatility. For the simulation purpose, we have configured a decremental memductor. The generated plot is shown in Fig. 19 showing the obtained current response with staircase pattern noted to show the nature of memductance (G_M).

The Figs. 20 and 21 shows the obtained Monte-Carlo plots generated for 50 iterations for both realized meminductor and memristor. These plots are generated for the selected values of simulation parameters. The Monte Carlo analysis has been used to investigate the effect of the process parameters and the mismatch between transistors. The mismatch between the transistors and various process corners such as fast and slow mode operations for NMOS

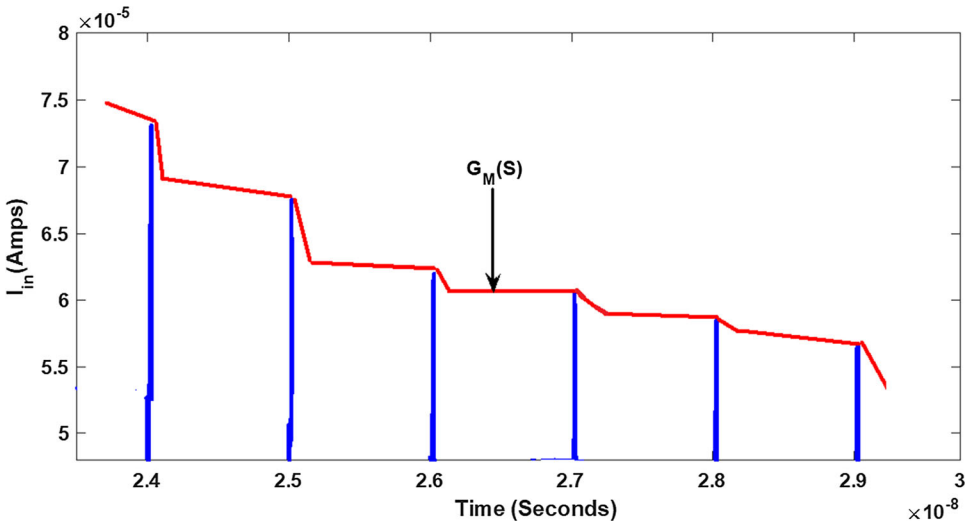

Fig. 19 Non-volatile nature of realized memristor emulator shown through current behavior and derived staircase response of memductance (G_M) on applying pulse voltage signal

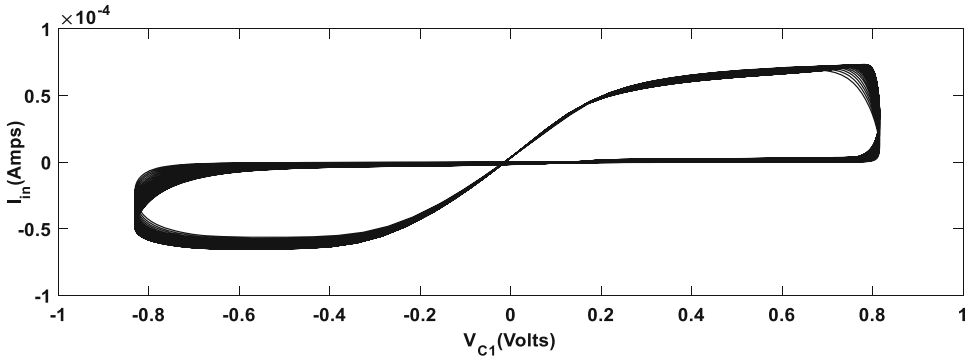

Fig. 20 Monte-Carlo simulations plots corresponding to the realized meminductor emulator

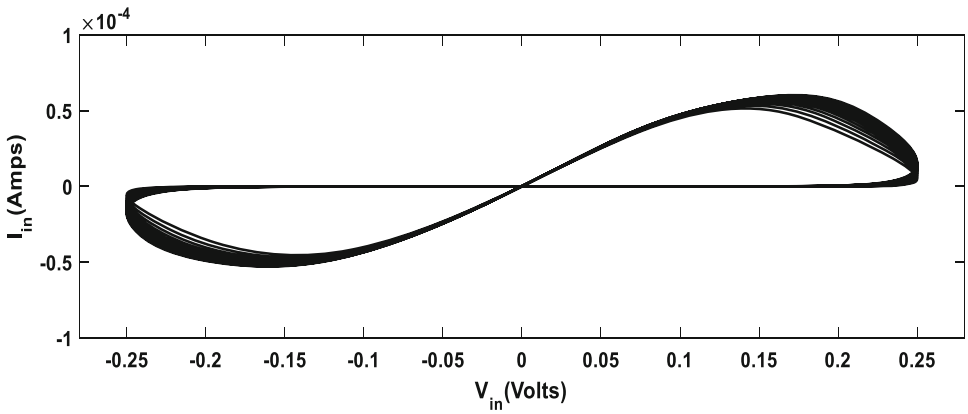

Fig. 21 Monte-Carlo simulations plots corresponding to the realized memristor emulator

and PMOS transistors were taken into account. The plots given in Figs. 20 and 21 clearly shows that the proposed floating meminductor and memristor exhibit a good performance in 50 different iterations although the hysteresis loops may be slightly altered.

To illustrate the effects of different process corners, the hysteresis loops have been generated at a temperature of 27 °C and have been shown in Figs. 22 and 23 for both the realized memelements. The three different process corners are; slow NMOS and PMOS (SS), fast NMOS and PMOS (FF), and typical NMOS and PMOS (TT).

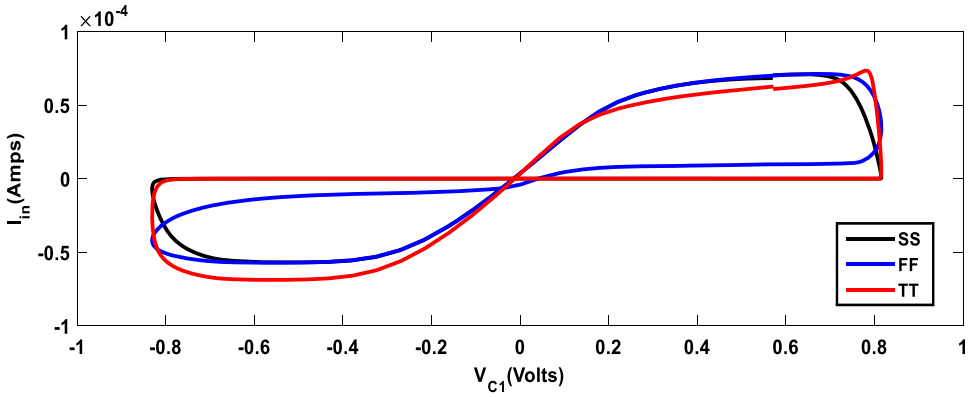

Fig. 22 PHL plots of the realized meminductor emulator for different process parameters

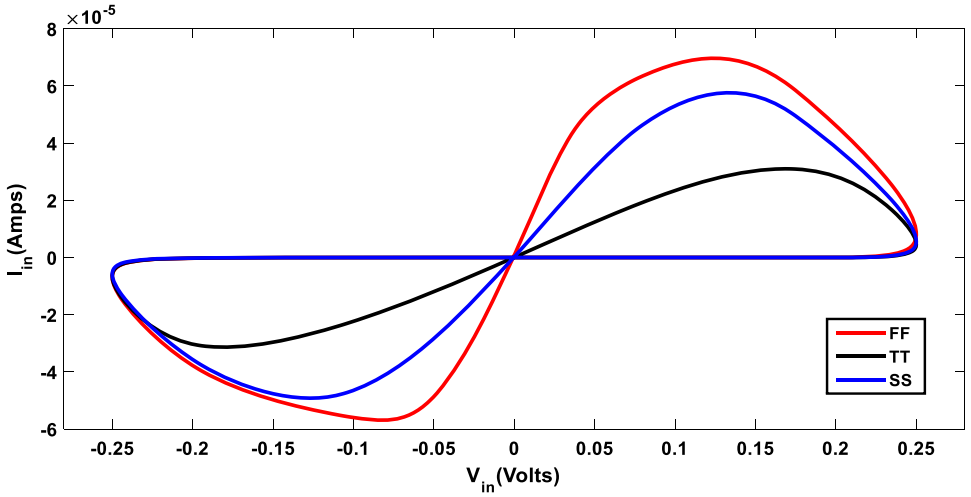

Fig. 23 Transient *v-i* curves of the realized memristor emulator for different process parameters

5 Application examples

The functioning of the reported emulator configuration can also be exhibited by employment of the realized memelements in the application examples, which have been illustrated in the following section.

5.1 Meminductor based neuromorphic circuit for mimicking amoeba behaviour

The use of memristor in neural applications has been a popular research interest in the last decade. Due to the unique nature of memristors of resistance variability with respect to applied excitation, it has been used in modelling of natural neurons and unicellular species. Like in [58], a passive element-based circuit configuration has been proposed to demonstrate the amoeba action. Using similar approach, this circuit can also be implemented by employing other memelements [59]. This discussed circuit in [59] has been depicted in Fig. 24, based on the floating meminductor emulator developed using MVDCC. This circuit generates the response of Amoeba exhibited during the temperature change takes place around it. The amoeba shows a change in its locomotive speed whenever there is any change in its surrounding temperature. This process of slowing down the speed takes a certain time in which temperature drops multiple times in that period, after which the movement seems to become slow. But, due to this unique nature of learning found in the amoeba, from the next time the speed starts to slow down immediately just after the temperature drop.

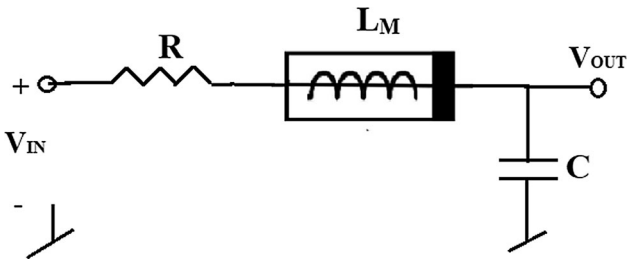

Fig. 24 Meminductor based neuromorphic circuit for simulating amoeba behaviour with passive element values taken as C_1 = 0.2 nF, C_2 = 0.05 nF, R_2 = 5 K, R = 15 K and C = 0.9 nF

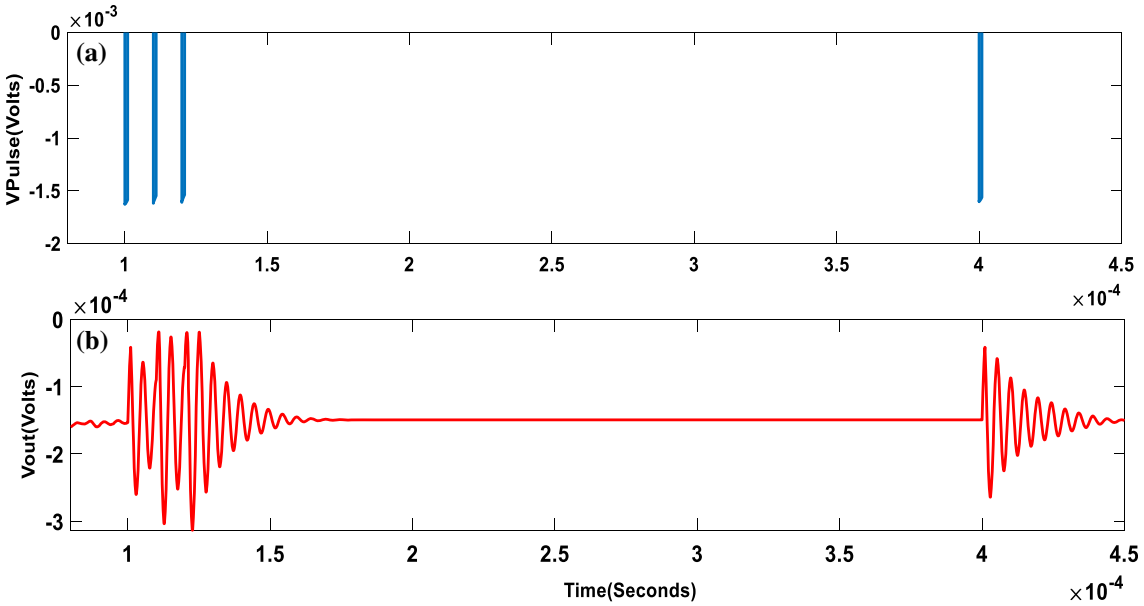

Fig. 25 Response of the voltage V_{out} (**b**) for the input V_{IN} applied as pulse excitations (**a**) to the circuit shown in Fig. 16 with parameters value chosen as; peak value as V_m = 10 mv and pulse width as T_W = 10 µs

In Fig. 25, the input $v_{in}(t)$ of the developed circuit represents the temperature change in the close environment, while the $v_{out}(t)$ represents the variation in the locomotive speed of the amoeba. And the simulation results for the $v_{out}(t)$ is shown in Fig. 25(b) with the input voltage $v_{in}(t)$ taken as pulse signal ($V_{p(t)}$ in Fig. 25(a). It can be observed from the output $v_{out}(t)$ that for the occurrences of multiple pulses, the output first grows then oscillations go down gradually, but for the single pulse arriving after some time, the output seems to suddenly increases but slows down instantly, so, it is confirming that the presented circuit is validating the amoeba behavior.

5.2 Proposed memristor emulator based associative learning demonstration

Next, we have shown the application example of the realized memristor element. The proposed memristor has been used to model the behaviour of a synapse architecture, which are the basic elements of any neural related applications. The synapse behaves as a communication link between two neurons and its response is decided by the signal received from the pre-synaptic neuron and signal transmitted to the post-synaptic neuron. The function of the memristor element also matches with such kind of behaviour and it has also been depicted in several works [58].

The synapse like behaviour of the memristor can be validated through a popular example of Pavlov learning experiment of associative learning. Pavlov showed this behaviour exhibited by a dog, when he periodically showed the food to the dog along with the ringing of the bell. Firstly, he gave the food to the dog and rang the bell at the same time, then he used to ring the bell only and observed that dog started to salivate even when the food is not served. He called this behaviour as the associative learning. The corresponding Op-amp based circuit is represented in Fig. 26(a), which can be used to mimic this behaviour through its two pulse voltage inputs V_{NS} and V_{UCS} and output voltage V_{out}.

We have applied pulse input voltages V_{NS} and V_{UCS} to this op-amp based circuit shown in Fig. 26(a), which consists of multiple pulse excitations having dissimilar time delays. The simulated transient response of voltages V_{NS} and V_{UCS} has been shown in Fig. 26(b) followed by the generated pulse output response. In the first phase, which is the duration before the learning, we have applied V_{NS} and V_{UCS} pulse input at different instants, and it can be noticed from the output that the circuit only responds to the V_{NS} input in this phase. In the second phase, both inputs have been applied simultaneously and output is produced. Now interestingly, when the two pulse excitations (V_{NS} and V_{UCS}) are given at different time instants, the output is generated for both the input pulses. This nature of the circuit is confirming its ability of associative learning.

6 Experimental results

The section presents experimental results of the proposed memelement emulator implemented using commercially available ICs; LM13700, AD844 and µA741. For the

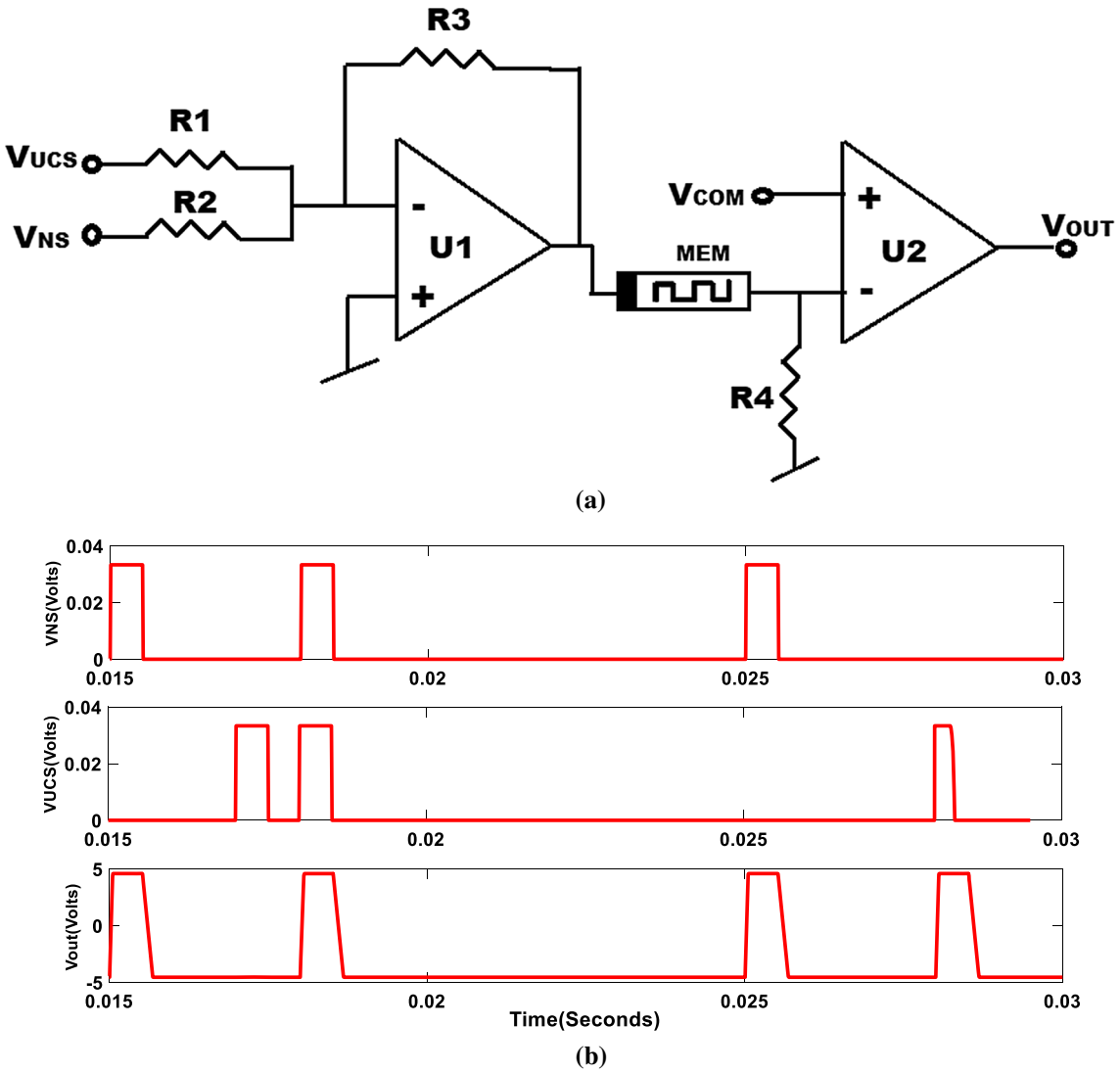

Fig. 26 **a** Proposed memristor based circuit for exhibiting associative learning ability. Where, R1 = 30 kΩ, R2 = 200 kΩ, R3 = 40 kΩ, R4 = 1 GΩ, V_{COM} = − 5 mV. **b** Simulation results of the developed circuit shown in (**a**)

implementation of the proposed circuit (in Fig. 4), we need to obtain the function of MVDCC and OTA using these ICs. The MVDCC is made up of a dual-output input transconductance stage and a second-generation current conveyor. Both of these stages can be replaced by the ICs LM13700 and AD844 respectively. As both current outputs of MVDCC (I_{Z+} and I_{Z-}) are used in the circuit, we need to use two single output transconductance amplifiers. Fortunately, the LM13700 IC consists of two transconductance amplifiers. Moreover, the µA741 is also required to obtain the relationship between X, Z+ and Z− ports' voltages, which is ($V_X = V_{Z+} - V_{Z-}$) for MVDCC. Furthermore, one more LM13700 IC needed to realize the function of OTA used in the proposed circuit. Therefore, the complete schematic diagram of the MVDCC-OTA based emulator circuit using two LM13700 ICs, a µA741 and an AD844 IC, is shown in Fig. 27 for both realized meminductor as well as the memristor. In the circuit, Z_1, R_2 and C_2 are corresponding to the passive elements used in the proposed emulator, and the resistances R_5 are R_4 are needed for the biasing of two LM13700 ICs respectively. The resistance R_3 is connected just to pass the current of AD844 output to ground as it has no active use in the circuit. The resistances R_6, R_7, R_8 and R_9 are the integral part to design a voltage subtractor using Op-Amp IC.

From the presented circuit shown in Fig. 27, we can observe that differential input voltages at the input terminal of the emulator circuit, V_1 and V_2, are applied at the buffer inputs, therefore buffer outputs are obtained as;

$$V_{\text{Buffup}} = V_1 \tag{19}$$

$$V_{\text{Bufflow}} = V_2 \tag{20}$$

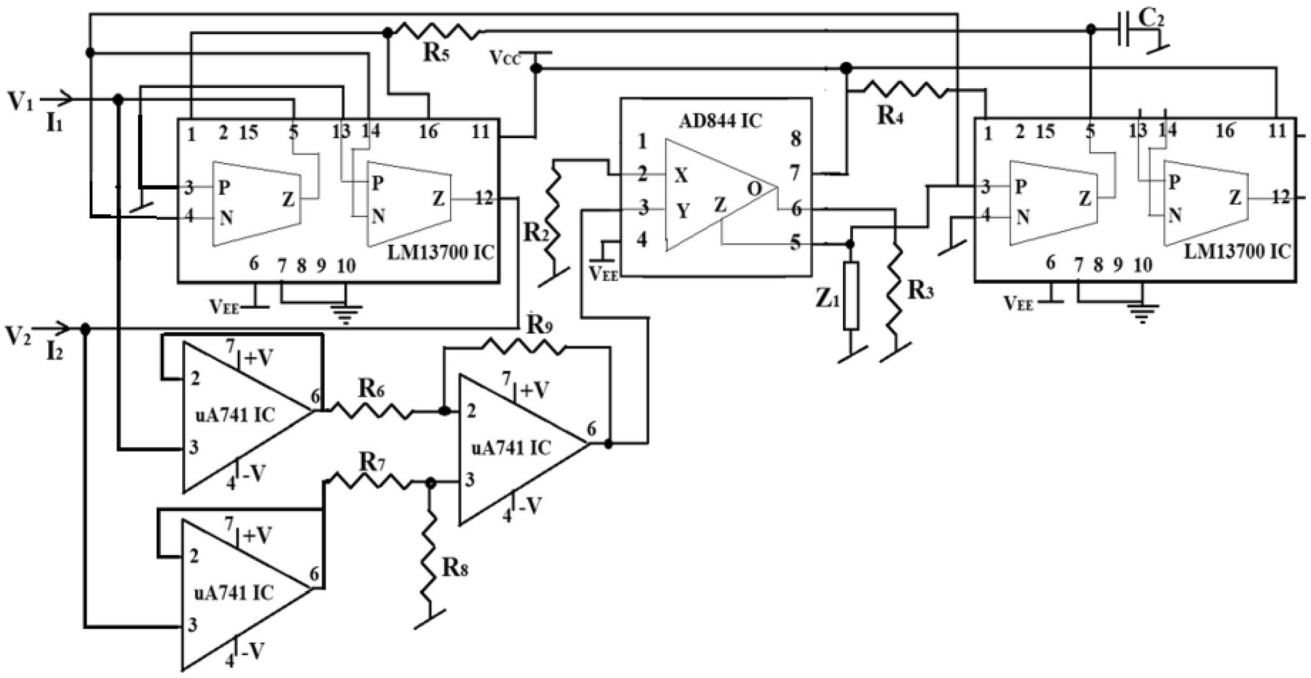

Fig. 27 Schematic diagram of commercial IC based implementation of discussed MVDCC-OTA based memelement emulator with power supply voltage taken as $V_{CC,EE} = \pm$ 20 V and V = ± 15 V

Now, these voltages appear at the input of subtractor through resistance R6 and R7. If, the resistances value as chosen as $R_6 = R_7 = R_8 = R9$, then subtractor output is obtained as;

$$V_{\text{Subout}} = V_2 - V_1 \tag{21}$$

Now, this voltage (given in Eq. 21) is applied at the 3rd pin (Y port) of the AD844 IC and for AD844, we know,

$$V_X = V_Y (= V_{\text{Subout}}) \tag{22}$$

Hence, potential at the Pin 2 (X port) of AD844 IC is found as;

$$V_X = V_2 - V_1 \tag{23}$$

The resistance R_2 is connected at the X port, therefore, current through R2,

$$I_{R2=}I_X = \frac{V_2 - V_1}{R_2} \tag{24}$$

For AD844 IC the $I_X = I_Z$, therefore, the current flowing out of the Pin no. 5 will be,

$$I_Z = I_X = \frac{V_2 - V_1}{R_2} \tag{25}$$

Hence, voltage V_{Z1} will be equals to,

$$V_{Z1} = \frac{V_2 - V_1}{R_2} Z_1 \tag{26}$$

This voltage V_{Z1} is applied at the transconductance stage of LM13700, whose output is taken across the capacitor C_2, hence, the voltage V_{C2} will be,

$$V_{C2} = G \frac{V_2 - V_1}{sC_2R_2} Z_1 \tag{27}$$

where G is the transconductance gain of the LM13700 IC.

Now, this voltage V_{C2} is applied for the biasing purpose of both the transconductance stages of another LM13700 IC. So, transconductance of the both stages will be modified and become function of V_{C2} voltage. For first LM13700, the transconductance gain (G') in terms of biasing voltage is given as;

$$G' = kV_{C2} = kG \frac{V_2 - V_1}{sC_2R_2} Z_1 \tag{28}$$

where k is constant, depends upon the LM13700 parameter.

So, as per the circuit configuration, the input currents I_1 and I_2 (which are fed to the outputs of LM13700) will be;

$$I_1 = G' V_{Z1} = \left(kG \frac{V_2 - V_1}{sC_2R_2} Z_1 \right) \frac{V_2 - V_1}{R_2} Z_1 \tag{29}$$

and

$$I_2 = -G' V_{Z1} = \left(kG \frac{V_2 - V_1}{sC_2R_2} Z_1 \right) \frac{V_1 - V_2}{R_2} Z_1 \tag{30}$$

From Eqs. 29 and 30, we can observe that this circuit shown in Fig. 28, realizes a memelement emulator based on LM13700 and AD844. For choosing Z_1 as C_1 and as R_1,

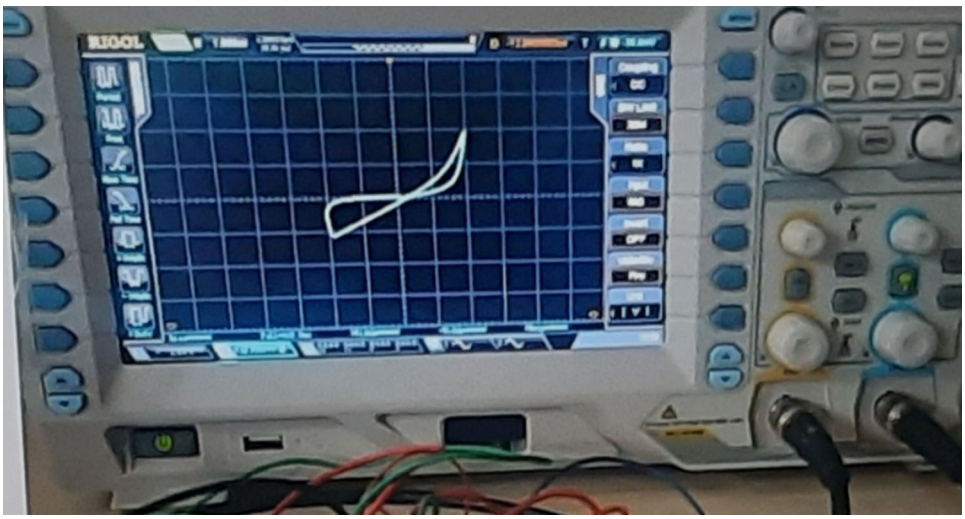

Fig. 28 ϕ-i curves (V_{C1} is proportional to flux ϕ) of the realized meminductor generated on the DSO screen

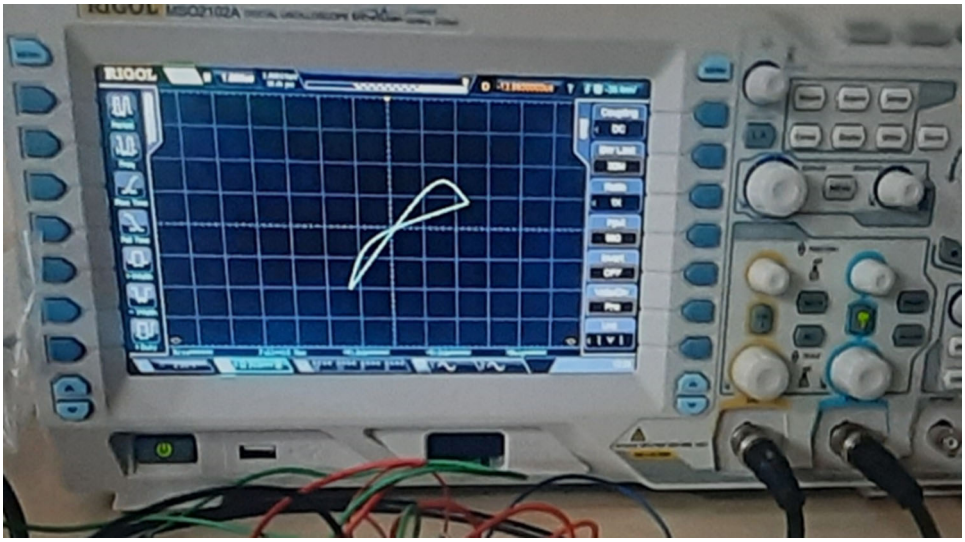

Fig. 29 Obtained transient v-i response of the memristor displayed on the DSO screen

the depicted circuit emulate the behavior of a meminductor and memristor respectively.

The experimental verification of the developed emulators has been performed and results have been discussed in Figs. 28 and 29.

For the validation of the meminductor emulator, the parameters values are chosen as; C_1 = 1 pF, R2 = 1.8 K, R3 = 15 K and R5 = 25 K, R6 = R7 = R8 = R9 = 1 K and C2 = 4.7 nF with maximum *i/p* voltage value as V_{P-} = 0.008 V at a frequency of 7.5 kHz. Now, to obtain the ϕ–i curves, here also, the voltage across the capacitor C_2 is chosen, whose potential is proportional to the flux of input voltage and plot has been traced between input current and capacitor voltage. The result can be displayed on the CRO screen, which is shown in Fig. 28.

Similarly, to investigate the implemented memristor emulator, the parameters values are chosen as; R_1 = 100 K, R_2 = 10 K, R_3 = 20 K, R_4 = 24 K, R_4 = 20 K, R6 = R7 = R8 = R9 = 1 K and C_2 = 4.7 nF with applying peak input value of V_P = 0.35 V at 10 kHz. The generated Lissajous pattern for the memristor is displayed on the CRO screen and presented in Fig. 29.

7 Conclusion

The behavior of a flux-controlled and voltage-controlled meminductor and memristor element has been realized in this work. The architecture used for the realization of these two memelements is developed by using an MVDCC and an OTA. The MVDCC active element is based on thirty CMOS transistors and nine transistors are needed for OTA and hence, the developed memelement emulator employs only thirty transistors. Additionally, from the perspective of monolithic integration, the use of grounded elements employed in the circuit adds to the preferability of the

developed circuit. The analysis has also been presented for taking non-ideal gains of used ABBs and parasitic ports into account. The discussed PSPICE generated simulation results clearly depicted that hysteresis behavior observed in the transient contour curves of the realized memelements can be tuned through the use of employed passive elements and through variation of the biasing voltage as well. The functioning of the both realized elements has also been verified for the neural related applications based on the proposed emulator. And finally, we have depicted the commercial ICs based implementation of suggested emulator circuit and experimental results are demonstrated (shown in Figs. 28 and 29), confirming its operability as the meminductor and as a memristor element.

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Data availability Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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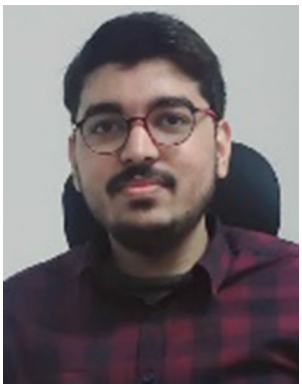

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