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A deterministic digital calibration technique for pipelined ADCs using a non-nested algorithm

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Abstract

This paper proposes a novel deterministic technique to digitally calibrate 1.5-bits/stage and 1-bit/stage pipelined as well as algorithmic analog-to-digital converters (ADCs). The technique accounts for mismatches between the sampling and feedback capacitors, comparator offsets and charge injection. Compared to other existing deterministic calibration techniques, this technique is characterized by its simplicity, minimal hardware and low power dissipation. The technique is demonstrated on a 1.5-bits/stage, 10-stage pipelined ADC, in a 180-nm CMOS technology. For 5% mismatches in the capacitances in the 3 most significant bit stages, there was a significant reduction in the integral nonlinearity in both pipelined and algorithmic ADCs after calibration; Signal-to-noise ratio improved by 10dB and spurious-free dynamic range improved by 15dB in the pipelined ADC.

Keywords Pipelined ADC · Algorithmic ADC · Integral non-linearity (INL) · Capacitor mismatch · Digital calibration

1 Introduction

Pipelined analog-to-digital converters (ADCs) form an integral part of many communication and other electronic systems. Their accuracy and linearity is limited by non-idealities such as capacitance mismatches, comparator offsets, charge injection and finite op-amp gain. A widely used method to improve the accuracy of an ADC is to use calibration. Calibration techniques for ADCs can be broadly divided into three categories: Deterministic [1–3], Statistical [4–7] and Analog [8–10]. The technique described in this paper is a deterministic technique. Deterministic techniques measure the errors caused by non-idealities by comparing the actual digital outputs of the ADC with an ideal mathematical model, for known analog inputs. This error is then added to/subtracted from the digital output of the ADC during normal operation, thus correcting for the error, and making the ADC output linear. Deterministic techniques require very little hardware and memory, consume less power. Their calibration is also faster as compared to statistical calibration techniques. Many deterministic calibration techniques have been reported in literature [1–3]. Karanicolas et al. [1] proposed a technique for 1 bit/stage ADCs which is very simple to implement, uses simple hardware and needs very little memory to store digital calibration coefficients. The algorithm works as follows: To calibrate the *n*th stage, first the analog input to that stage and the digital output of the stage are forced to 0. The residue output of the stage (say R1) is digitized by an ideal backend ADC. While keeping the analog input of the stage at 0, the digital output of the stage is forced to 1. From the digitized residue output (say R2), R1 is subtracted, and this gives the digital correction code of the *n*th stage. Digital correction codes for all required stages are calculated similarly. These digital calibration codes are added to/subtracted from the raw ADC output to obtain a calibrated digital output. The limitations of this algorithm are: the gain of the first few (i.e. MSB) stages are intentionally reduced to <2 to avoid saturation of the

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subsequent stages in order to avoid missing decision levels. But this lowers the resolution of the ADC. The calculation of digital calibration coefficients is done in a nested manner starting from LSB to MSB of the stages to be calibrated. Sahoo and Razavi [2] described a calibration technique for a pipelined ADC that had a 4-bit resolution in the first stage, 1.5-bit resolution in the next 7 stages and 2 bits in the last stage. Digital calibration was carried out to account for capacitor mismatch error and gain mismatch error in the first stage and only capacitor mismatch errors in the next 4 stages. The technique requires generation of some precise analog voltages and hardware for digital multiplication and division. Chuang and Sculley [3] describe a digital calibration technique for 1.5 bits/stage ADC similar to Karanicolas et al. [1] with stage gain > 2. A stage gain of > 2 saturates the output when the inputs are close to the rail, thus decreasing the input dynamic range. This technique uses simple hardware and very little memory for implementation. Statistical techniques are superior for calibrating ADCs in lower geometry technology nodes where the process-dependent errors are larger. But these techniques require a large amount of hardware and hence dissipate more power. They also require a larger number of clock cycles for calibration. Analog calibration techniques [9–11] are more prone to errors since they need trimming of capacitors to adjust the gain. They also require more clock cycles compared to digital techniques.

In this paper, a novel digital calibration technique is proposed. The advantages of the proposed technique are as follows: The pipeline hardware is neither interrupted nor externally controlled during calibration; the technique can handle both missing codes and missing decision levels (i.e. amplifier gains <2 as well as > 2), and it can be applied to calibrate pipelined as well as algorithmic ADCs. The paper is divided into 4 sections. Section 2 describes the proposed calibration technique. Section 3 describes the circuit implementation and simulation results, and Sect. 4 concludes the paper.

2 Proposed calibration technique

To illustrate the technique, a 1.5-bits per stage, 10-stage fully-differential pipelined ADC is considered, of which the first 3 stages are calibrated, and stages 4–10 are assumed to be ideal [1]. The input analog voltage is assumed to have the range -1.2 to 1.2 V. Nominally, the amplifier gain of every stage is designed to be 2. But due to capacitance mismatch, the gain of a stage may be lower or higher. The former leads to missing codes, and the latter leads to missing decision levels [20]. Unfortunately, deterministic calibration techniques, such as the one proposed in this paper, cannot correct for missing decision levels (gains > 2) [1]; they can correct only for missing codes (gains < 2). Therefore the technique proposed here performs calibration in two steps. In the first step, it is determined if the gain of each stage to be calibrated is less than or > 2. If it is > 2, then the circuit of the amplifier is modified so as to make the gain <2. To first determine the gains, a finely incremented ramp voltage is input to the ADC from 0 to $\frac{V_{ref}}{4}$. As the input voltage is ramped up, when the Nth output code changes from 0 to $+1$, an increased gain of the Nth stage amplifier causes a negative jump in the output characteristics and a decreased gain causes a positive jump [3]. This is illustrated in Fig. 1a, b, respectively, for a gain error in the first stage (due to capacitance mismatch) and an ideal back-end ADC. If the gain of a particular stage is > 2, then the capacitors in the multiplying digital-to-analog converter (MX2) of that stage are swapped, so that the stage gain becomes <2. This is done as shown in Fig. 2, which shows a modified MX2 circuit that enables the swapping of capacitors.

A conventional MX2 circuit (for a gain of 2) will not have the switches marked with a $\overline{swap}$ clock signal, and its gain will be $(1 + \frac{C2}{C1})$, with C1 = C2 in the ideal case. If due to capacitance mismatch, C2 > C1, then this gain will be > 2. In such a case, in the circuit of Fig. 2, the clock signal $\overline{\phi 1 \cdot \text{swap}}$ is made high, rather than the signal $\phi 1 \cdot \text{swap}$. This causes the gain to be $(1 + \frac{C1}{C2})$, which becomes <2 [3]. Once this is done for all the stages that are to be calibrated, each of them will have a gain <2, and the digital calibration technique described below can then be applied. This process of swapping the capacitors eliminates the need for intentionally forcing the gain of each stage to be <2 by design, as was done in [1]. The latter caused a reduction in the resolution of the ADC, which the present technique does not suffer from. Note that only the stages that are to be calibrated need to have the modified MX2 circuit of Fig. 2. The rest of the stages will have the conventional MX2 circuit.

We now discuss the second step of the proposed calibration algorithm. For the 1.5-bits per stage architecture being considered, the output voltage (V_{out}) of the MX2 stage (assuming that the op-amp open-loop gain is large) is given by [3],

$$V_{out} = (1 + \beta) \cdot V_{in} - B \cdot V_{ref} \cdot \beta \tag{1}$$

where $B = 1$ if $V_{in} > \frac{V_{ref}}{4}$, B = -1 if $V_{in} < -\frac{V_{ref}}{4}$ and $B = 0$ otherwise, V_{ref} is the reference voltage, and β is the ratio of sampling capacitance to feedback capacitance.

Let $\beta 1$, $\beta 2$ and $\beta 3$ be the capacitance ratios of stage1, stage2 and stage3 respectively. With each of these three stages having a gain less than or equal to 2, a capacitance mismatch will cause an upward jump in the transfer characteristics. The goal now is to determine the height of each

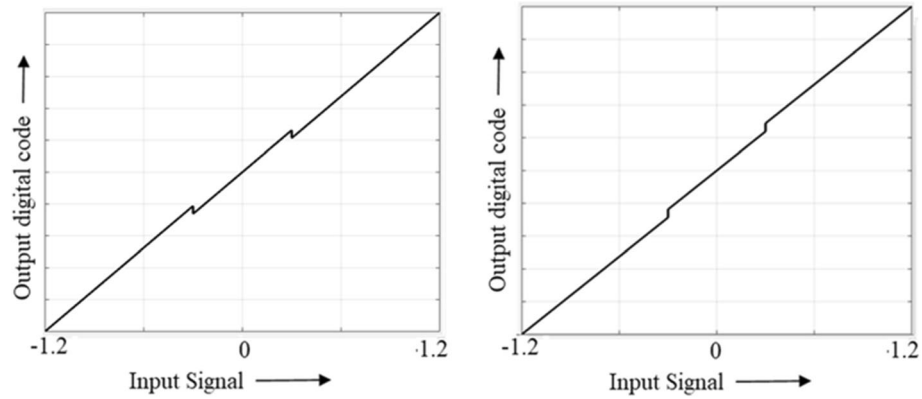

Fig. 1 1.5 bits/stage ADC output characteristics with first stage gain **a** >2, and **b** <2

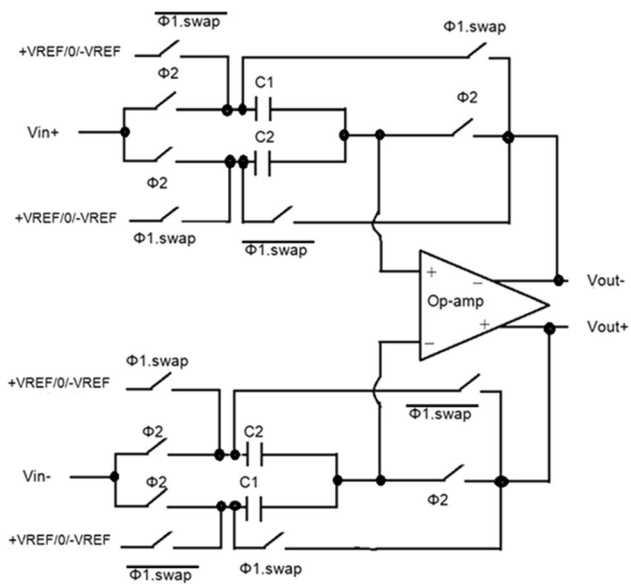

Fig. 2 MX2 stage of the Pipelined ADC of the stages that require calibration

jump, and then correct it in the digital output of the ADC. We begin by noting that a gain error in the *N*th stage causes a jump in the output characteristics when the *N*th output digital code changes from -1 to 0 or from 0 to $+1$. This is shown in Fig. 3 for capacitance mismatches in the first three MSB stages, where a capacitance mismatch of 10% is assumed for each of these stages. Note that as the digital output traverses from all -1's to all $+1$'s, the MSB stage causes 2 jumps in the transfer characteristics (indicated by triangles in Fig. 3), the second MSB causes 6 jumps (shown by rectangles in Fig. 3), and the third MSB causes 14 jumps (shown by circles in Fig. 3), so that there are a total 23 segments in the characteristics.

The jumps caused by a particular stage have the same height, because this height is a function of only the capacitance mismatch of that stage. Thus only one jump per stage needs to be measured. Let S1, S2 and S3 be the heights of the jumps due to stages 1, 2 and 3 respectively. We calculate S3 for an analog input of around 75mV ($\approx \frac{V_{ref}}{16}$), which corresponds to an input to the 3rd stage of 300mV ($=\frac{V_{ref}}{4}$). At this voltage, the 3rd MSB changes from 0 to $+1$. The analog equivalent ($V_{3,1}$) of the ADC digital output when the input to stage3 is $\frac{V_{ref}}{4}$ and the 3rd MSB is $+1$ is given by [1],

$$V_{3,1} = \frac{V_{ref}}{8} + \frac{(1+\beta 3)\cdot\frac{V_{ref}}{4} - \beta 3 \cdot V_{ref}}{8} \tag{2}$$

Similarly, the analog equivalent ($V_{3,0}$) of the ADC digital output when the input to stage3 is $\frac{V_{ref}}{4}$ and the 3rd MSB is 0 is given by,

$$V_{3,0} = \frac{(1+\beta 3)\cdot\frac{V_{ref}}{4}}{8} \tag{3}$$

Thus, the analog equivalent of the jump in the output when the 3rd MSB transitions from $+1$ to 0, is given by,

$$S3, analog = V_{3,1} - V_{3,0} = \frac{V_{ref}}{8} - \frac{\beta 3 \cdot V_{ref}}{8} \tag{4}$$

Note that ideally, $\beta 3 = 1$, and then S3, analog = 0V, which is as expected. Similarly, the jump due to the 2nd MSB is determined at analog input of around 150 mV, and can be written as S2, analog = $\frac{V_{ref}}{4} - \frac{\beta 2 \cdot V_{ref}}{4}$, and the jump due to the MSB is determined at 300 mV, and can be written as, S1, analog = $\frac{V_{ref}}{2} - \frac{\beta 1 \cdot V_{ref}}{2}$. During calibration, the hardware required for digital computations consist of a few comparators and adder/subtractor. Hardware complexity is highly reduced since no division and multiplication operations are necessary. Calibration mode ends when the calibration coefficients for all the stages to be calibrated are calculated.

Having determined the jumps (S1, S2 and S3), we now use them to perform correction in the digital output of the ADC (cf. Fig. 3). The goal of the correction algorithm is to obtain a smooth straight line [1, 3]. To achieve this, any of the 23 segments in Fig. 3 is taken as a reference segment, and for all other segments an appropriate linear

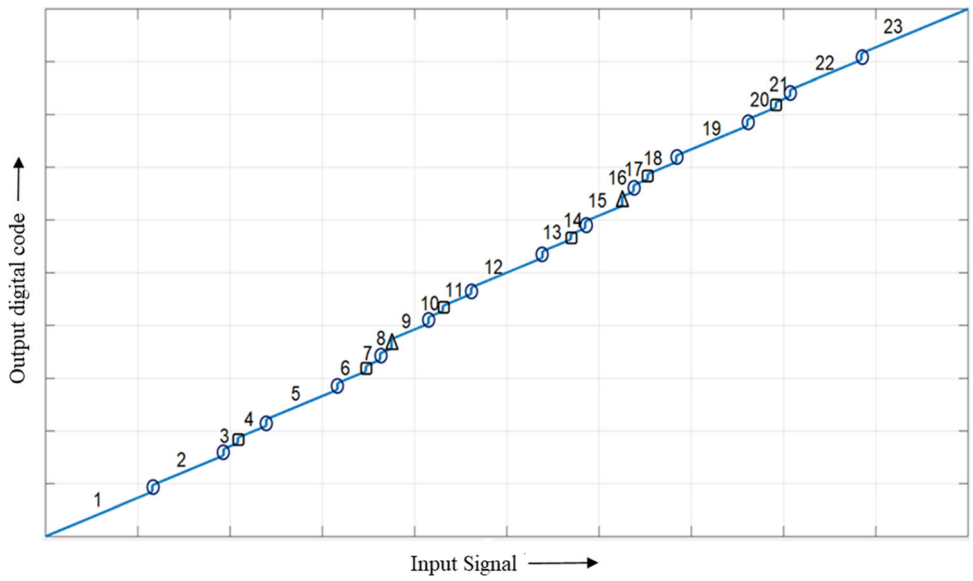

Fig. 3 Output characteristics of ADC for the capacitor mismatch in 3 MSB stages

combination of S1, S2 and S3 is added/subtracted to eliminate the jumps. We choose segment 12 as the reference, as this requires the minimum hardware for error correction. Starting with segment 12, segments 11 and 13 encounter jumps due to the capacitance mismatch of the 3rd MSB stage. So S3 is added to the digital codes belonging to segment 11 and subtracted from the digital codes of segment 13, to align them with segment 12. Similarly (S3 + S2) is added to the digital codes of segment 10 and subtracted from the digital codes of segment 14, and so on. The complete set of corrections is shown in Table 1. With these corrections, all the jumps due to capacitor mismatches are eliminated and the output characteristic of the ADC is made linear.

A bird's eye view of the calibration algorithm for the capacitance mismatch in the first stage is shown in Fig. 4.

Figure 4a shows the output characteristics of the ADC for a first stage gain > 2. Figure 4b shows the output characteristics for a first stage gain < 2, after the sampling capacitor and feedback capacitors are swapped. The calibration coefficients are calculated by subtracting x1 from x as shown in Fig. 4b. Figure 4c shows a graph of the calibrated output digital code of the ADC after adding/subtracting the calibration coefficients from the raw code of the ADC. The calibration algorithm improves the linearity of the ADC, but it results in missing codes (y − y1) near the rails.

The proposed algorithm can also be used to calibrate 1 bit/stage pipelined ADCs, as well as algorithmic ADCs. For algorithmic ADCs, which is a single 1-bit pipelined stage used in a cyclic fashion, there is only one stage, and only one MX2 circuit, and therefore only a single-step calibration is necessary. The procedure for calibration is as follows: force the input voltage to 0 V and the first digital output bit to 1. Then, let the algorithmic ADC calculate the rest of the bits. At the end of (N − 1) cycles, the (N − 1) bits are output. Let the N-bit output (with MSB = 1) be called R1. Find the complement of R1 (say R1'). Then (R1 − R1') is the digital calibration code equivalent to S1 of

Table 1 Correction magnitudes for each of the segments of Fig. 3

Segment	D1	D2	D3	Correction
1	00	00	00	$S1*1+S2*3+S3*7$
2	00	00	01	$S1*1+S2*3+S3*6$
3	00	00	10	$S1*1+S2*3+S3*5$
4	00	01	00	$S1*1+S2*2+S3*5$
5	00	01	01	$S1*1+S2*2+S3*4$
6	00	01	10	$S1*1+S2*2+S3*3$
7	00	10	00	$S1*1+S2*1+S3*3$
8	00	10	01	$S1*1+S2*1+S3*2$
9	01	00	01	$S2*1+S3*2$
10	01	00	10	$S2*1+S3*1$
11	01	01	00	$S3*1$
12	01	01	01	0
13	01	01	10	$-(S3*1)$
14	01	10	00	$-(S2*1+S3*1)$
15	01	10	01	$-(S2*1+S3*2)$
16	10	00	01	$-(S1*1+S2*1+S3*2)$
17	10	00	10	$-(S1*1+S2*1+S3*3)$
18	10	01	00	$-(S1*1+S2*2+S3*3)$
19	10	01	01	$-(S1*1+S2*2+S3*4)$
20	10	01	10	$-(S1*1+S2*2+S3*5)$
21	10	10	00	$-(S1*1+S2*3+S3*5)$
22	10	10	01	$-(S1*1+S2*3+S3*6)$
23	10	10	10	$-(S1*1+S2*3+S3*7)$

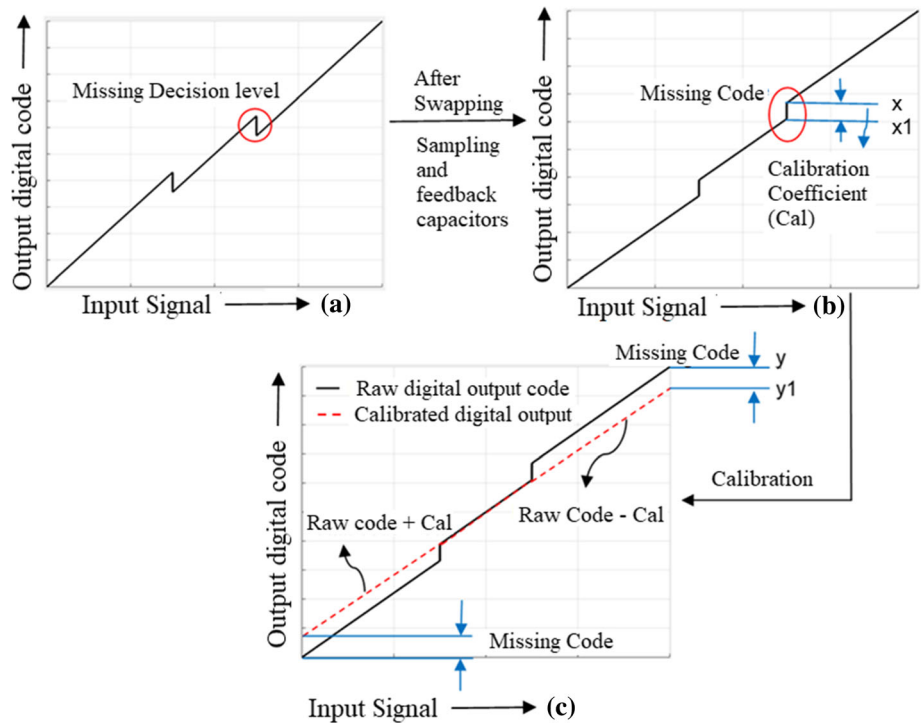

Fig. 4 Bird's eye view of the calibration algorithm to calibrate the first stage

the pipelined ADC. Similarly, let R2 be the first, i.e. most significant, (N − 1) bits of R1, and let R2' be the complement of R2. Then (R2 − R2') gives the digital calibration code equivalent to S2 of the pipelined ADC. This process is repeated for as many bits as is desired. The higher the number of bits calibrated, the better is the INL, but the lower is the resolution [1].

The flowchart to calculate the calibration coefficients of the 'N' MSB stages to be calibrated is as shown in Fig. 5.

During normal operation of the ADC, correction magnitudes calculated as discussed earlier in this section, are added/subtracted from the raw code to get the calibrated digital output. The algorithm can also be applied to calibrate a 1.5 bits/stage algorithmic ADC with the input voltage forced to $\frac{V_{ref}}{4}$ and first digital output bit forced to +1.

3 Implementation and simulation results

3.1 Implementation

The circuit was implemented in Semiconductor Complex Limited, India (SCL)'s 180-nm CMOS technology, and was simulated in Cadence-AMS environment with the calibration portion coded in Verilog HDL. As mentioned in Sec.2, a 1.5 bits/stage, 10-stage pipelined ADC was implemented as a test case. The 1.5-bit flash ADC in each stage was designed with Strong-ARM latch comparators [18]. The reference voltages ($\pm\frac{V_{ref}}{4}$) for the comparator were generated using switched-capacitor voltage divider circuit [19]. The circuit of the multiply-by-2 DAC (MX2) was discussed in Sec.2 (see Fig. 2). The op-amp in the MX2 was a two-stage op-amp with a telescopic cascode first-stage followed by a push pull common source stage, and common-mode feedback for each stage. The op-amp was designed to provide a gain of 87dB, a unity-gain frequency of 500 MHz, and a phase margin of 56° over all process corners. Thermal noise of the op-amp is measured to be approximately equal to $\frac{LSB}{4}$ [12].

The hardware required for calibration consisted of the digital block needed to calculate the correction codes of Table 1, and a circuit to generate a very accurate ramp voltage. The block level representation of the calibration algorithm that calculates the calibration coefficients of the first MX2 stage is shown in Fig. 6. This circuit was used for all the stages that were calibrated.

In Fig. 6, the input *D [9:0]* represents the 10 raw digital output codes from the ADC before calibration. It is known that the digital output code from each MX2 stage can take a value of +1, 0 or −1 [cf. Eq. (1)] which is digitally represented using 2 bits. The MX2 digital output code '+1' is represented by the digital bits '10', '0' is '01' and '−1' by '00'. The input bit $MX2_1_MSB$ represents the MSB of the first MX2 stage which takes a value of '0' if the digital output code of the MX2 stage is '0' or '−1', and takes a value of '1' if the digital output code of the MX2 stage is '+1'. The bit $\overline{MX2_1_MSB}$ is a complement of

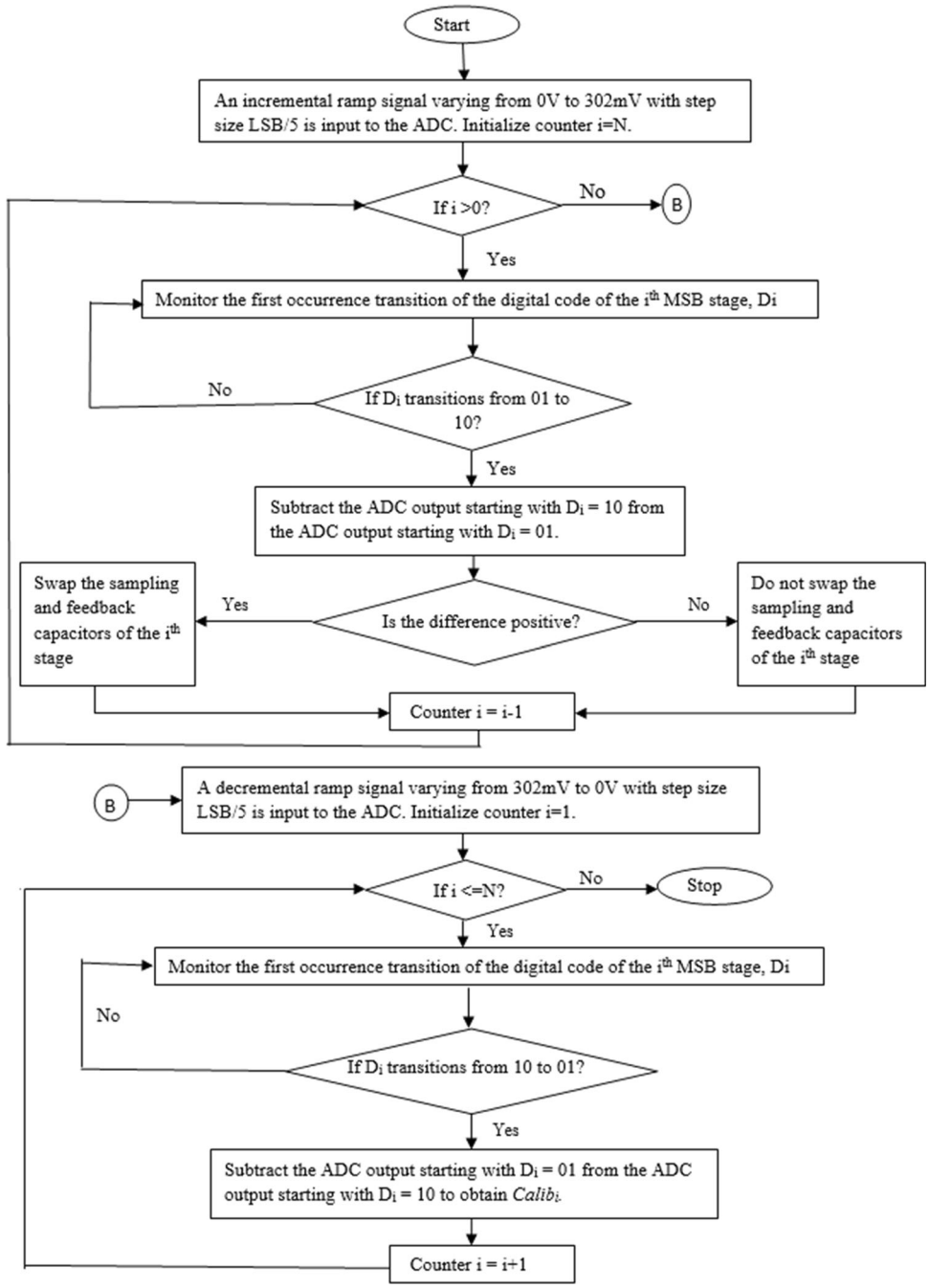

Fig. 5 Flowchart to calculate the calibration coefficients

*MX*2_1_*MSB*. The signal *Up_Down*, if set to '1', indicates that the input signal is ramping up (to swap the sampling and feedback capacitors if the stage gain is > 2), else the signal is set to 0 when the input signal ramps down (to calculate the calibration co-efficients). The output signals *Swap* and *Calibration Coefficient* are latched once during the calibration cycle. The former is latched when the input *MX*2_1_*MSB* changes from 0 to 1 during input signal ramp-up and the latter is latched when the bit *MX*2_1_*MSB* changes from 1 to 0 during ramp-down. Any further modification to the output signals are prevented by setting the flag bit to low (initially set to high) after the output signals are latched once. During the calibration phase, with input signal ramp-up (*Up_Down* = 1, flag = 1), when *MX*2_1_*MSB* bit changes from 0 to 1, the corresponding ADC output *D [9:0]*, is subtracted from the delayed ADC output *D1 [9:0]*. If the subtraction operation sets the *Borrow* bit low, indicating a stage gain > 2, then, *swap* signal is set high, else *swap* signal is set low indicating that the stage gain is < 2. At this point, the *flag* bit is set low so that the *Swap* signal remains unchanged after it is latched once. With decremented ramp (*Up_Down* = 0, flag = 1), when

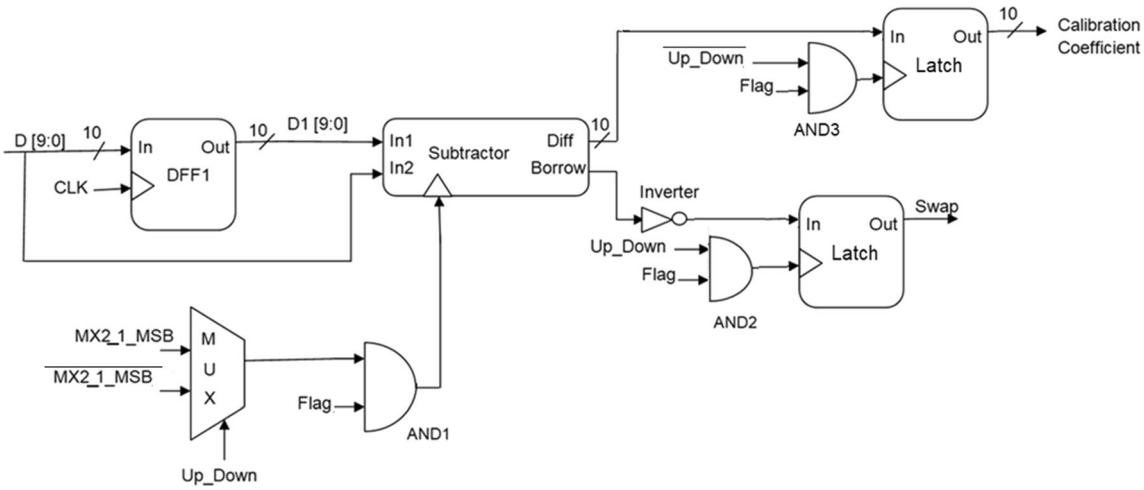

Fig. 6 Block diagram of the calibration algorithm

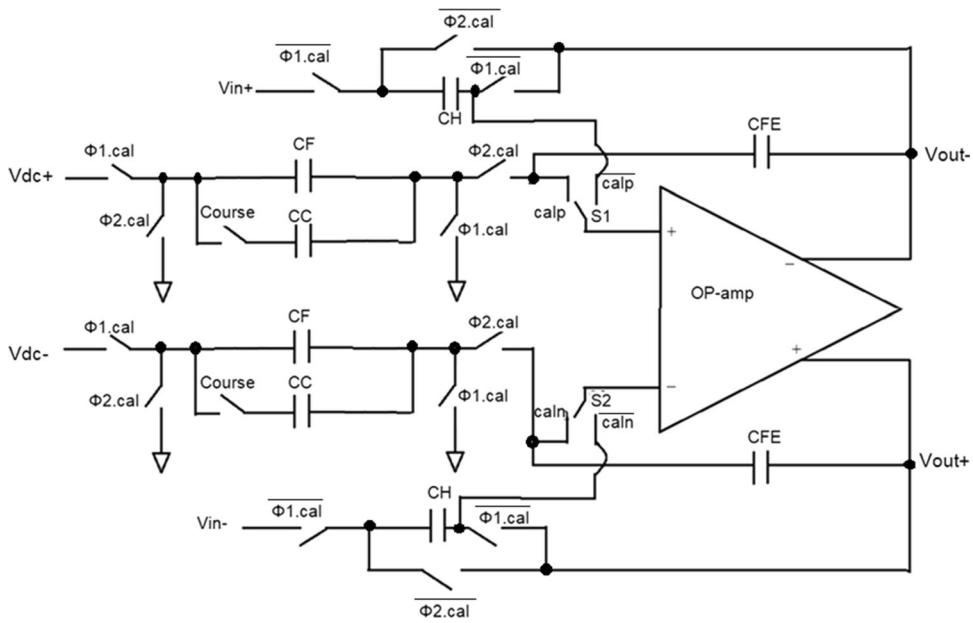

Fig. 7 Sample and hold amplifier and switched capacitor integrator

*MX*2_1_*MSB* bit changes from 1 to 0, the corresponding ADC output *D [9:0]* is subtracted from the delayed ADC output *D1 [9:0]* to calculate the calibration coefficients. At this point, the *flag* bit is set low so that the calibration coefficients remain unchanged after it is latched once. This marks the end of calibration phase.

The proposed calibration technique requires the ramp to be generated with a step size accurate to at least $\frac{LSB}{2}$ theoretically. The ramp generator is designed to have a step size of $\frac{LSB}{5}$ to take care of any non-ideality in the ramp generator. If the step size of the ramp is greater than $\frac{LSB}{2}$ near the jumps, then this would lead to incorrect calculation of calibration coefficients, hence, increasing the INL of the ADC. The ramp voltage was generated using a switched capacitor integrator [11]. As this calibration technique is a foreground technique, the same (high-performance) op-amp was used for the sample-and-hold circuit during normal operation and for the switched-capacitor integrator during calibration. The circuit of the combined block is shown in Fig. 7. C_H, $\overline{\phi 1.cal}$ and $\overline{\phi 2.cal}$ form the sample-and-hold circuit, and C_C, C_F, C_{FE}, ϕ1.cal and ϕ2.cal form the calibration circuit. $\phi 1$ and $\phi 2$ are non-overlapping clocks. Switches S1 and S2 are connected to *calp* and *caln*, respectively, during calibration and to $\overline{calp}$ and $\overline{caln}$, respectively, during normal operation. Recalling from Sec.2 that the ramp is used to determine the three jumps caused in the transfer characteristics due to the mismatches in the three MSB stages, the ramp needs to be extremely fine in the vicinity of the three jumps of interest, and can be coarse while traversing from one jump to the

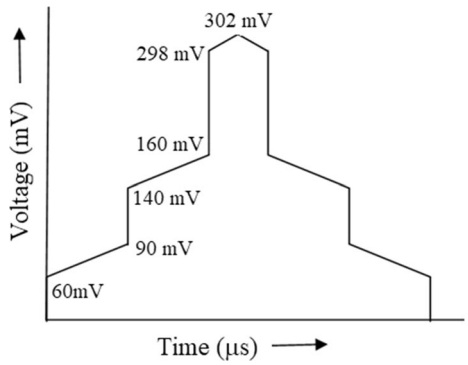

Fig. 8 Generation of fine and coarse ramp

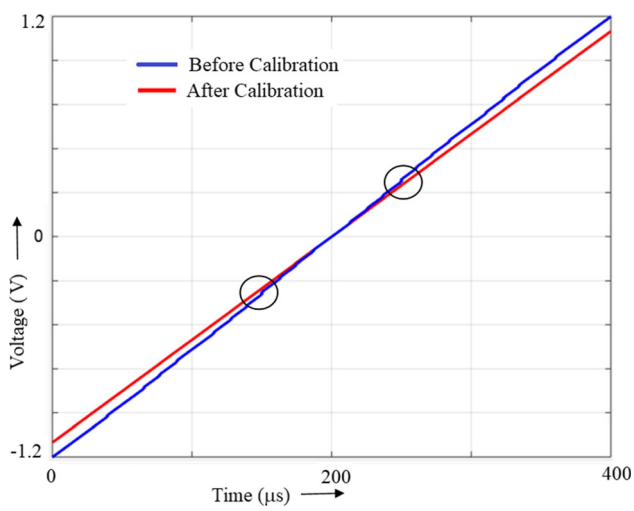

Fig. 9 Output transfer characteristics of the ADC before and after calibration

next. A fine ramp throughout will also work, but will take an inordinately long time to process. Thus in the switched capacitor integrator, C_F provides a fine ramp, and C_C is added in parallel to obtain a coarse ramp, with C_F set approximately to $\frac{C_C}{100}$.

The ramp signal needs to traverse the range from 0 V to 302 mV ($\approx \frac{V_{ref}}{4}$) for calibration. The range of the fine ramp that is to be generated varies depending on the maximum gain error considered. For this design, fine ramp is required to be generated between 75 ± 15 mV, 150 ± 10 mV and 300 ± 2 mV. Therefore a coarse ramp is generated from 0 to 60 mV, 90 to 140 mV and 160 to 298 mV. Both increasing and decreasing ramps are generated, the former to determine the gain and latter to calculate the digital calibration coefficients. Figure 8 shows the ramp voltage.

3.2 Simulation Results

A ramp signal varying from −1.2 to 1.2 V was applied to the ADC. The outputs of the ADC before and after calibration are shown in Fig. 9. A capacitance mismatch error of up to 5% in the first three stages was assumed. Fig. 9 shows that the proposed algorithm effectively eliminates the errors caused by capacitance mismatches. A couple of jumps are highlighted in Fig. 9.

Figure 10a, b show the INL plots of the ADC before and after calibration. As can be seen, INL is reduced significantly after calibration.

Figure 11a, b show the output spectrum of a 100 kHz full scale analog sine input which is sampled at 4 MSPS, before and after calibration. It is seen that SFDR improves from 38 dB before calibration to 53 dB after calibration. The power consumed by the ADC was 110 mW, out of which digital calibration hardware consumes only 76 µW. The power of the digital calibration circuit was estimated by the Cadence-Genus tool after synthesis of the Verilog HDL code to the target 180-nm CMOS SCL library.

The speed of the ADC is limited by the unity gain bandwidth of the op-amp. The op-amp used in this design [12] allows the ADC to operate with maximum sampling frequency of 40 MHz. For the purpose of testing the digital calibration algorithm, the input signal is being sampled at f_s = 4 MSPS. The designed ADC allows an input frequency

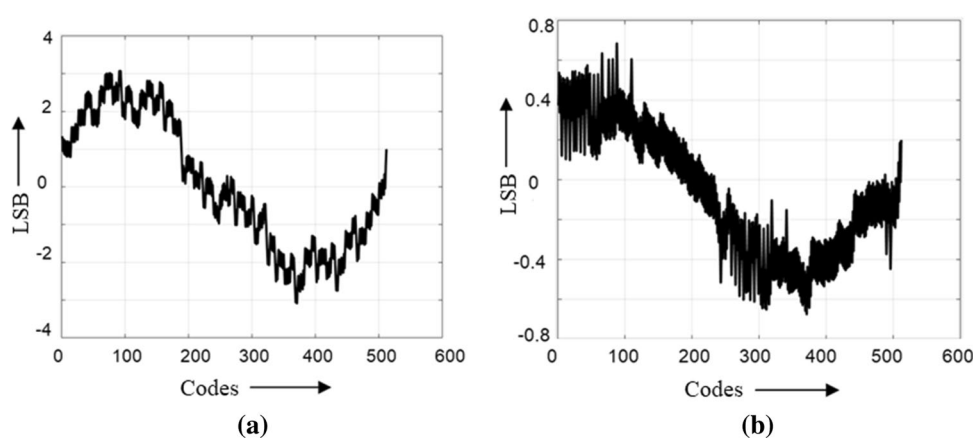

Fig. 10 INL of the 1.5 bits/stage ADC **a** before calibration and **b** after calibration

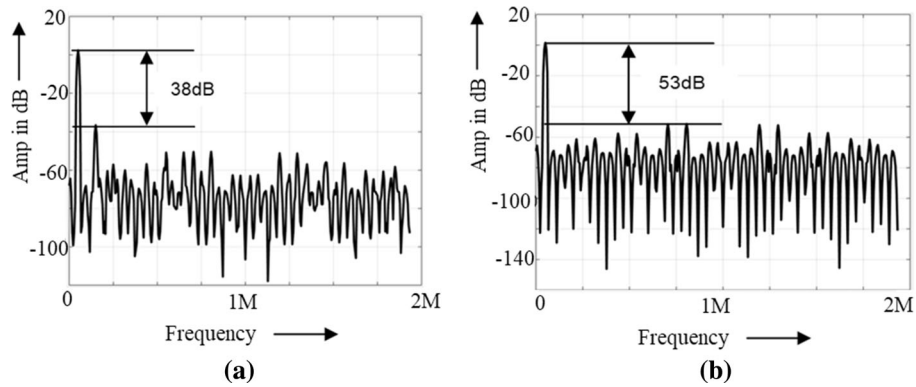

Fig. 11 Pipelined ADC output spectrum **a** before calibration and **b** after calibration

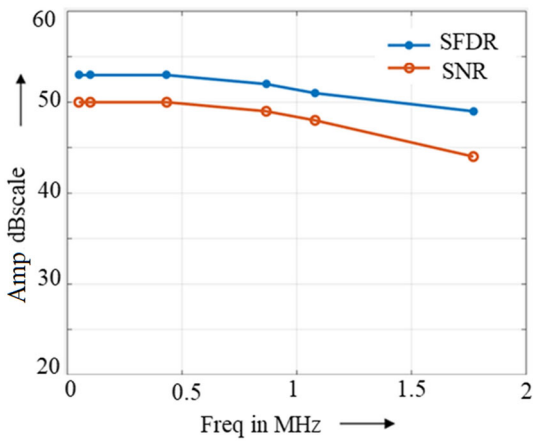

Fig. 12 SNR and SFDR variations versus the input signal frequency

of up to $\frac{f_s}{3}$ with little SNR degradation for 2% capacitance mismatch. Figure 12 shows the SNR and SFDR variations of the calibrated pipelined ADC versus the input signal frequency.

Figure 13a shows the output plots for a 10-stage, 1-bit/stage ADC with capacitance mismatch of 5% in the first 3 stages, before and after calibration, simulated in Matlab. Once again, it can be seen that the post-calibration plot eliminates the jumps due to capacitance mismatches. Figure 13b shows the INL of the ADC after calibration, which is seen to be within ± 0.5 LSB.

Similar to Figs. 13a, b and 14a, b show the characteristics of a one bit/stage algorithmic ADC for a 9 bits resolution simulated in Matlab. Once again it can be seen that the proposed algorithm is effective in obtaining a linear output characteristic and an INL in an acceptable range.

The proposed calibration scheme for 1.5 bits/stage Pipeline ADC is compared with several other techniques in Table 2 while Table 3 summarizes the performance of the ADC. Please note that '*' in the Table 2 indicates the fabricated ADCs where as the rest of them are simulated ones. Also, the figure of merit (FOM) is calculated based on the INL, DNL, Fabricated/simulated ADCs and resolution of the ADC. ADCs with lower FOM give a better performance. Performance of higher resolution ADCs are quite non-linear compared to the low resolution ADCs. The formula for calculating the FOM is as shown in Eq. (5). It can be seen that the ADC in the present work has the lowest FOM and hence has a better performance.

$$FOM = F \cdot \frac{(INL + DNL) \times 1000}{2^N} \tag{5}$$

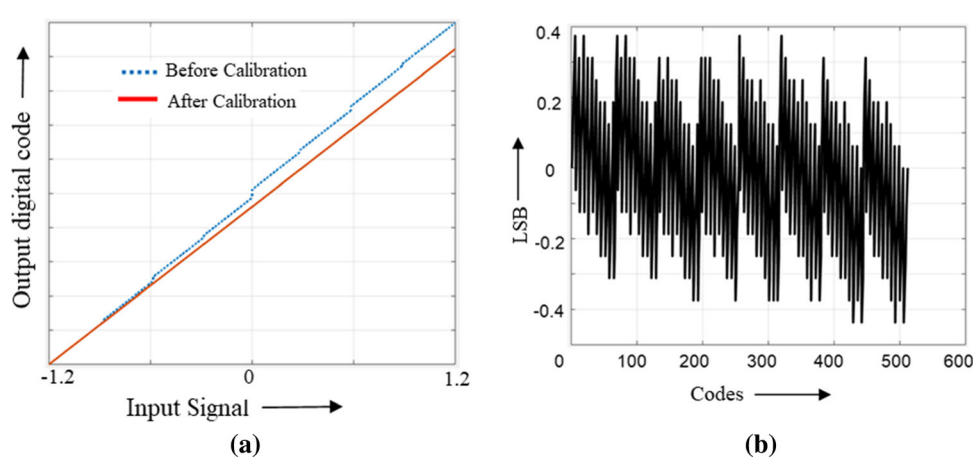

Fig. 13 **a** Output Characteristics of 1bit/stage pipelined ADC, **b** INL of 1 bit/stage pipelined ADC after calibration

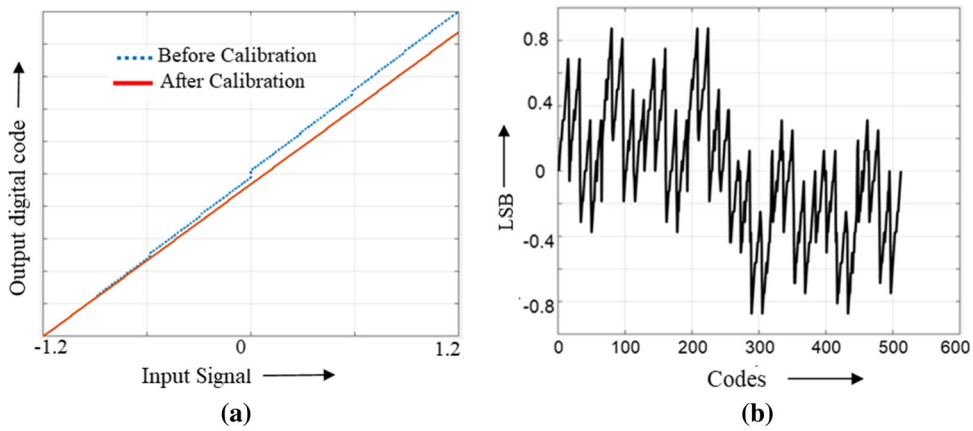

Fig. 14 **a** Output Characteristics of 1bit/stage algorithmic ADC, **b** INL of 1 bit/stage algorithmic ADC after calibration

Table 2 Comparison of 1.5 bits/stage Pipeline ADC with other calibration techniques

Reference	Resolution	Technology in nm	INL in LSB	DNL in LSB	Reference voltage in volts	FOM
[16]	8	600	0.75	0.75	5	5.8
[17]	8	180	0.8	–	3.3	–
[13]	8	250	0.8	0.65	3.3	5.6
[14]	8	180	0.9	0.7	1.8	6.2
[15]*	9	180	4.1	1.6	1.8	5.5
This work	9	180	0.72	0.56	1.8	2.5

Table 3 Performance table of the 1.5 bits/stage Pipeline ADC

Resolution	9-bits
Sampling rate	4 MHz
SNR	50 dB@100 KHz
SFDR	53 dB@100 KHz
INL	0.72 LSB
DNL	0.56 LSB
Input voltage swing	1.2 Vp-p
Power dissipation (Without scaling currents in stages)	110 mW
Predicted power dissipation by scaling consecutive stages	40 mW
Process	1.8 V, 180 nm CMOS
Power supply	1.8 V

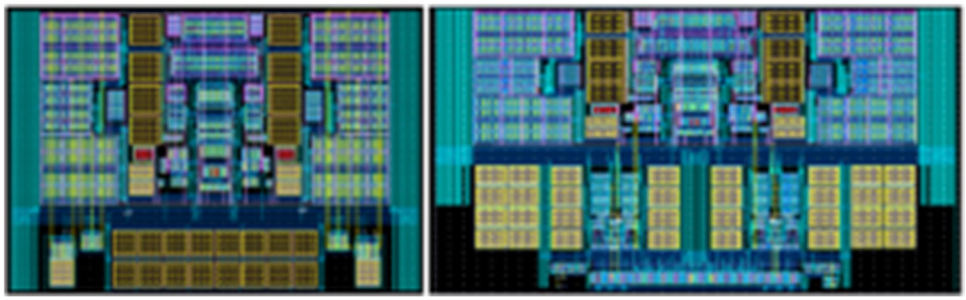

Fig. 15 Layouts of **a** SHA, **b** MX2 stage

Table 4 Summary of schematic and extracted layout simulations

	Schematic simulation results	Post layout simulation results
Op-amp (low frequency gain)	88.8 dB	89 dB
Op-amp bandwidth	594.6 MHz	528.4 MHz
Op-amp phase margin	56°	53°
Difference in voltage between required MX2 output and actual MX2 output	421 μ V	932.6 μ V

where $F = 0.5$ for fabricated ADCs and 1 for simulated ADCs. The fabricated ADCs are given 50% more weightage than the simulated ones during the calculation of FOM.

Figure 15a, b shows the layout of the SHA and the MX2 stage. The layout of the op-amp is discussed in detail in [12]. The extracted post-layout simulations of the individual blocks of the ADC are found to be satisfactory. Post Layout simulations of the MX2 stage shows that the difference between the expected output and final MX2 output is less than half LSB which is acceptable. Even if the heights of the jump in the ADC output transfer characteristics differ during post layout simulation, the calibration coefficients are suitably calculated to maintain the linearity of the ADC. The schematic and layout simulation results are summarized in Table 4.

4 Summary

A simple and efficient deterministic digital calibration technique is proposed to calibrate the errors due to capacitance mismatch and finite op-amp gain in pipelined ADCs. The technique handles both missing codes and missing decision levels, thus reducing the INL of the ADC. The technique was demonstrated on a 10-stage, 1.5-bits/stage pipelined ADC. With a 5% capacitance mismatch in the three MSB stages, calibration reduced the INL to less than 0.8 LSB for inputs ranging from -1.2V to 1.2V. The technique can be used for algorithmic ADCs as well.

All data generated or analysed during this study are included in this published article.

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