CMOS realization of OTA based tunable grounded meminductor

Anamika Raj[1] · Keshab Kumar[1] · Pankaj Kumar[1]

Abstract

A simple and robust design for CMOS realization of a tunable grounded meminductor using three operational transconductance amplifier (OTA) and two capacitors have been proposed. Both theoretical analyses and simulation using Cadence Virtuoso at $0.18\ \mu m$ CMOS technology parameters verify the validity of the meminductor. Its meminductance can be tuned with the help of external bias voltage and has an operating frequency of 10 MHz, which makes it suitable for high-frequency applications. The proposed meminductor can also be configured using both incremental and decremental mode by interchanging the pin of OTA. Various parameters variability analysis like process variation, capacitor variation, voltage variation, temperature variation, and frequency variation has been carried out and our proposed meminductor has shown excellent performance.

Keywords Memristor emulator · Meminductor · Pinched hysteresis loop · OTA

1 Introduction

According to the circuit theory, there are three fundamental two-terminal circuit element, defined with the relationship of current-voltage, charge-voltage, and flux-current. The relationship between current (I) and voltage (v) defines resistor, the relationship between charge (q) and voltage (v) defines capacitor, and the relationship between flux (ϕ) and current (I) defines inductor. The fourth missing fundamental two-terminal circuit element is characterized by the relation between flux (ϕ) and charge (q), known as the memristor.

In 1971 L. O. Chua [1] reported the fourth missing circuit element memristor, which means memory depending upon past history (memory + resistor) and the physical relationship between ϕ and q is not a necessary condition. Memristor is characterized by a relation $g\ (\phi,\ q) = 0$. It provides a missing link between flux and charge. Maxwell's equation explain the non-linear characterization of memristor, charge $q(t) = \int_{-\infty}^{t} i(t)dt$ and flux $\phi(t) = \int_{-\infty}^{t} v(t)dt$. Memristor has peculiar properties, then resistor, inductor, or capacitor which cannot be realized using RLC networks. Somehow memristor behaves as a non-linear resistor with memory. At high frequency, the memristor behaves as a linear resistor.

The two new memory elements that are generalized by the memristor are memcapacitor and meminductor [2]. Both have the storage capacity of energy in the form of capacitance and inductance, respectively. Recently in analog memory, these circuits have many applications as adaptive filters [3], neuromorphic circuit [4], low power computation [5], and programmable analog circuits [6,8]. Hewlett Packard designed a thin-film $Ti\,O_2$ [8] based memristor, but it had a disadvantage of complexity in design. The complexity of design in Hewlett Packard led the analog designer to use various active blocks for the modeling of the memristor [9]-[11]. But, there are no standard models of memristor that can be followed for designing memristor. Recently it has been generated with VDTA (Voltage Difference Transconductance Amplifier) and OTA (Operational Transconductance Amplifier). In this, memristance swing can be controlled by changing the current of the OTA. Later, a flux controlled memristor using Operational Transconductance become new analog emulator circuit. Meminductor is a new special class of memory element realized by connecting memristors with the mutator circuit. This phenomenon is similar to a memristor emulator that converts the mutator into a non-linear characteristic of a memristor [12,13]. Mutator based meminductor [14] does not apply to all memristors. However, the researcher designed a meminductor using commercially available ICs [15]; but, this type of meminductor has a large number of passive components and less operating frequency. Therefore, in this paper meminductor with three active ele-

✉ Pankaj Kumar
   pankajjha@nitp.ac.in

1   Microelectronics and VLSI Design Lab National Institute of
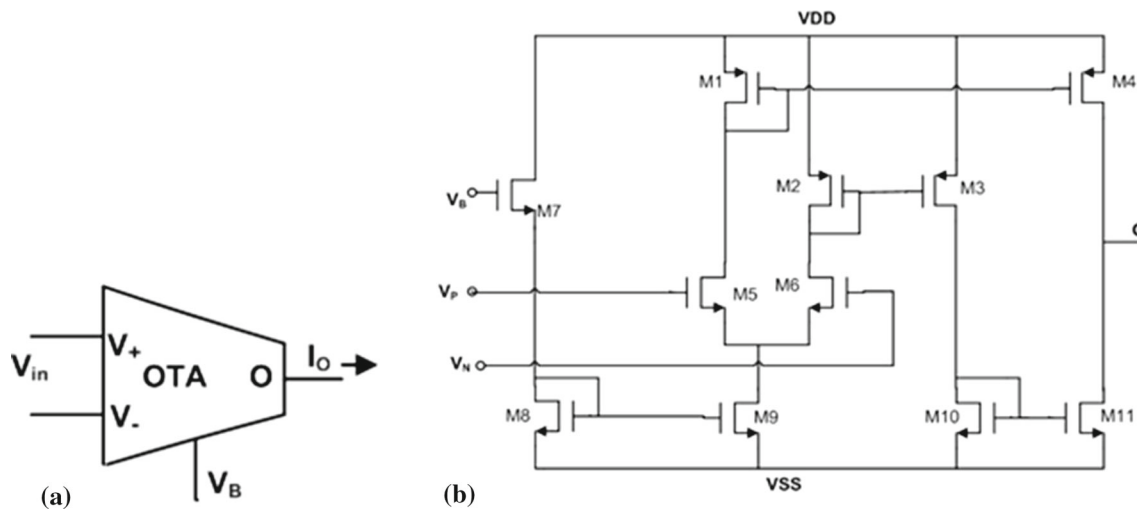   Technology Patna, Bihar, India

Fig. 1 **a** Circuit symbol of OTA and **b** internal structure of CMOS realization of OTA

ment (OTA) and only two capacitor has been proposed. This paper is organized as follows: Sect. 2 incorporates the circuit description of proposed OTA based tunable meminductor, along with the mathematical derivation for investigation. Simulation parameters and results are elaborated in Sect. 3. Parameters variability analysis has ben done in Sect. 4. Finally, Sect. 5 draws important conclusions from present investigation.

2 Circuit description

The Operational Transconductance Amplifier (OTA) has high input impedance as well as high output impedance. The circuits symbol of OTA is shown in Fig. 1a and CMOS realization of OTA is shown in Fig. 1b.

The characteristics of an OTA is expressed as

$$I_o = G_m V_{in}, \tag{1}$$

where $V_{in} = V_+ - V_-$, called as differential input, G_m is the transconductance of an OTA [16]. The transconductance of an OTA is expressed as

$$G_m = \frac{K}{\sqrt{2}}(V_B - V_{ss} - 2V_{th}), \tag{2}$$

$$K = \mu C_{ox} \frac{W}{L}, \tag{3}$$

where μ, C_{ox}, W, L, and V_{th} are mobility of carrier, capacitance per unit area, channel width, channel length, and threshold voltage of MOSFET respectively. The CMOS realisation of the proposed grounded meminductor emulator is shown in Fig. 2

The mathematical analysis of the proposed meminductor emulator can be done in following ways using design shown in Fig. 2

$$I_1 = G_{m1} V_{in}, \tag{4}$$

$$V_1 = \frac{G_{m1}}{C_1} \int V_{in} dt = \frac{G_{m1}\phi(t)}{C_1} \tag{5}$$

$$I_2 = G_{m2} V_1, \tag{6}$$

$$I_2 = \frac{G_{m1} G_{m2}\phi(t)}{C_1}, \tag{7}$$

$$V_2 = \frac{G_{m2} G_{m1}\rho(t)}{C_1 C_2}, \tag{8}$$

$$V_{B3} = V_2, \tag{9}$$

$$V_{B3} = \frac{G_{m2} G_{m1}\rho(t)}{C_1 C_2}, \tag{10}$$

where $\rho(t) = \int \phi(t)dt$. Further, calculations are;

$$I_3 = \pm G_{m3} V_1, \tag{11}$$

$$I_3 = \pm \frac{G_{m1} G_{m3}\phi(t)}{C_1}, \tag{12}$$

$$I_{in} = -I_3, \tag{13}$$

$$I_{in} = \pm \frac{G_{m1} G_{m3}\phi(t)}{C_1}, \tag{14}$$

$$\frac{I_{in}}{\phi(t)} = \pm \frac{G_{m1} G_{m3}}{C_1}. \tag{15}$$

From Eqs. (2)–(15)

$$\frac{I_{in}}{\phi(t)} = \pm \frac{G_{m1}}{C_1} \frac{K}{\sqrt{2}}(V_{B3} - V_{ss} - 2V_{th}). \tag{16}$$

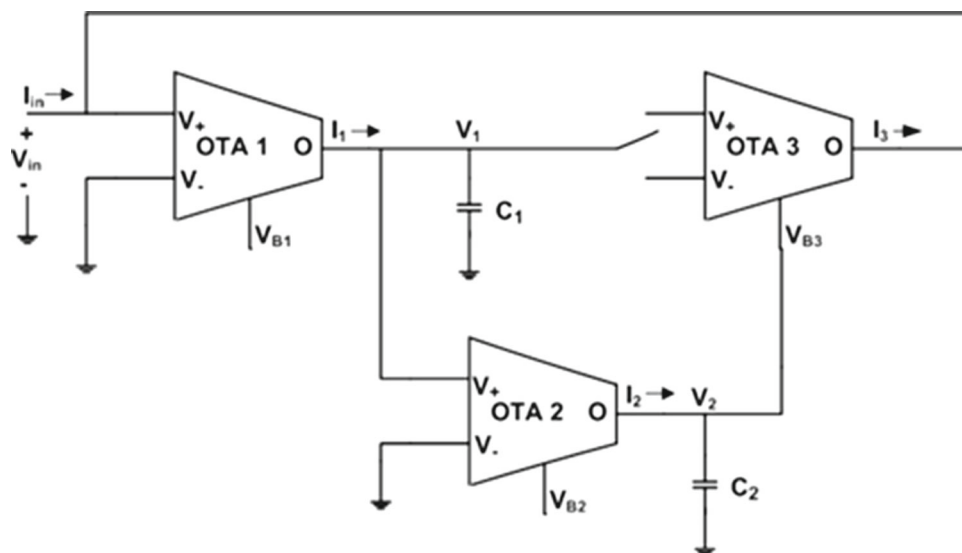**Fig. 2** **a** Schematic diagram of the proposed grounded meminductor emulator realization with CMOS

Table 1 Aspect ratio of MOSFET used for the simulation of the proposed meminductor

MOSFET	W (μm)	L (μm)
M_{1-4}	12	0.375
M_{10}	12	0.510
M_{5-9}, M_{11}	12	0.500

From Eqs. (10)–(16)

$$\frac{I_{in}}{\phi(t)} = \pm \frac{G_{m1}}{C_1} \frac{K}{\sqrt{2}} \left(\frac{G_{m2} G_{m1} \rho(t)}{C_1 C_2} - V_{ss} - 2V_{th} \right). \quad (17)$$

Thus, the relation between I_{in} and $\phi(t)$ has been obtained in Eq. (17). Here, the positive sign indicate the incremental operation and negative sign indicate the decremental operation. Hence, the proposed tunable CMOS realization of OTA can operate in both incremental and decremental operation by interchanging the terminal of third OTA between V_+ and V_-.

3 Simulation parameters and results

Simulation of OTA based grounded tunable meminductor realization with CMOS using Cadence Virtuoso Tool, at gdpk 0.18 μm technology having aspect ratio as given in Table (1) justify the above theoretical explanation. In simulation a supply voltage of $V_{DD} = -V_{SS} = 1.2$ V with a tuned voltage of $V_{B1} = V_{B2} = 0.1$ V. Layout of the proposed OTA based grounded meminductor is shown in Fig. 3, transient response are shown in Fig. 4a, b, whereas hysteresis plot is shown in Fig. 4c. These responses were carried out for input supply voltage having magnitude 500 mV at frequency 10 MHz.
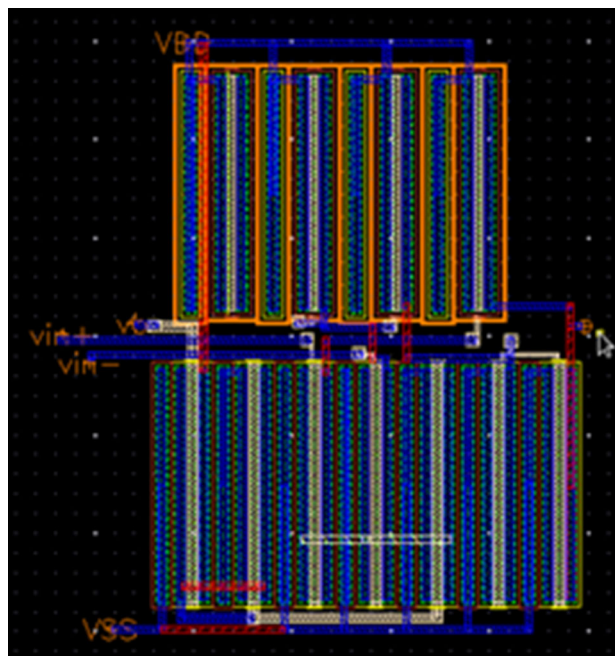

Fig. 3 Layout of proposed OTA based tunable meminductor

The value of capacitor $C_1 = 1$ pF and $C_2 = 2$ pF. The input voltage and flux have a 90° phase shift.

As non-volatile nature is an important characteristic of the memristor family, the proposed meminductor is examined for non-volatile nature in Fig. 5 by considering the input pulse amplitude of 500 mV at a pulse width of 100 ns for the period of 250 ns. The external bias voltage is 500 mV, $C_1 = 90$ pF, and $C_2 = 1$ pF. In Fig. 5a, b input voltage and meminductance is plotted with respect to time and shows that proposed grounded meminductor is non-volatile in nature as the flux and current varies during on time and it remains constant during off state.
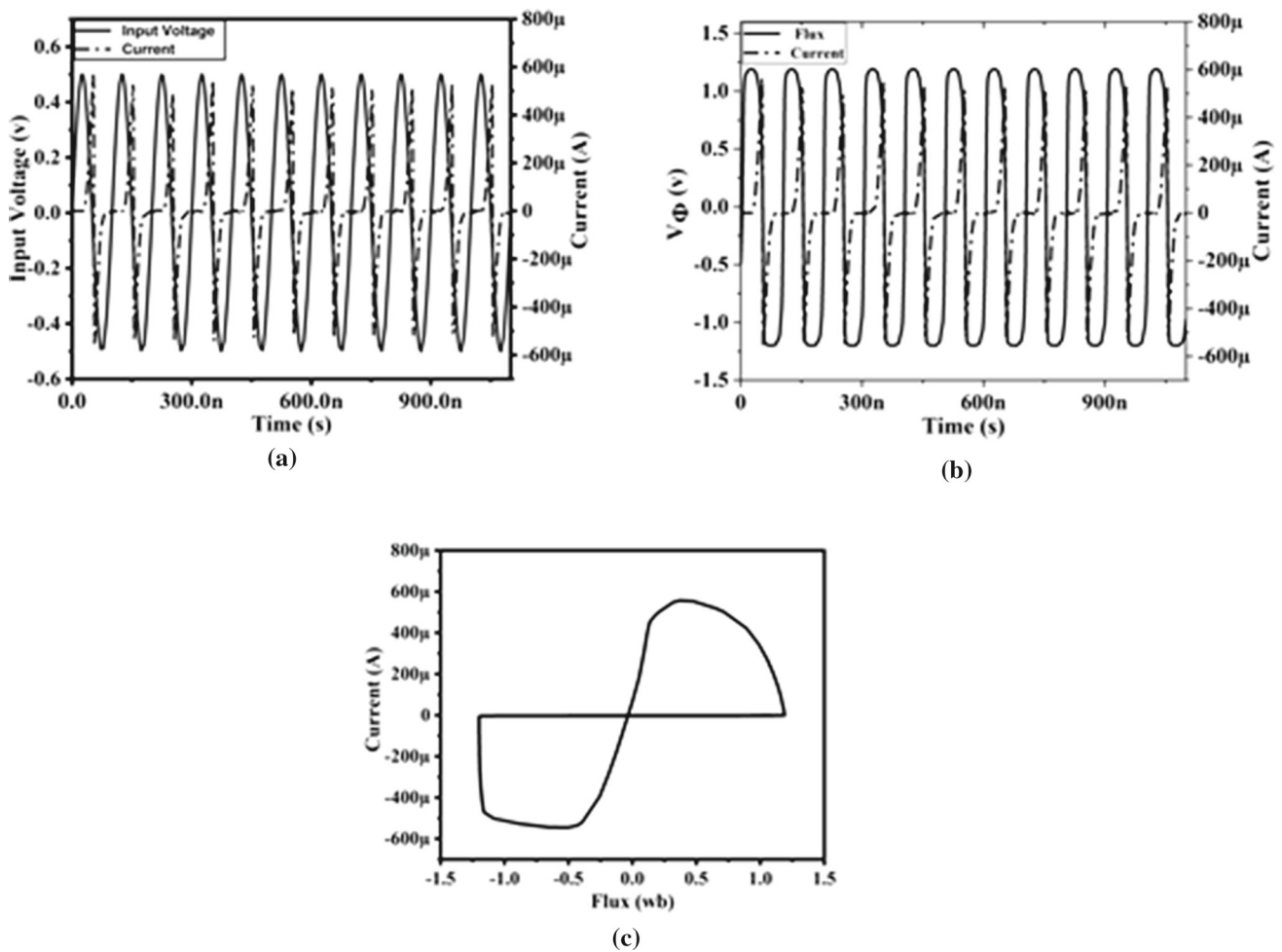
Fig. 4 Transient response of the proposed OTA based tunable meminductor between **a** input voltage and current, **b** between flux and current, and **c** hysteresis loop of the proposed tunable meminductor
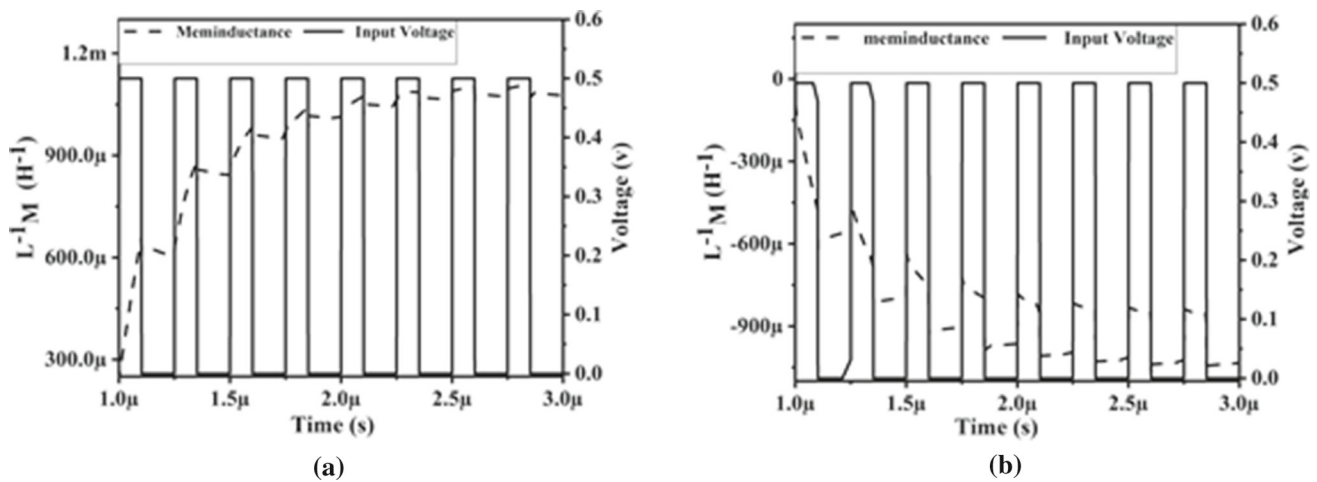

Fig. 5 **a** Incremental mode and **b** decremental mode of the proposed meminductor
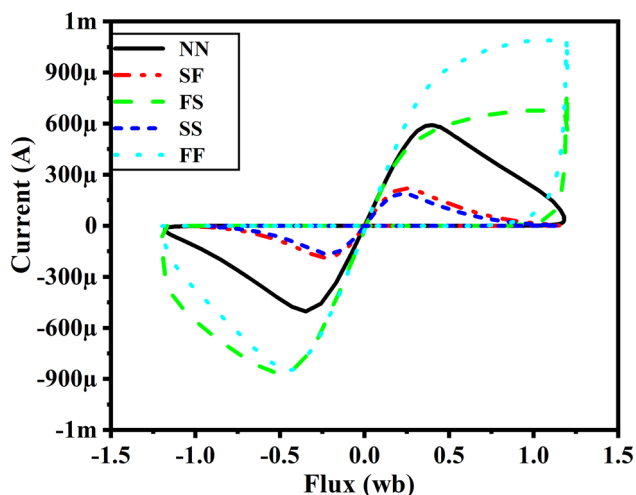
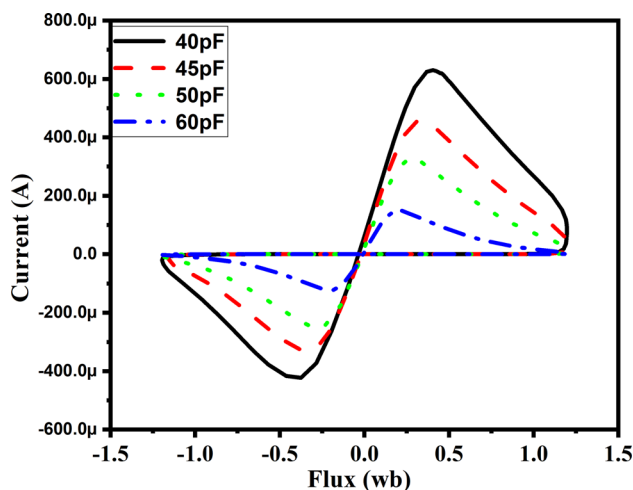**Fig. 6** Hysteresis loop at different process corners

Fig. 7 Hysteresis loop of $V_\phi - I$ for $C \in \{40, 45, 50, 60\}$ pF, at $V_{B1} = V_{B2} = 0.1$ V, and input signal 1 V

4 Parameters variability analysis

4.1 Process variation

Process variation for different process model like SS, SF, NN, FS, and FF has been examined for the proposed grounded tunable meminductor. The current flow in FF model is larger than SS model along with area variation in hysteresis loop for 500 KHz at $C_1 = 30$ pF and $C_2 = 40$ pF as shown in Fig. 6. It also exhibits pinched hysteresis loop in all the process variation.

4.2 Capacitor variation

Effect on $V_\phi - I$ hysteresis loop for $C \in \{40, 45, 50, 60\}$ pF at fixed value of frequency 500 KHz, fixed bias voltage $V_{B1} = V_{B2} = 0.1$ V, and amplitude of input signal 1 V has been shown in Fig. 7. It shows that the magnitude of current increases through the meminductor by moving to the lower value of capacitances, which validates the Eqs. (17) as this equation says that current through meminductor is inversely proportional to the capacitance.

4.3 Voltage variation

Equation (17) of the proposed meminductor shows that current of meminductor is directly proportional to transconductance G_{m1} and G_{m2}. This G_{m1} and G_{m2} are directly proportional to external bias voltage V_{B1} and V_{B2} as per Eq. (2). So, according to these equation meminductance should increase with increase of external voltage and same characteristic is shown by the proposed meminductor in Fig. 8. The simulation is carried for external bias voltage $V_{B2} \in \{25, 50, 75, 100\}$ mV at frequency 500 KHz,
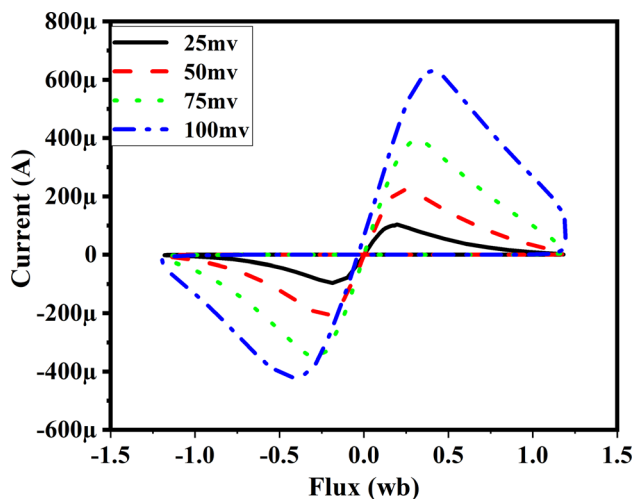

Fig. 8 Hysteresis loop of $V_\phi - I$ for $V_{B2} \in \{25, 50, 75, 100\}$ mV, at frequency 500 KHz, $C_1 = 30$ pF, and $C_2 = 40$ pF

$C_1 = 30$ pF, and $C_2 = 40$ pF. It concludes that meminductance can be tuned by external bias voltage.

4.4 Temperature variation

In CMOS circuit temperature has a large impact on the carrier mobility, threshold voltage, and velocity saturation [17], which further affect the drain current and performance of the circuit. The effect of temperature on the hysteresis loop is shown in the Fig. 9. for $T \in \{-40°, -20°, 0°, 20°, 40°\}$ C at frequency 500 KHz, $C_1 = 30$ pF, $C_2 = 40$ pF, $V_{B1} = V_{B2} = 0.1$ V and amplitude of input signal 1 V. The proposed meminductor shows robust performance with the change of temperature.
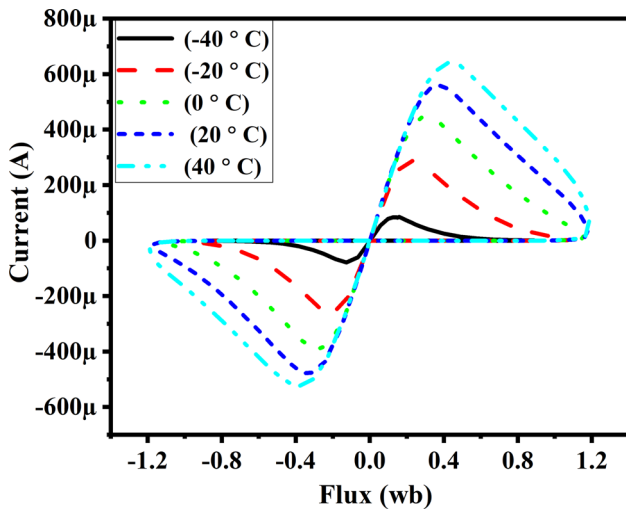
Fig. 9 Hysteresis loop of $V_\phi - I$ for $T \in \{-40°, -20°, 0°, 20°, 40°\}$ C at frequency 500 KHz, $C_1 = 30$ pF, $C_2 = 40$ pF, $V_{B1} = V_{B2} = 0.1$ V and amplitude of input signal 1 V

Fig. 11 Hysteresis loop of $V_\phi - I$ for various combination of f, C_1, and C_2 at $V_{B1} = V_{B2} = 0.1$ V and amplitude of input signal 1 V

4.6 Comparison

The proposed tunable meminductor has been compared with existing meminductor in terms of number of active components like VDTA, OTA, etc., number of passive components like resistor, capacitor, inductor, etc., modes in which these are operating, and their operating frequency. The comparison are shown in Table 2. Thus, from this comparison we conclude that the proposed tunable meminductor has less number of passive components which reduces the power consumption of the circuit. The current in the pinched hysteresis loop of our proposed grounded meminductor circuit ranges from 600 to $-600\,\mu$A in comparison 20 to $-20\,\mu$A in circuit design reported by Vista and Ranjan (2020) [22]. At the same time capacitor used in our design is 1 pF and 2 pF, whereas Vista and Ranjan (2020) used 50 pF and 85 pF, therefore in the proposed circuit design delay will be less and will also require less area in layout design. The average power dissipation in proposed circuit is 120 μW, whereas circuit reported by Vista and Ranjan has 200 μW average power dissipation. Finally, the operating frequency of 10 MHz for proposed tunable meminductor is highest among all the reported work in Table 2, which makes it more suitable for high-frequency applications. Further, it can also be tuned to desired frequency by proper selection of capacitor.

5 Conclusion

Memristor emulators have gained attention nowadays because of its unique features, so it becomes essential to develop a memristor-based circuit and system design. We have proposed a simple and robust design for CMOS realization of a tunable grounded meminductor using three
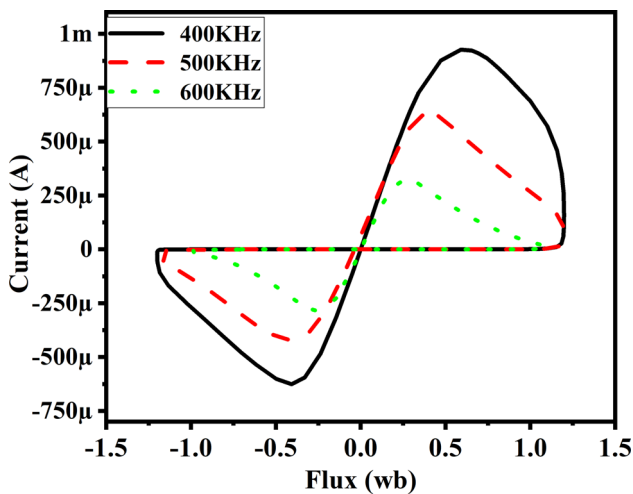

Fig. 10 Hysteresis loop of $V_\phi - I$ for $f \in \{400, 500, 600\}$ KHz at $C_1 = 30$ pF, $C_2 = 40$ pF, $V_{B1} = V_{B2} = 0.1$ V and amplitude of input signal 1 V

4.5 Frequency variation

In the proposed meminductor frequency variation of $f \in \{400, 500, 600\}$ KHz at $C_1 = 30$ pF, $C_2 = 40$ pF, $V_{B1} = V_{B2} = 0.1$ V and amplitude of input signal 1 V is shown in Fig. 10. According to this meminductance decreases with increase of frequency. But, this issue has been resolved by proper selection of capacitance value of C_1 and C_2 as shown in Fig. 11 where at $C_1 = 1$ pF and $C_2 = 2$ pF the proposed meminductor give good performance even at $f = 10$ MHz.
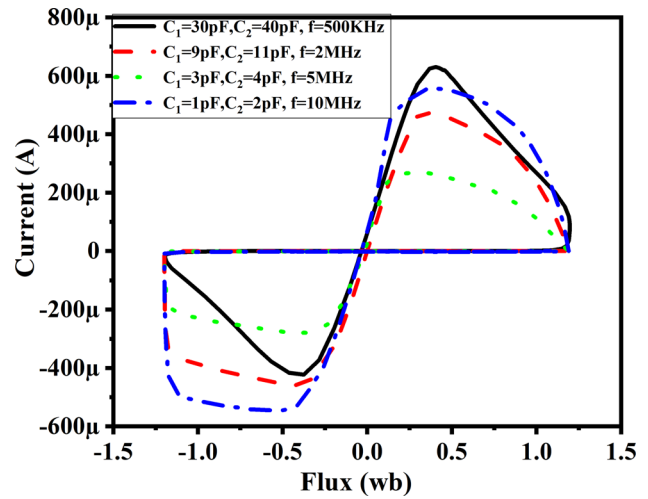
Table 2 Comparison of proposed tunable meminductor with existing meminductor on different parameters

Ref. No.	No. of active component	No. of passive component	Mode	Operating frequency
[18]	–	–	–	Few Hz
[19]	Opamp-1	R-1, C-1, MR	Grounded	Few Hz
[14]	DOCCII-2	R-1, C-1, MR-1	Floating	Few Hz
[20]	Opamp-2, AD633-1	R-7, C-2	Floating	Few Hz
[21]	Opamp-3, NMOS-12, AD633-1	R-2, C-2, L-1	Grounded	Few Hz
[22]	VDTA-2	R-1, C-2	Floating	1 MHz
[Proposed]	OTA-3	C-2	Grounded	10 MHz

OTA and two capacitors. Meminductor has grounded passive elements, which make it more suitable for making it fully monolithic. The proposed meminductor exhibits excellent performance in comparison to existing emulators. Both theoretical analyses and simulation using commercially available tool Cadence Virtuoso at $0.18 \ \mu m$ CMOS technology parameters verify the validity of the meminductor. Various parameters variability analysis like process variation, capacitor variation, voltage variation, temperature variation, and frequency variation has been carried out, and our proposed meminductor has shown excellent performance. For a better analysis of performance, the proposed meminductor has been compared with the existing emulators and has shown better performance than existing. Its operating frequency of 10 MHz makes it suitable for high-frequency applications.

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Keshab Kumar is pursuing M. Tech. degree in electronics and communication engineering department at National Institute of Technology, Patna, India.

Anamika Raj is pursuing M. Tech. degree in electronics and communication engineering department at National Institute of Technology, Patna, India.

Pankaj Kumar received the M.Tech. degree in electronics and communication engineering from PDPM Indian Institute of Information Technology Design & Manufacturing, Jabalpur, India in 2014. He is currently Assistant Professor in the Department of Electronics and Communication Engineering, National Institute of Technology, Patna, India.