Analog Integrated Circuits and Signal Processing (2021) 107:567–573
https://doi.org/10.1007/s10470-021-01802-5

A dual-input extended-dynamic-PCE rectifier for dedicated far-field RF energy harvesting systems

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Received: 30 June 2020 / Revised: 25 November 2020 / Accepted: 22 January 2021 / Published online: 13 March 2021

Abstract
This paper presents a dual-input extended-dynamic-range, high-PCE rectifier for dedicated far-field RF energy harvesting systems. Two identical input RF energy supply source are applied into two individual rectifier. The rectifier with the highest PCE is selected to deliver dc power to a single-load element. A logic control circuit senses P_{in} from the rectified dc voltage and toggles between the rectifiers by generating two control voltage to attain high-PCE across P_{in}. Simulated in a 65nm CMOS process, the proposed system achieves an extended DR of 26 dB for an output load, R_L = 100 kΩ. Furthermore, a peak PCE of 54.85% and 47.87% was achieved for R_L = 100 kΩ and R_L = 150 kΩ, respectively. The sensitivity for an output voltage of 1 V with R_L = 100 kΩ is -20.6 dBm.

Keywords Rectifier · RF energy harvesting (RFEH) system · Power conversion efficiency (PCE) · Logic control circuit

1 Introduction

Internet of things (IoT) is an emerging technology that has been perceived by the semiconductor industry as the next technological revolution that will transform the consumers need. The vision of realizing IoT requires major enabling technologies such as wireless sensor nodes (WSNs) which are group of spatially dispersed sensors used to monitor the physical conditions of the environment as illustrated in Fig. 1. Though WSN has significant applications in various IoT infrastructure, the technology comes with a major bottleneck in its requirement of a reliable and extended power source.

Energy harvesting has gained widespread attention as an alternative power source for WSNs [1, 2]. However, ambient energies is dependent on the available energy in the free space environment, inhibiting the reliability of the power source. A dedicated far-field Radio Frequency (RF) energy source which transmits RF energy in the surrounding environment can alternatively be used to power-up WSNs [3]. Despite the effectiveness of radiating RF energy as a power source, the energy density received by each WSN in a network of dispersed sensors varies according to its distance from the transmitter. This prompts the need of a high power conversion efficiency (PCE) rectifier in Far-Field RF energy harvesting (RFEH) systems to efficiently convert the RF energy to DC across wide variation of input RF power (P_{in}) level. Hence, a wide-PCE range rectifier with satisfactory performance in sensitivity for a given output load (R_L) is desirable.

Initiatives to improve the dynamic range (DR) performance of rectifiers in RFEH systems have been reported in [4–6] where DR is defined in this work as the P_{in} range for PCE above 20% [6] and PCE is expressed as,

$$\mathrm{PCE} = \frac{P_{out}}{P_{in}} = \frac{V_{out}^2 R_L}{P_{in}} \quad (1)$$

where P_{out} is the power consumption of the load, R_L and V_{out} is the rectified output voltage. A cross-connected Dickson rectifier is employed in [6] to minimize the detrimental effect of V_{th} to obtain a peak PCE of 60% and a sensitivity of -21 dBm. However, the performance was only reported for open load condition. Generally, R_L has significant effect on PCE and sensitivity performances which are inherent trade-offs in RFEH systems [2]. In [5], an adaptive CCDD scheme is proposed to extent the high-

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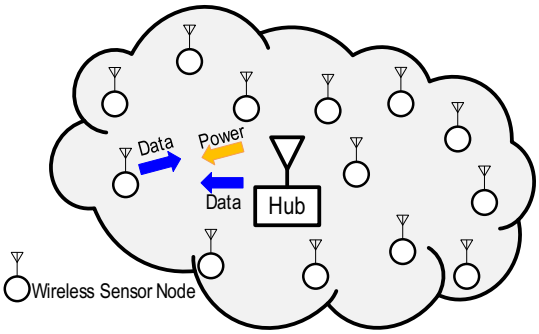

Fig. 1 Illustrated concept of Dedicated Far-Field RF energy harvesting WSN

PCE range of the rectifier. A 2-stage CCDD rectifier is configured in series/parallel (cascade/cascode) configuration through a control circuit according to the level of P_{in}. Despite achieving a DR of 11 dB, it reports a poor sensitivity of 0 dBm which is not suitable for far-field RFEH systems. A dual-path rectifier is proposed in [6] to extend the high-PCE range for RFEH systems. The rectifier consists of a low-power path and a high-power path to rectify the RF energy at low and high, P_{in}, respectively. An adaptive control circuit selects the rectifier path according to P_{in}. A DR of 11 dB and a peak sensitivity of -17.7 dBm was achieved. However, the adaptive control circuit consumes a portion of the harvested P_{in} which impairs the achievable PCE.

To overcome the aforementioned challenges, this work propose a dual-input rectifier to achieve an extended-dynamic-PCE range for dedicated far-field RFEH systems. The novelty of this system is in the integration of a dual-input rectifier scheme to harvest RF energy from two individual energy sources with identical P_{in} level inspired by [7]. A logic control circuit complements the system to sense and toggle between the two rectifiers to select the path of high-PCE with respect to P_{in}. Section II presents the proposed rectifier scheme. The design methodology of the rectifier is discussed in Section III. Section IV presents the simulation results and Section V concludes the findings.

2 Proposed dual-input rectifier

Figure 2 shows the block diagram of the proposed rectifier scheme. The scheme harvests RF energy of the same frequency as two input sources [7]. Alternatively, two dissimilar rectifier topologies – CCDD and Dickson – are utilized into a single unit to achieve an extended DR performance. MN_{S1}, MP_{S2}, MP_{S3} and MP_{S4} are gate switching transistors for selecting the rectifier according to P_{in}. Across P_{in} level, the logic control circuit sense the output rectified DC voltage and generate two control voltages

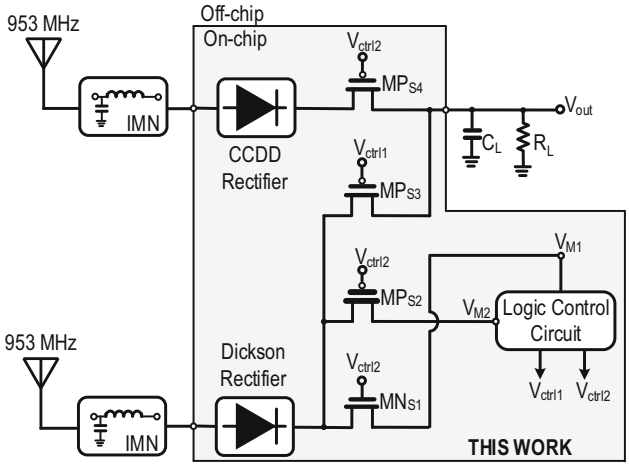

Fig. 2 Block diagram of the proposed rectifier in an RFEH system

(V_{ctrl1} and V_{ctrl2}) to select the rectifier with high-PCE to extend the DR performance. Section III further elaborates the design of the rectifier.

3 Design methodology

3.1 Rectifier

The Dickson and CCDD rectifiers are the two primary rectifier topology for RFEH [10]. Their performances are restricted by the intrinsic V_{th} drop of the transistors during forward conduction and reverse leakage current [11, 12]. In addition, the PCE range of the rectifier for a specific R_L differs across P_{in}, which is an inherent trade-off. The PCE curve of the Dickson and CCDD rectifier for R_L = 150 kΩ is shown in Fig. 3. Generally, the CCDD rectifier attains peak PCE at low P_{in} levels due to its active V_{th} cancellation scheme, resulting in a small *on*-resistance [10]. However,

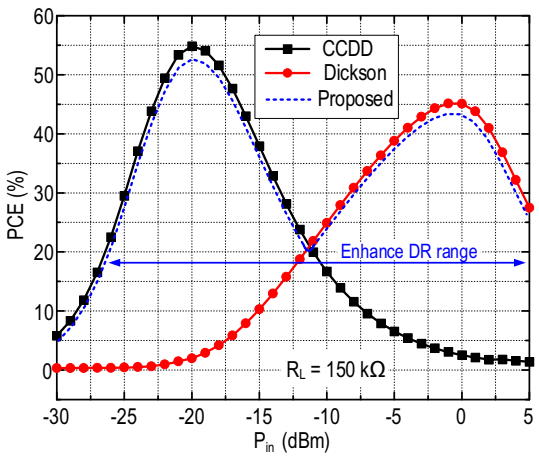

Fig. 3 Rectifier PCE plot for R_L = 150 kΩ

at high P_{in} levels, the small *on*-resistance promotes high reverse leakage current which detriments the rectifier's PCE. Inversely, the Dickson topology achieves peak PCE when the level of P_{in} is high as the diode-connected transistors configuration of this topology acts as an effective voltage pumping devices [12]. At low P_{in} the V_{th} of the transistors creates a large voltage drop resulting in lower voltage harvested, degrading the PCE. By exploiting the high-PCE range for each topology for a specific R_L, the cumulative PCE from of each rectifier maximize the performances of the architecture as illustrated in Fig. 3.

Figure 4(a) and Fig. 4(b) shows schematic diagram of adopted Dickson and parallel CCDD rectifier, respectively. Multi-stage configuration delivers higher output voltage and enhances the peak PCE performance compared to a single-stage rectifier. In addition, each rectifier topology has an optimum number of stages to achieve peak PCE for a given R_L. However, exceeding the number of optimal stages could degrade rather than improve the PCE performance [3, 11]. Figure 5(a) and (b) shows the simulated PCE plot of CCDD and Dickson rectifier for different number of stages in the adopted technology. It was found that the optimum number for both rectifiers is 4-stage. Therefore, 4-stage rectifier are adopted for the CCDD and Dickson topology.

An additional design consideration in improving the PCE performance of the CCDD rectifier can be attributed to the number of stage configuration in the rectifier. As reported in [7], two modular CCDD rectifier connected in parallel achieves higher PCE at low P_{in} compared to a single modular CCDD rectifier. Figure 6 describe the PCE plot for the conventional 4-stage CCDD and two 4-stage modular CCDD in parallel. The plot in Fig. 6 shows a higher peak of PCE can be achieved at lower P_{in} when incorporating two modular CCDD rectifier in parallel. Hence, a CCDD rectifier with a second modular CCDD rectifier (1b, 2b, 3b, and 4b) as shown in Fig. 4(a), connected in parallel with the first modular CCDD rectifier (1a, 2a, 3a, and 4a) is adopted in this work to attain higher PCE performance at low P_{in}.

3.2 Logic control circuit

Figure 7 shows the schematic diagram of the logic control circuit. Two digital inverters cascaded in series forms the logic control switch. Voltage V_{M1} act as the input supply voltage of the inverter cells and V_{M2} being the input signal voltage. A voltage divider that consist of two resistors, R_1 and R_2 establishes a voltage at the gate terminal of the MOSFETs to be lower than V_{M1}. Two control voltages, V_{ctrl1} and V_{ctrl2} are generated with an extreme magnitude (digital LOW and digital HIGH) respectively to the magnitude of V_{M2} to control the operation of the control gates and the rectifiers across the harvesting range, P_{in}.

At low P_{in}, a digital LOW V_{ctrl2} will switch on MP_{S4} where the CCDD rectifier will supply power to the load and a digital HIGH V_{ctrl1} switches off MP_{S3} where the Dickson rectifier does not supply any power to the load (Fig. 2). Therefore, only the CCDD rectifier operates when P_{in} is low. Alternatively, a digital LOW V_{ctrl2} switches on MP_{S2} to maximize the input signal voltage of the logic control circuit. Maximizing the overdrive voltage of MP_{S2} allows the voltage to exceed the MOSFETs' V_{th} at the desired switching point. In addition, a digital LOW V_{ctrl2} partially switches on MN_{S1} to minimize the voltage feed from MN_{S1} to the source terminal limiting the amount of voltage

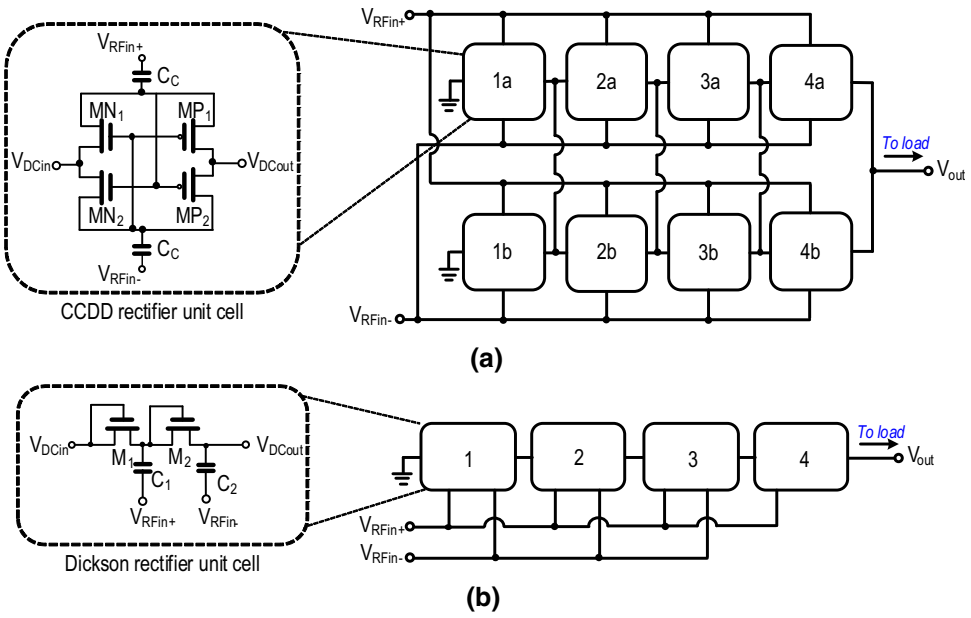

Fig. 4 CMOS rectifier. (**a**) 4-stage parallel CCDD. (**b**) 4-stage Dickson

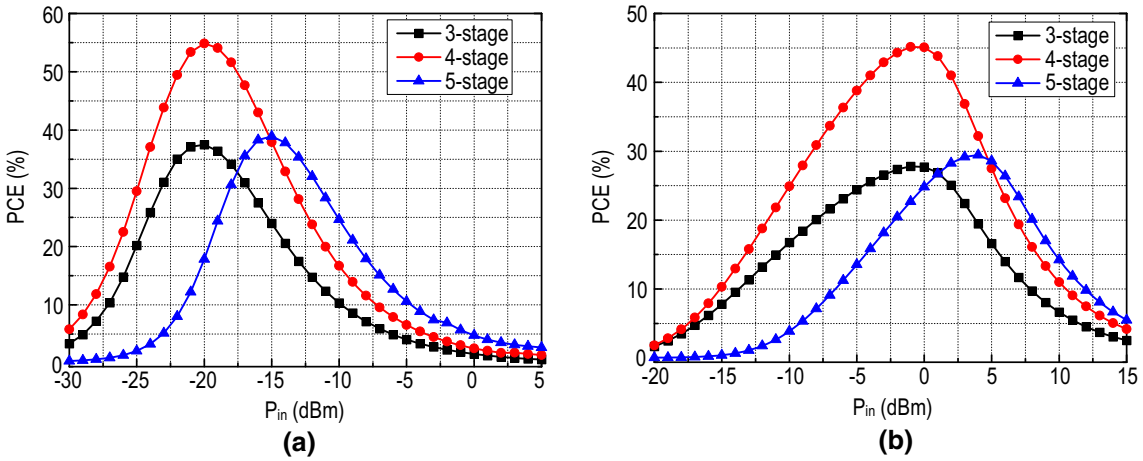

Fig. 5 PCE versus number of stages. (**a**) CCDD. (**b**) Dickson

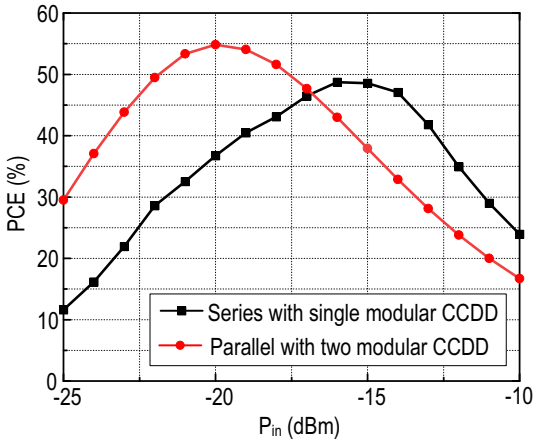

Fig. 6 PCE plot for series single modular CCDD and parallel with two modular CCDD

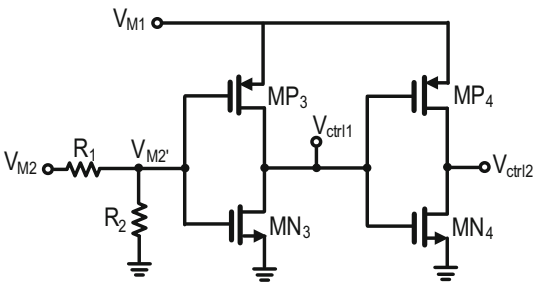

Fig. 7 Schematic diagram of the logic control circuit

necessary to power up logic control circuit. This is to improve the output voltage delivered to the load, thus, upholding the PCE performance.

At high P_{in}, the operation is inversed where the voltage from MP_{S2} into the logic control circuit will be higher than the MOSFETs' V_{th}. This generates a digital LOW control voltage, V_{ctrl1} (with magnitude almost equal to zero) and a digital HIGH control voltage, V_{ctrl2} (with magnitude almost equal to V_{M1}). The digital HIGH V_{ctrl2} switches MP_{S4} off to cut off the power from the CCDD rectifier and the digital LOW V_{ctrl1} switches on MP_{S3} for the Dickson rectifier to supply power to the load. MP_{S2} will be partially switched off to maximize the generation of the digital HIGH control voltage V_{ctrl2} when the input signal voltage into the logic control circuit from MP_{S2} is higher than the MOSFETs' V_{th}. A digital HIGH V_{ctrl2} switches on MN_{S1} to maximize the input supply voltage from MN_{S1} into the logic control circuit to uphold the PCE. Table1 summarizes the operation of logic control circuit.

4 Simulation results

The proposed rectifier is simulated on a 65-nm CMOS technology. The rectifier is optimized for a frequency of 953 MHz and covers an active chip area of 0.657 mm^2 as shown in Fig. 8(a). The equivalent circuit of the RFEH front-end is represented in Fig. 8(b) where $L_{p1,2}$, $C_{p1,2}$ and $R_{p1,2}$ represents the parasitic inductance, capacitance and resistance, respectively. The parasitic components are derived from bond wire inductances, bonding pads and package capacitances and sheet resistance of the polysilicon [13].

Figure 9(a) present the PCE results which show a peak PCE of 47.87% and 54.85% for a load of R_L = 150 kΩ and R_L = 100 kΩ, respectively. Also, the rectifier observes a peak sensitivity of -20.6 dBm from a load of R_L = 100 kΩ. A significant performance of 25 dB and 26 dB in DR (PCE > 20%) was achieved for a load of 150 kΩ and 100 kΩ, respectively. Figure 10 plots the simulated output noise across R_L. Table 2 summarize and compare the performances of the proposed rectifier. The comparison shows that the performance in DR range, peak PCE and sensitivity for similar R_L superseding that of prior-art

Table 1 Operational summary of the rectifier scheme

Input power, P_{in}	V_{M2}	V_{ctrl1}	V_{ctrl2}	MN_{S1}	MP_{S2}	MP_{S3}	MP_{S4}
Low	0	1	0	Partially ON	Fully ON	OFF	ON
High	1	0	1	Fully ON	Partially ON	OFF	ON

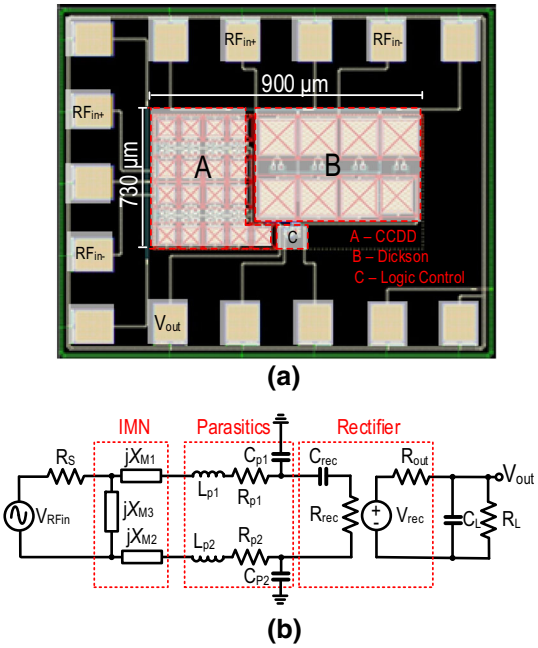

Fig. 8 (**a**) Chip layout of proposed rectifier, (**b**) equivalent circuit of RFEH front-end [6]

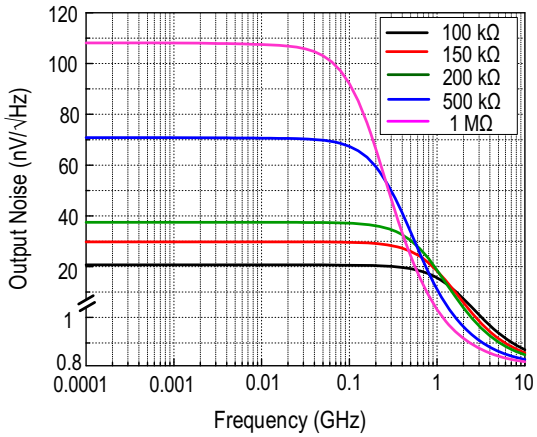

Fig. 10 Simulated output noise across R_L

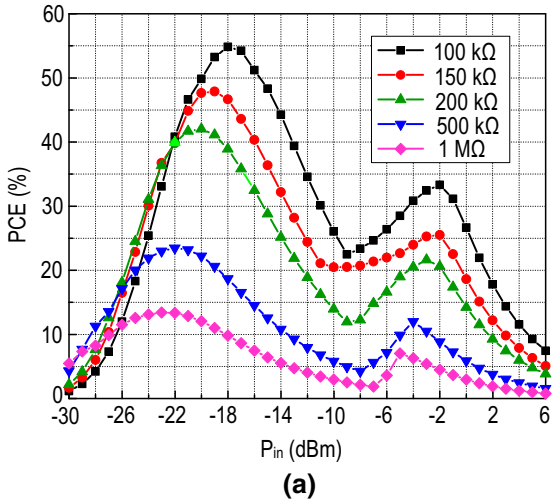

Fig. 9 Simulated results at a frequency of 953 MHz. (**a**) PCE. (**b**) V_{out}

solutions. The proposed rectifier shows a significant enhancement in DR compared to [6, 12] with competitive performance in peak PCE where [6] has adopted similar concept of rectifying the RF energy from two separate path to feed a single load element. In addition, the solution of harvesting RF energy of the same frequency from two individual source of antenna far exceeds that of dual-band CMOS RF rectifiers [8, 9].

5 Conclusion

A dual-input extended-dynamic-PCE rectifier in 65 nm CMOS technology is proposed for dedicated far-field RFEH systems. Exploiting the high-PCE range of the CCDD and Dickson for a given R_L, the proposed system achieved an extended PCE across a wide P_{in} range. A logic

Table 2 Performance summary and comparison with prior-art RFEH rectifiers

	This work[#]		[6]	[11]	[8]	[9]
Technology (nm)	65		65	130	130	180 + IPD
Frequency (MHz)	953		900	900	900/2000	930/2630
Rectifier architecture	Dual-input rectifier		Dual-path rectifier	Self-body-biasing rectifier	Dual-band	Dual-band
Rectifier topology	Dickson/CCDD		CCDD	CCDD	Dickson	Dickson
No. of rectifier stages	4/4		5	3	4/5	–
Load, R_L (kΩ)	150	500	147	100	1500/1000	500
Peak PCE,% @ (P_{in}, dBm)	47.87(−19)	23.48 (−22)	36.5(−10)	80.3(−17)	9.1 (−19.3)/ 8.9(−19)	7(−15.5)
Sensitivity at 1 V, dBm@ (R_L, kΩ)	−20.6(100)		−17.7(∝)	−18.7(100)	−19.3(1500)	−15.5(500)
Dynamic range* (dB)	25	15	11	14.5	–	–
Power consumption of load, R_L (μW)	194.4	60.5	51.45	62.5	0.88/1.10	20
Output noise @ 953 MHz ($nV/\sqrt{Hz}$)	39.12	32.65	n.a	n.a	n.a	n.a

[#]Simulation,*PCE > 20%

control circuit complements the system to passively switch between the rectifiers by sensing the rectified dc voltage. The proposed rectifier achieves an extended DR performance of 26 dB (R_L = 100 kΩ, PCE > 20%), a peak PCE of 54.85% (R_L = 100 kΩ) and a peak sensitivity of -20.6 dBm (R_L = 100 kΩ) for a 1 V output.

Acknowledgement This work was supported by RU Grant-Faculty Program (GPF056B-2020). This manuscript has no associated data.

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