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MIXED SIGNAL LETTER

MSB-split VCM-based charge recovery symmetrical switching with set-and-down asymmetrical switching method for dual-capacitive arrays SAR ADC

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Abstract
With the advanced development of CMOS manufacturing process, the capacitive-array in the successive approximation register analog-to-digital converters (SAR ADCs) has become the dominant source of energy consumption and silicon area. This requires an immediate attention to design a more energy-efficient capacitive switching method while maintaining excellent linearity and noise rejection. A hybrid switching method is proposed for the SAR ADC with dual-capacitive arrays architecture, which consists of MSB-split V_{CM}-based charge recovery symmetrical switching and set-and-down asymmetrical switching methods for the coarse and fine resolution conversions, respectively. As a result, it has achieved 99.53% switching energy reduction and 73.44% area reduction compared to the conventional switching method.

Keywords SAR ADC · V_{CM}-based charge recovery switching · Set-and-down switching · Dual-capacitive array · MSB-split · LSB switching

1 Introduction

Successive approximation register (SAR) analog-to- digital converters (ADCs) have been extensively used for its highly competitive energy-efficiency performances [1]. The advancement in the CMOS manufacturing process has provided a significant benefit in reducing the power consumption and silicon area of the SAR ADCs' control logic, making the capacitive DAC the most costly part in the SAR ADC circuit. Hence, it has become increasingly important to identify the next generation of capacitive DAC architecture with its most optimal switching method.

The capacitive DAC architectures in SAR ADCs can be classified into (1) conventional binary-weighted capacitive array (CBW) [2, 4, 5], (2) conventional binary-weighted split-capacitive array with an attenuation capacitor (BWA) [2, 3, 6–9], and (3) dual-capacitive array (DCA) [10–12]. The differences among these architectures can be summarized into Table 1 according to simulation results and references [2, 3]. The capacitors in the N-bit CBW DAC is a binary-weighted capacitor array ($2^{N-1}C_U$, $2^{N-2}C_U$, $\cdots$, $2C_U$, C_U, C_U) that sums up to 2^NC_U, where C_U represents the unit capacitor [4, 5]. The total number of unit capacitors increases exponentially with the resolution, leading to a significant increase in area, power consumption and settling time that limits the speed and resolution of the SAR ADC [8]. To overcome these problems, BWA DACs use an attenuation capacitor to divide the N-bit capacitive-array DAC into the B-bit MSB sub-array and (N-B)-bit LSB sub-array [2, 3, 6, 7]. The attenuation capacitor is usually a non-integer multiple of the unit capacitor, degrading the accuracy of the DAC due to the finite lithography manufacturing grid and poor matching with other unit capacitors [2, 13]. Attentively, C-2C capacitive-array [14–16] has significantly reduced the total number of unit capacitors but the floating nodes in the capacitive-array can be easily affected by neighbouring electromagnetic (EM) interferences and radiation, thus degrading the linearity of the ADC. Furthermore, in both architectures, the parasitic capacitance will further degrade the linearity of the ADC severely [2, 3]. The SAR ADC with DCA DAC architecture has provided an alternative

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Table 1 Comparison of different architectures for 10-bit SAR ADC

Architecture	MSB:LSB (bit:bit)	σ_{DNL} (LSB)	σ_{INL} (LSB)	Energy ($C_U V_{ref}^2$)	Area (C_U)	Number of capacitors
CBW [2]	10	0.32	0.16	1363.3	2048	11
BWA [2]	5:5	1.81	0.91	87.3	128.1	12
DCA [3]	5:5	0.64	0.23	646.0	2112	13

solution by using a (*S/H*) capacitive-array to sample and quantize the input signal, obtaining the first few bits (coarse resolution). The remaining bits (fine resolution) are obtained through the quantization of the *Main* capacitive array [11]. In this way, the switching energy of first few bits has been significantly reduced compared to CBW DAC [11]. The earlier proposed architectures require more unit capacitors compared to the CBW architecture [10, 11]. Hence, it is important to propose a better switching method with improved DCA architecture, leading to significant savings in power and area without linearity deterioration.

There are several state-of-the-art switching methods to further improve the energy-efficiency of the DCA SAR ADC, such as set-and-down switching method [12, 16, 17], V_{CM}-based charge-recovery switching [11, 18], tri-level switching [19], two-step switching [15, 16, 20, 21] and merge and split switching [15, 22]. These methods have achieved more than 80% reduction in switching energy compared to the conventional charge-redistribution switching [5]. However, these state-of-the-art switching methods come with different design trade-offs. The set-and-down switching method [12, 16, 17] is an asymmetrical switching method, which suffers from poor common-mode noise rejection and linearity. The V_{CM}-based charge-recovery switching [11, 18] and two-step switching [15, 16, 20, 21] require an extra voltage reference compared to the conventional charge-redistribution switching [5] and set-and-down switching method [17]. The two-step switching [15, 16, 20, 21] requires additional control logic to perform intermediate switching. The merge and split switching method [15, 22] connects bottom-plates of the capacitors together to create floating nodes, which allows reuse of the charge. Thus, it has achieved the best energy-efficiency. However, without low-leakage and high linearity switches, the floating nodes in the capacitive-array will lose charge across time, causing severe degradation of linearity [23]. Therefore, to identify a practical and energy-efficient switching method, it is important to consider the design constraints imposed on the DAC, such as total number of unit capacitors, switching energy, linearity, common-mode voltage variations, circuit noise and the influence of parasitic capacitance.

In this work, we explore and propose an improved DCA DAC architecture with optimized switching methods. Two different hybrid switching methods are proposed in the *S/H* and *Main* capacitive arrays, respectively, to optimize the switching energy and linearity. For the *S/H* capacitive arrays, bottom-plate sampling technique and MSB-split V_{CM}-based charge-recovery switching method [18, 24] with "LSB-down" switching technique are used to improve the sampling linearity, minimize V_{CM} variation and alleviate offset requirement for the comparator. Since the input common mode range is within $\pm 1/2^{B+1}$ of the entire dynamic range, V_{FS}, we use set-and-down switching with MSB preset [5] and LSB switching techniques in the *Main* capacitive arrays to further reduce the switching energy and total unit capacitors without degrading the linearity.

The rest of the paper is organized as follows. Section 2 describes the improved DCA DAC architecture used in the proposed SAR ADC. Section 3 presents the proposed switching methods for the DCA DAC. Section 4 analyses performances of the SAR ADC architecture including switching energy, linearity, noise and the influence of parasitic capacitance. Section 5 compares and discusses our proposed work with the state-of-the-art switching methods. Finally, conclusions are drawn in Sect. 6.

2 Proposed dual-capacitive array (DCA) SAR ADC architecture

Similar to our previous work [11], a fully differential architecture is adopted as it is less susceptible to supply and substrate noises, and increases the range of input signal with a good common-mode noise rejection. As shown in Fig. 1, the dual-capacitive arrays architecture consists of a pair of *B*-bit *S/H* capacitive arrays and (*N*-*B*)-bit *Main* capacitive arrays. The *S/H* capacitive array can be broken down into a *MaSB* capacitive sub-array ($C_{a,1}$, $C_{a,2}$, $\cdots$, $C_{a,B-2}$) and a *MiSB* capacitive sub-array (C_1, C_2, $\cdots$, C_{B-2}), both consisting of *B*-2 capacitors. According to Fig. 1, capacitors in the *S/H* capacitive arrays are calculated as follows:

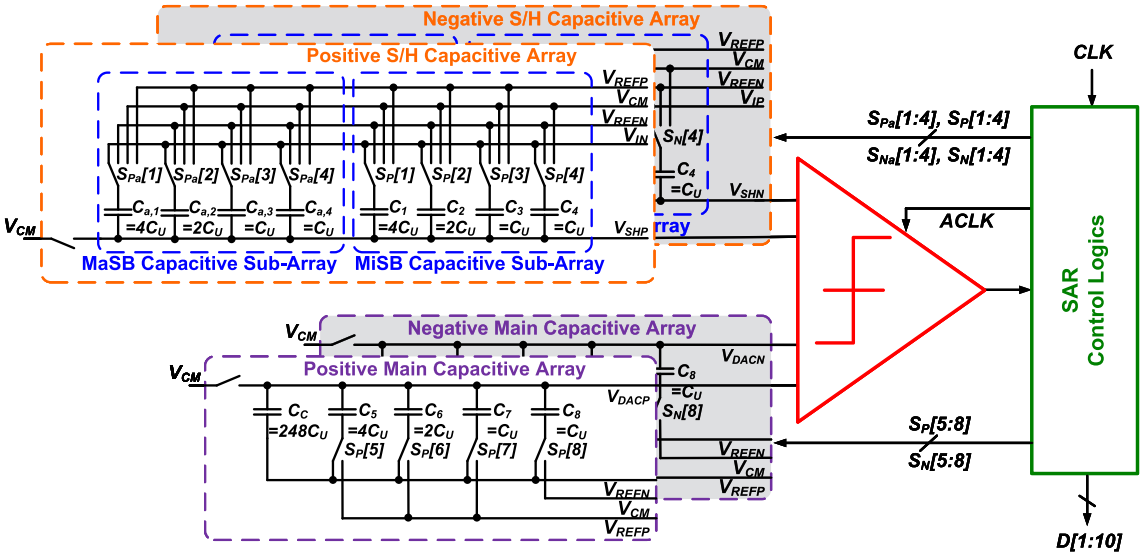

Fig. 1 An example of our proposed 10-bit DCA SAR ADC

$$C_j = C_{a,j} = \begin{cases} 2^{B-j-3}C_U, 1 \leqslant j \leqslant B-3 \\ C_U, \qquad\quad j = B-2 \end{cases} \tag{1}$$

The *Main* capacitive array is made up of a (*N*-*B*)-bit binary-weighted capacitive array (C_{B-1}, C_B, $\cdots$, C_{N+B-9}) and a compensation capacitor C_C. As shown in Fig. 1, the capacitors in the *Main* capacitive arrays are calculated as follows:

$$C_j = \begin{cases} 2^{N-j-3}C_U, \qquad B-1 \leqslant j \leqslant N-3 \\ C_j = C_U, \qquad j = N-2 \end{cases} \tag{2}$$

$$C_C = \left(2^{N-2} - 2^{N-B-1}\right)C_U. \tag{3}$$

The total number of unit capacitors for the proposed differential SAR ADC is:

$$\begin{aligned} C_{total} &= 2\left(C_C + \sum_{j=1}^{B-2} C_{a,j} + \sum_{j=1}^{N-2} C_j\right) \\ &= \left(2^{N-1} + 2^{B-1}\right)C_U. \end{aligned} \tag{4}$$

Consider a 10-bit differential SAR ADC as an example, the *S/H* and *Main* capacitive arrays contain a total capacitance of $16C_U$ and $256C_U$, resulting $544C_U$ in total.

3 Proposed switching methods

The proposed switching method is summarized in the flowchart, as shown in Fig. 2. The whole working procedure of the proposed SAR ADC can be divided into three

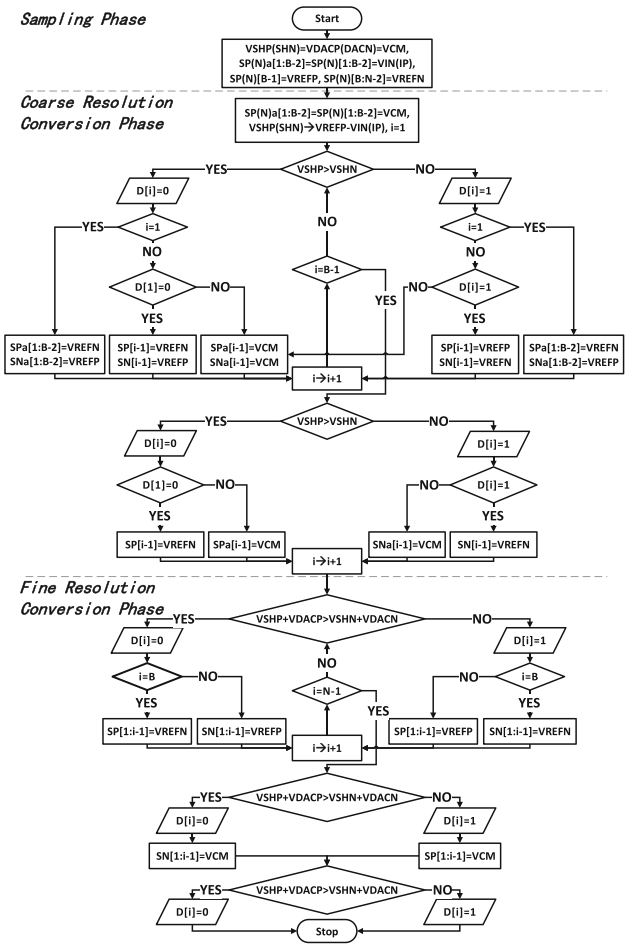

Fig. 2 Flow chart of the proposed switching method

phases: (1) the sampling phase, (2) the coarse resolution conversion phase, and (3) the fine resolution conversion phase. The first two phases are performed on the *S/H* capacitive arrays and the last phase is performed on the *Main* capacitive arrays.

3.1 Sampling phase

For simplicity, a 4-bit SAR ADC is used as an example to illustrate the sampling phase and the coarse resolution conversion phase, as shown in Figs. 3 and 4, where V_{ref} refers to $V_{REFP} - V_{REFN}$. During the sampling phase, the differential analog signal V_{IP} and V_{IN} are sampled to bottom plates of the capacitors in the *S/H* capacitive arrays, whereas the top plates of capacitors are connected to common mode voltage, V_{CM} using the *S/H* switches, as shown in Fig. 3. Bottom plate sampling technique is used to avoid additional parasitic capacitance from the *S/H* switches, so as to minimize the effect of channel charge injection and improve switching linearity [25]. This technique also improves the ADC's harmonic distortions as compared to the top-plate sampling technique [25]. V_{CM} is sampled to the top plates of the capacitors in both positive and negative *Main* capacitive arrays.

3.2 Coarse resolution conversion phase

The hybrid switching method used in the coarse resolution conversion combines the charge recovery switching method [18], the MSB-split technique [24] and "LSB-down" switching technique [26]. After the sampling phase, the *S/H* switches are switched off and the first conversion is carried out without energy consumption. If $V_{SHP} < V_{SHN}$, output $D(:,1) = 1$, capacitors in positive *MaSB* capacitive array are switched to V_{REFP} and capacitors in negative *MaSB* capacitive array are switched to V_{REFN}. In the subsequent *B-3* bit cycles, the capacitor C_j $(1 \leqslant j \leqslant B-3)$ in positive *MiSB* capacitive array is switched to V_{REFP} and that in negative *MiSB* capacitive array is switched to V_{REFN} every time $V_{SHP} < V_{SHN}$. C_j $(1 \leqslant j \leqslant B-3)$ in the both *MaSB* capacitive arrays are switched back to V_{CM} every time $V_{SHP} > V_{SHN}$. During the $(B\text{-}1)$-th conversion, "LSB-down" switching is introduced as shown in Fig. 4, decreasing V_{SHP} (V_{SHN}) by $1/2^{B-1}$ of the entire dynamic range, V_{FS}, when $D(:,1) = 0$ $(D(:,1) = 1)$ [26].

There are several advantages of the proposed hybrid switching method for coarse resolution conversion. (1) The conversion process of the V_{CM}-based charge recovery switching method corresponds to a compensation of the charge transferred to the positive *S/H* capacitive array with charge coming from the negative *S/H* capacitive array and vice-versa [18], reducing the switching energy by 87.5% compared to the conventional switching method [27]. (2) Furthermore, the MSB capacitor in the *S/H* capacitive array (C_0) is split into a *MaSB* sub-array [24]:

$$C_0 = \sum_{j=1}^{B-2} C_{a,j}. \tag{5}$$

With the MSB-split technique, a 37% energy saving of the coarse quantized steps can be achieved by reducing power dissipation in a "down" transition. (3) During the initial conversion, it is important to adopt symmetrical switching method, minimizing common mode variations [18]. It is justifiable to use the "LSB-down" switching technique (an asymmetrical switching method) in the last bit conversion

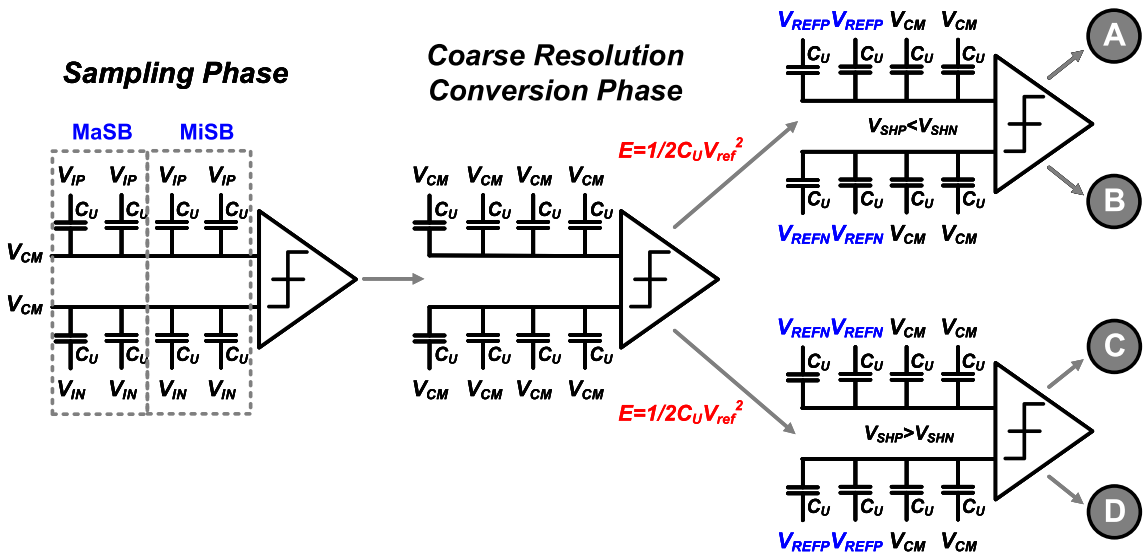

Fig. 3 The first two conversion steps of our proposed coarse resolution conversion using 4-bit ADC

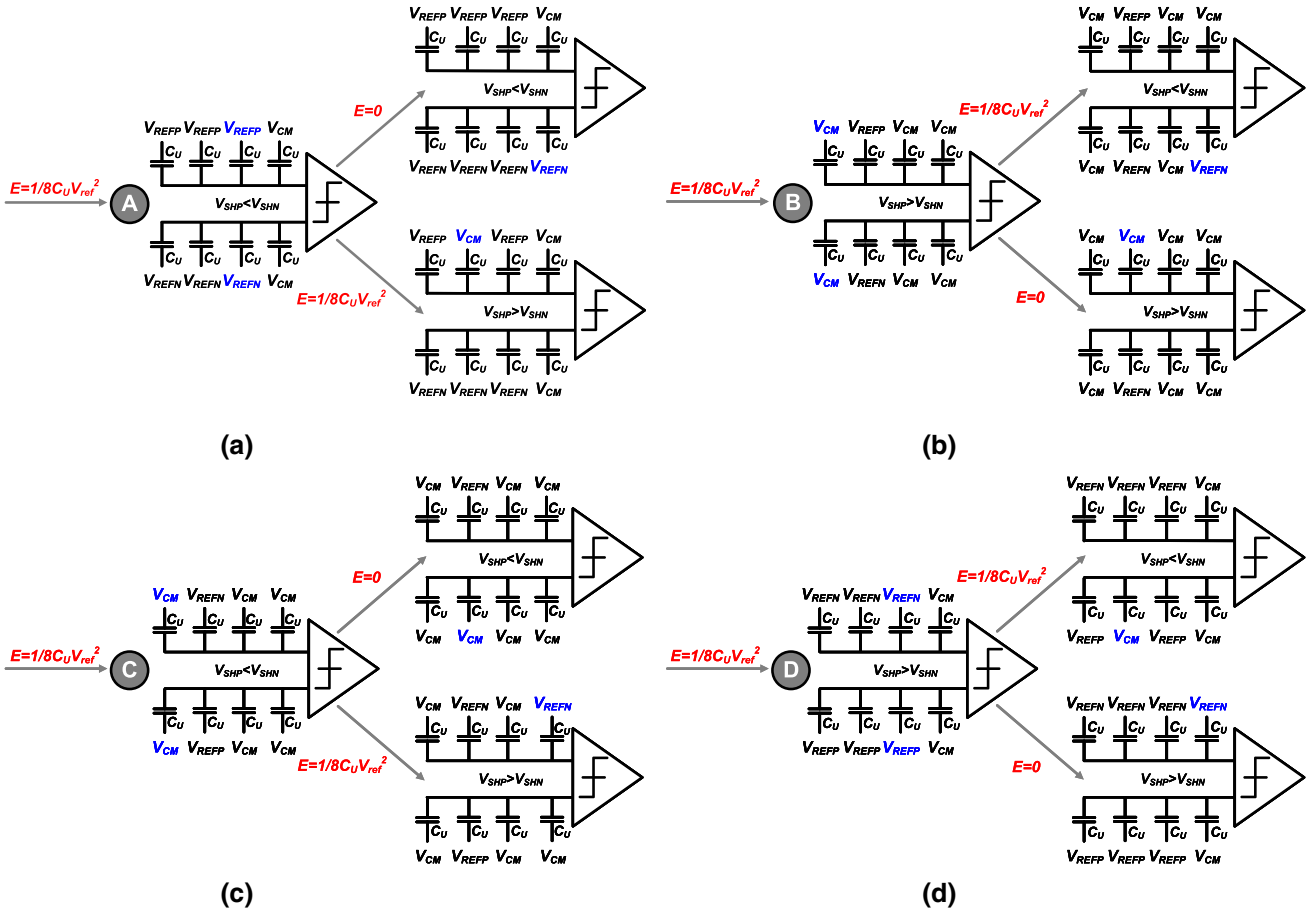

Fig. 4 The last two conversion steps of our proposed coarse resolution conversion using 4-bit ADC

since the dynamic range has reduced from full scale to $\pm 1/2^B\ V_{FS}$, which further reduces the charge transfer in the DAC and the switching transitions of the control circuit and switch buffer [12]. Therefore, the proposed architecture achieves a 6-bit output with a 4-bit *S/H* capacitive array, reducing the total number of unit capacitors and energy consumption. There is a marginal degradation in the linearity since the asymmetrical switching happens only at LSB capacitor.

3.3 Fine resolution conversion phase

With the reduction in the input dynamic range after the coarse conversion phase, the set-and-down switching method (an asymmetrical method) [12, 17] with MSB preset [5] and LSB switching [12] techniques is proposed for fine resolution conversion, which can further reduce the switching energy compared to the charge recovery switching. As illustrated in Fig. 5, bottom plate of the MSB capacitior C_{B-1} is set to V_{REFP} while the remaining capacitors are set to and V_{REFN} before commencing the fine resolution conversion phase [12]. The output of the last comparison bit of coarse resolution steps is used to determine the first conversion of *Main* capacitive array. If V_{SHP} is higher than V_{SHN}, bottom plate of the corresponding capacitor is switched to V_{REFN} and vice versa. From the (B+1)-th to (N-2)-th resolution conversions, the corresponding capacitor C_j $(B \leqslant j \leqslant N-2)$ in the positive *Main* capacitive array is switched from V_{REFN} to V_{REFP} when $V_{SHP} + V_{DACP} < V_{SHN} + V_{DACN}$ $(D(:,j) = 1)$, as shown in Fig. 6a, c. The bottom-plate connection of the corresponding capacitor C_j $(B \leqslant j \leqslant N-2)$ in the negative *Main* capacitive array is switched instead when $V_{SHP} + V_{DACP} > V_{SHN} + V_{DACN}$ $(D(:,j) = 0)$, as shown in Fig. 6b, d. For the LSB conversion, the level-shift is generated through switching the terminal capacitor C_{N-2} to the reference common mode voltage V_{CM} [12].

We have considered the following design constraints for *Main* capacitive arrays: (1) There is no dominant mismatch and non-linearity caused by the set-and-down switching method since the input common mode range is within $\pm 1/2^{B+1}$ of the entire dynamic range, V_{FS}. The top-plate sampling technique does not consume any energy from the reference voltages, V_{REFP} and V_{CM} [28]. Furthermore, one third of the switches are saved

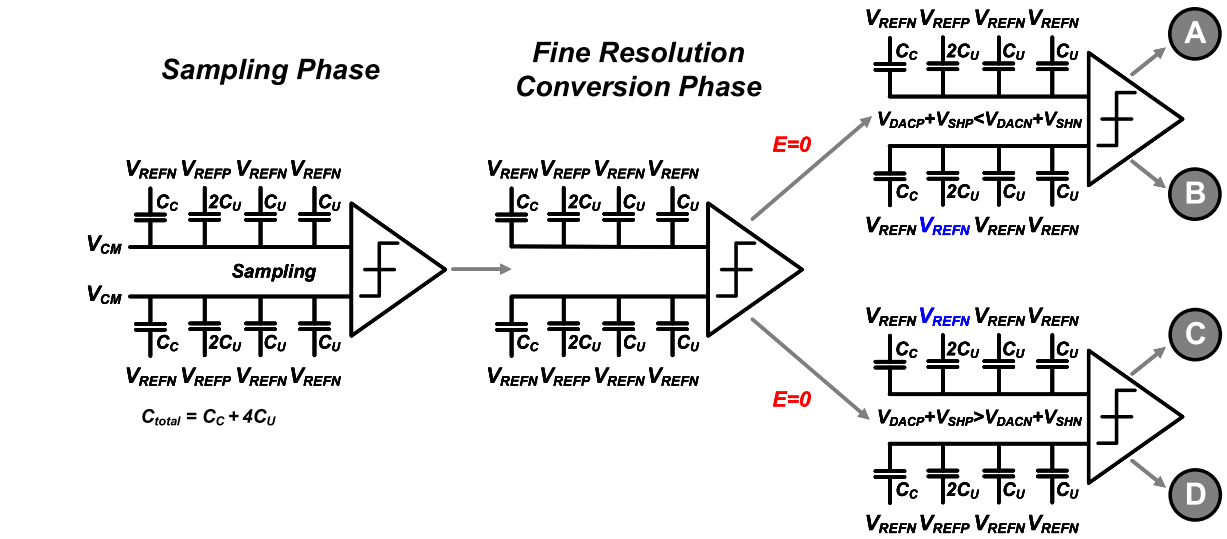

Fig. 5 The first two conversion steps of our proposed fine resolution conversion using 4-bit ADC

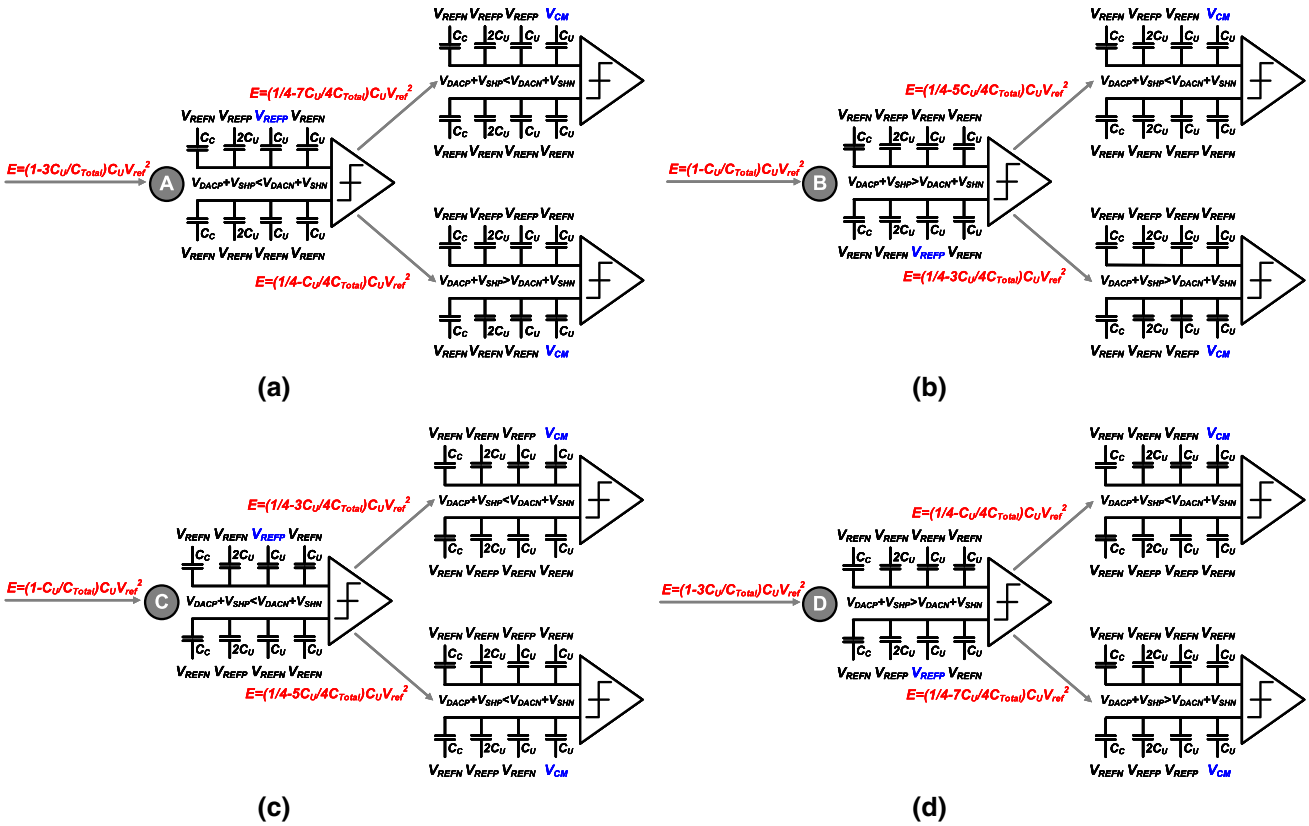

Fig. 6 The last two conversion steps of our proposed fine resolution conversion using 4-bit ADC

compared to bottom-plate sampling, relieving the parasitic effects and adverse impacts on the input voltage range of the SAR ADC, which also saves chip area [28]. (2) During the sampling phase, all the bottom plates are reset to the reference voltage, V_{REFN} except for that of the MSB capacitor, which is reset to reference voltage, V_{REFP}. This technique allows the DAC to achieve a full-scale fast sampling time without using extra reset switching phase [5]. (3) The LSB switching technique further reduced area and power consumption, which is similar to "LSB-down" switching used in the *S/H* capacitive arrays [12].

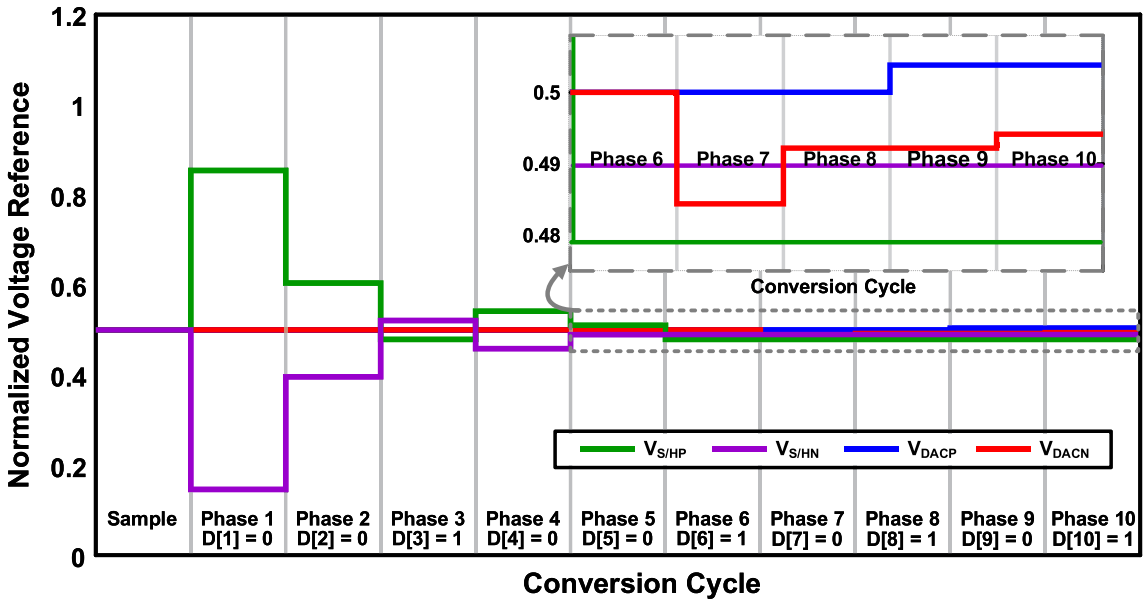

Fig. 7 Transient waveform of our proposed hybrid switching method

Figure 7 provides an example waveform of the proposed switching methods.

4 SAR ADC performance analysis

The performance analysis of our proposed architecture and switching methods are presented. The DAC's switching energy, linearity, common-mode voltage variation and noise are discussed based on N=10 and B=6 unless otherwise specified.

4.1 DAC's switching energy analysis

To derive the switching energy of our proposed method, the analysis can be broken down into the coarse and fine resolution conversion phases. During the coarse resolution conversion phase, the output voltage from the *S/H* capacitive array changes from $V_{SHP(N)}(i,j)$ to $V_{SHP(N)}(i,j+1)$, where i and j are input level and conversion step, respectively. The voltage changes during the conversion is given by:

$$V_{SHP}(i,j+1) - V_{SHP}(i,j) = \begin{cases} \left(D(i,j) - \overline{D(i,j)}\right)\frac{V_{ref}}{2^{j+1}}, & 1 \leqslant j \leqslant B-2 \\ -\overline{D(i,j)}\frac{V_{ref}}{2^{j}}, & j = B-1 \end{cases} \quad (6)$$

$$V_{SHN}(i,j+1) - V_{SHN}(i,j) = \begin{cases} \left(\overline{D(i,j)} - D(i,j)\right)\frac{V_{ref}}{2^{j+1}}, & 1 \leqslant j \leqslant B-2 \\ -D(i,j)\frac{V_{ref}}{2^{j}}, & j = B-1 \end{cases} \quad (7)$$

Given the initial condition:

$$V_{SHP(N)}(i,1) = V_{IP(N)}, \quad (8)$$

$V_{SHP(N)}(i,j)$ can be calculated as:

$$V_{SHP}(i,j) = V_{IP} + \sum_{k=1}^{j-1}\left(D(i,k) - \overline{D(i,k)}\right)\frac{V_{ref}}{2^{k+1}}, \quad (9)$$

$$V_{SHN}(i,j) = V_{IN} + \sum_{k=1}^{j-1}\left(\overline{D(i,k)} - D(i,k)\right)\frac{V_{ref}}{2^{k+1}}. \quad (10)$$

During the fine resolution conversion phase, the comparator's input has changed from $V_{SHP(N)}(i,j) + V_{DACP(N)}(i,j)$ to $V_{SHP(N)}(i,j+1) + V_{DACP(N)}(i,j+1)$ in the j-th conversion. Since $V_{SHP(N)}(i,j)$ remains unchanged, the voltage level-shift at each clock cycle is given by:

$$V_{DACP}(i,j+1) - V_{DACP}(i,j) = \begin{cases} -\overline{D(i,j)}\frac{V_{ref}}{2^{j}}, & j = B \\ D(i,j)\frac{V_{ref}}{2^{j}}, & B+1 \leqslant j \leqslant N-1 \end{cases} \quad (11)$$

$$V_{DACN}(i,j+1) - V_{DACN}(i,j) = \begin{cases} -D(i,j)\frac{V_{ref}}{2^j}, & j = B \\ \overline{D(i,j)}\frac{V_{ref}}{2^j}, & B+1 \leqslant j \leqslant N-1 \end{cases} \quad (12)$$

Given the initial condition that:

$$V_{DACP(N)}(i,j) = V_{CM} 1 \leqslant j \leqslant B, \quad (13)$$

$V_{DAC}(i,j)$ can be calculated as:

$$V_{DACP}(i,j) = V_{CM} - \overline{D(i,6)}\frac{V_{ref}}{2^6} + \sum_{k=B+1}^{j-1} D(i,k)\frac{V_{ref}}{2^k}, \quad (14)$$

$$V_{DACN}(i,j) = V_{CM} - D(i,6)\frac{V_{ref}}{2^6} + \sum_{k=B+1}^{j-1} \overline{D(i,k)}\frac{V_{ref}}{2^k}, \quad (15)$$

where $B+1 \leqslant j \leqslant N$.

The total charge, $Q_{i,j}$, calculated on the *S/H* capacitive array in the j-th conversion is:

$$\begin{aligned} Q_{i,j} = {} & D(i,1)\{[C_0 + \sum_{k=2}^{j}\left(D(i,k) - \overline{D(i,k)}\right)C_{k-1}]\cdot \\ & (V_{SHP}(i,j) - V_{SHP}(i,j+1)) + D(i,j)\cdot C_{j-1}V_{CM}\} \\ & + \overline{D(i,1)}\{[C_0 + \sum_{k=2}^{j}\left(\overline{D(i,k)} - D(i,k)\right)C_{k-1}]\cdot \\ & (V_{SHN}(i,j) - V_{SHN}(i,j+1)) + \overline{D(i,j)}\cdot C_{j-1}V_{CM}\}, \end{aligned} \quad (16)$$

where $1 \leqslant j \leqslant B-2$. When j = B-1, the average charge is basically negligible in estimating the total switching energy for C_{B-2} ($C_{a,B-2}$) is as small as C_U.

The MSB preset technique used during the B-th conversion does not consume any energy in the *Main* capacitive array [12]. From *(B+1)* to *(N-2)*-th conversions, the total charge that V_{REFP} supplies to the *Main* capacitive array in the j-th conversion $Q_{i,j}$ can be calculated as:

$$\begin{aligned} Q_{i,j} = {} & (\sum_{k=1}^{j-1} D(i,k)C_{k-1} \\ & + C_{j-1})(V_{DACP}(i,j) - V_{DACP}(i,j+1)) \\ & + (\sum_{k=1}^{j-1} \overline{D(i,k)}C_{k-1} \\ & + C_{j-1})(V_{DACN}(i,j) - V_{DACN}(i,j+1)) \\ & + C_{j-1}V_{ref}, \end{aligned} \quad (17)$$

where $B \leqslant j \leqslant N-2$.

The average charge for LSB switching is neglected in the estimation. Consequently, the average switching energy of the proposed 10-bit differential SAR ADC is:

$$\begin{aligned} E_{average} = {} & \frac{1}{2^N}\sum_{i=1}^{2^N}\sum_{j=1}^{N-1} Q_{i,j}V_{ref} \\ = {} & \sum_{j=1}^{B-2}\frac{1}{2^2}C_{j-1}V_{ref}^2 - \sum_{j=2}^{B-2}\frac{1}{2^{j+1}}C_{j-1}V_{ref}^2 \\ & + \sum_{j=B+1}^{N-2}\left(C_{j-1}V_{ref}^2 + \frac{1}{2^{j+2}}\sum_{k=B}^{j-1}C_{k-1}V_{ref}^2\right) \\ \approx {} & 6.10C_UV_{ref}^2. \end{aligned} \quad (18)$$

We have constructed the model in MATLAB to validate our theoretical calculation. The simulated average switching energy is $6.35C_UV_{ref}^2$, which achieves a 99.53% reduction compared to the conventional method [2].

It is important to consider the switching energy for the ADC's reset phase to account for the overall energy evaluation [24]. The energy required during the reset phase mainly depends on the state of the capacitor matrix at the end of the last conversion period [16]. According to the analysis on V_{CM}-based charge recovery switching method [18], the switching energy required to reset of the *S/H* capacitive array is zero energy on average. The energy required during the reset phase for the *Main* capacitive arrays is:

$$\begin{aligned} E_{reset,average} = {} & \frac{1}{2^N} \\ & \sum_{i=1}^{2^N}[4C_UV_{ref}(V_{DACP}(i,10) + V_{DACN}(i,10) \\ & + V_{ref}) - (C_{DPi} + C_{DNi})V_{ref}^2] \\ = {} & \left(1 - \frac{1}{2^7}\right)C_UV_{ref}^2, \end{aligned} \quad (19)$$

where C_{DPi} and C_{DNi} represent the capacitors connected to V_{REFP} and V_{REFN} after LSB output, respectively. Hence, the average reset switching energy is estimated to be $0.99C_UVref^2$.

4.2 Influence of parasitic capacitance

The parasitic capacitance in the *S/H* and *Main* capacitive arrays degrades the energy efficiency and linearity of the ADC; thus, it is important to understand how it impacts on our proposed architecture [16]. Based on Ref. [8], we assume that the parasitic capacitance amount to 5% and 10% at the top and bottom plates of unit capacitor,

respectively. Considering the influence of top-plate parasitic capacitance, the total charge that V_{REFP} supplies to the *S/H* capacitive array after the *j*-th conversion in the coarse resolution conversion phase:

$$\begin{aligned} Q_{TPi,j} &= 1.05C_{Ai,j}(V_{SH}(i,j) - V_{SH}(i,j+1)) \\ &\quad + 1.05C_{j-1}\left[D_{i,j} - \left(\sim D_{i,j}\right)\right]\cdot \\ &\quad (V_{SH}(i,j) - V_{SH}(i,j+1)) \\ &\quad + D_{i,j}\cdot 1.05C_{j-1}V_{CM}, \end{aligned} \tag{20}$$

where $1 \leqslant j \leqslant B-2$. The modified charge from V_{REFP} in the fine resolution conversion phase is given by:

$$\begin{aligned} Q_{TPi,j} &= 1.05C_{j-1}V_{ref} \\ &\quad + 1.05C_{j-1}\left(V_{DACi,j} - V_{DACi,j+1}\right) \\ &\quad + \left[D_{i,j}1.05C_{BPi,j} + \left(\sim D_{i,j}1.05C_{BNi,j}\right)\right]\cdot \\ &\quad (V_{DACi,j} - V_{DACi,j+1}), \end{aligned} \tag{21}$$

where $B+1 \leqslant j \leqslant N-2$. Through our observations in Eq. (16) and (17), the total capacitance and charge are approximately multiplied by 1.05. Thus, we can roughly estimate that the average switching energy with parasitic capacitance, $E_{parasitic,average}$ to be:

$$\begin{aligned} E_{parasitic,average} &= 1.05E_{average} + 1.1C_UV_{ref}^2 \\ &\approx 7.51C_UV_{ref}^2. \end{aligned} \tag{22}$$

To validate our theoretical calculation, we have constructed another model in MATLAB and obtained a value of $7.79C_UV_{ref}^2$ for a 10-bit SAR ADC. The parasitic capacitance accounts for 2.01% in the total switching energy. The proposed switching method still achieves a power reduction of 99.52% compared to the conventional method [2].

4.3 Linearity analysis

Since the proposed switching method determines MSB without conversion, the worst DNL occurs at 1/4 V_{FS} and 3/4 V_{FS} [29]. Assuming that each unit capacitor follows a random Gaussian distribution with a standard deviation of σ_0, the standard deviations of the maximum DNL and INL are given by [29]:

$$\sigma_{DNL,MAX} = \frac{\sqrt{2^{2N-B-1}}\sigma_0}{C_U}, \tag{23}$$

$$\sigma_{INL,MAX} = \frac{\sqrt{2^{2N-B-2}+2^{N-B-1}}\sigma_0}{C_U}. \tag{24}$$

To validate our theoretical calculation on the DNL and INL of the capacitive array, a total of 5,000 Monte-Carlo simulation runs are performed with $\sigma_0 = 1\%$. The differential and integral non-linearity (DNL, INL) distribution versus different output codes results are presented in Fig. 8. The maximum DNL and INL are 0.416-LSB and 0.254-LSB, which appear on the 255 and 858 output codes, respectively.

4.4 Common-mode (CM) voltage variation analysis

Even though a fully differential architecture is able to suppress supply voltage noise and improve the common-mode noise rejection [30], the variations in V_{CM} and the V_{REFP} voltages can not be ignored [30]. To understand these effects, we assume that the V_{CM} and the V_{REFP} voltages are two independent random Gaussian distributions. A total of 800,000 Monte-Carlo simulation runs are performed with a set of standard deviations ranging from 0.5%, 1%, 2% and 5%. We have also randomized the frequency of input signal, ranging from near DC to the ADC's bandwidth. As a result, as shown in Fig 9, the 10-bit ADC is able to achieve an average ENOB of above 9-bit with variation up to 2%.

4.5 Noise analysis

A statistical modeling for calculating the total input-referred noise σ_{total}^2 of the proposed SAR ADC can be described as follows [31]:

$$\sigma_{total}^2 = \sigma_{thermal}^2 + \sigma_{comp}^2 + \sigma_{quantization}^2, \tag{25}$$

where $\sigma_{thermal}^2$ is the thermal noise from capacitor arrays, σ_{comp}^2 is the input-referred noise from the comparator, and $\sigma_{quantization}^2$ is the quantization noise.

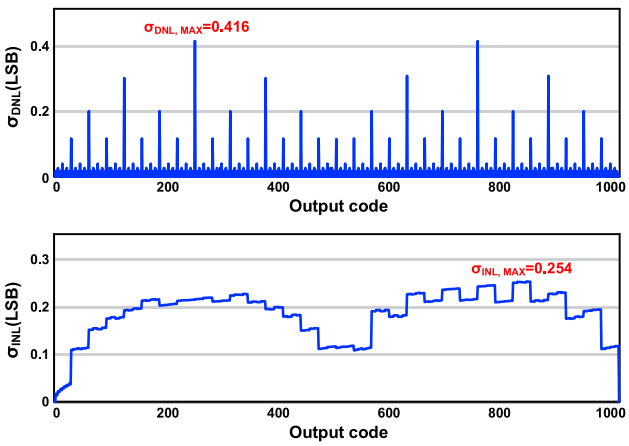

Fig. 8 DNL/INL against output code

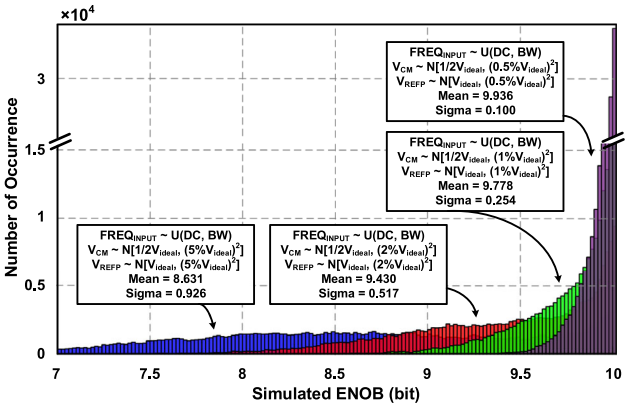

Fig. 9 Effective Number of Bits (ENOB) with supply noise and common-mode voltage variation

The proposed switching method reduces the total input capacitance to $544C_U$, which is a reduction of 73.4% compared with the conventional switching method [2]. However, this leads to an increase in thermal noise for our proposed architecture. The value of an unit capacitor is set to 10fF to calculate $\sigma^2_{thermal}$ [30]. The calculation of $\sigma_{thermal}$ can be described as follows:

$$\begin{aligned}\sigma_{thermal} &= \sqrt{\sigma^2_{S/H,thermal} + \sigma^2_{MAIN,thermal}} \\ &= \sqrt{\frac{KT}{C_{S/H,total}} + \frac{KT}{C_{MAIN,total}}},\end{aligned} \tag{26}$$

where K and T are the Boltzmann constant of 1.380649×10^{-23}J/K and the temperature is 300K, respectively. The total capacitance of the *S/H* and *Main* capacitive DAC arrays are 320fF and 5120fF, respectively. Hence, the $\sigma_{thermal}$ of our proposed switching methods are estimated to be 0.117mV.

The intrinsic capacitance of the comparator is often around 10fF in a typical design [30], so σ_{comp} of the proposed SAR ADC is estimated to be [32]:

$$\sigma_{comp} = \sqrt{\frac{KT}{C_{comp}}} \approx 0.643mV. \tag{27}$$

In a 10-bit SAR ADC with reference voltage of 1V, the quantization noise $\sigma_{quantization}$ is calculated as:

$$LSB = \frac{1}{2^{10}} \approx 0.977mV, \tag{28}$$

$$\sigma_{quantization} = \sqrt{\frac{LSB^2}{12}} \approx 0.282mV. \tag{29}$$

Based on Eq. (25), the total input-referred noise σ_{total} of the proposed SAR ADC is approximately $0.712mV$. As shown in Fig. 10, the noise contributions in the proposed SAR ADC are broken down into thermal, comparator and quantization noise, which approximately account for 6.94%, 85.01% and 8.05%, respectively. With the use of the proposed method, the unit capacitance can be further increased to match with the thermal noise especially when the design is employed in high resolution SAR ADCs which are typically limited by thermal noise [1]. This eases the implementation challenges involving the fabrication of super small capacitors in CMOS process [32].

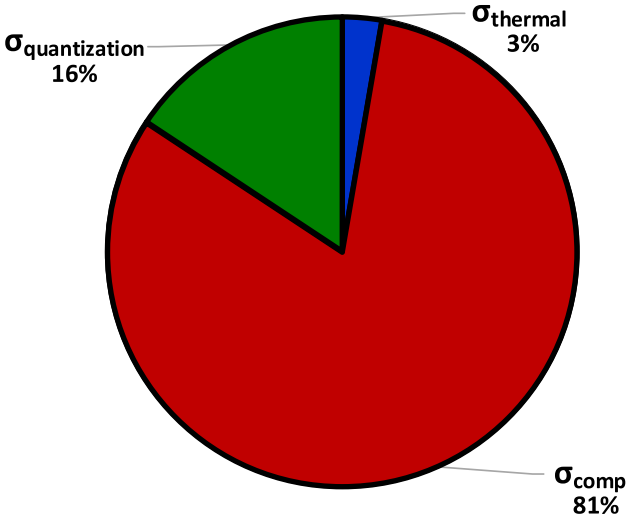

Fig. 10 Noise contributions in proposed SAR ADC

5 Comparison and discussion

Figure 11 illustrates the switching energy versus output code of the proposed hybrid switching method and the state-of-the-art switching methods. Table 2 summarises the average switching energy, reset energy, area and linearity for our proposed method and the state-of-the-art methods. The average switching energy of the proposed method is

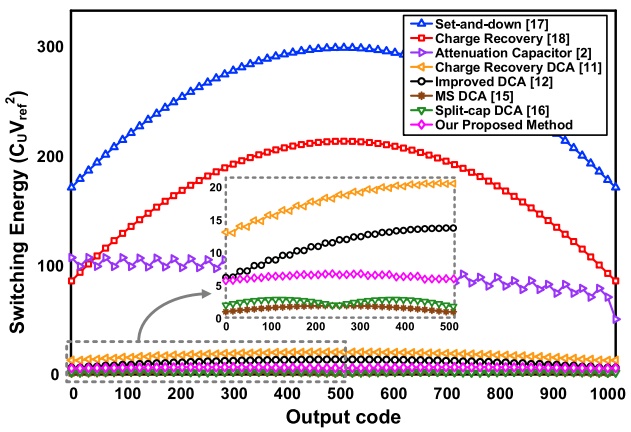

Fig. 11 Switching energy against output code

Table 2 Comparison of switching methods for 10-bit SAR ADC

Switching method	Year	Switching energy ($C_U V_{ref}^2$)	Energy saving (%)	Reset energy ($C_U V_{ref}^2$)	Total capacitance (C_U)	Area reduction (%)	σ_{DNL} (LSB)	σ_{INL} (LSB)	Float node
Conventional [2]	-	1363.3	reference	0	2048	reference	0.320	0.160	N
DCA [10]	2009	646.0	52.6	0	2112	− 3.1	0.64*	0.23*	N
Set-and-down [17]	2010	255.5	81.2	0	1024	50.0	N/A	N/A	N
Charge-recovery [18]	2010	170.2	87.5	0	1024	50.0	0.152	0.151	N
Tri-level [19]	2012	42.4	96.9	0	512	75.0	N/A	N/A	N
Charge-recovery DCA [11]	2013	17.6	98.7	0	1088	46.9	N/A	N/A	N
Improved DCA [12]	2016	10.2	99.3	1.7*	576	71.9	N/A	N/A	N
Vcm-based MS C-2C DCA [15]	2017	1.38	99.9	N/A	390	80.9	0.446	0.426	Y
Split-Cap C-2C DCA [16]	2019	2.14	99.8	0	320	84.4	0.234	0.281	Y
Our Proposed Method	**2020**	**6.35**	**99.5**	**1.0**	**544**	**73.4**	**0.416**	**0.254**	**N**

*: Not direct reference

$6.35CV_{ref}^2$, which achieves a 99.53% reduction in the switching energy compared with the conventional architecture [2]. In addition, our proposed architecture has achieved the area reduction of 73.44%.

The use of floating node switching technique severely degrades the linearity of the SAR ADC when applied to real circuits [15, 16]. Compared with the similar DCA SAR architectures without floating nodes [10–12], our proposed work has achieved the lowest switching energy. Furthermore, required additional control logic and conversion cycle for two-step switching method [15, 16, 20, 21] is avoided. Limited common mode variation is also achieved compared to the fully asymmetrical switching method [12, 16].

6 Conclusion

This paper presents a hybrid switching method to the dual-capacitive arrays SAR ADC. The MSB-split V_{CM}-based charge recovery symmetrical switching method with "LSB-down" and bottom-plate sampling techniques are applied to the *S/H* capacitive arrays [24, 26, 27]. The set-and-down asymmetrical switching method with LSB switching technique are applied to the *Main* capacitive arrays. The proposed switching methods consider the design trade-offs between the total number of unit capacitors, switching energy, linearity, common-mode voltage variations, circuit noise and the influence of parasitic capacitance, leading to good balance of switching energy, area and linearity. The proposed technique has improved the switching energy by 99.53% along with reducing the DAC capacitive array size by 73.44% compared to the conventional architecture [2].

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