



Low power and write-enhancement RHBD 12T SRAM cell for aerospace applications

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Received: 21 November 2019 / Revised: 30 November 2020 / Accepted: 12 December 2020 / Published online: 7 January 2021
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Abstract

In aerospace applications, the conventional Static Random Access Memories (SRAMs) are facing high soft error problems like a single event upset. Several radiation-hardened based design (RHBD) like twelve-transistor (12T) Dice, 12T We-Quatro SRAM cells, etc., had been developed to address the soft error problems. But they all are consuming comparatively more total and static power with more delay and area. The 10T SRAM cell had been developed to reduce the power dissipation and area overhead. But the analysis of 10T cell shows a write failure at high-frequency. An RHBD 12T SRAM cell has been proposed in this paper. The proposed 12T SRAM cell consumes less total, and static power dissipation compared to 12T We-Quatro and 12T Dice cell, respectively. The critical charge and hold noise margin of the proposed SRAM cell have been improved compared to We-Quatro and Dice cell. The simulated result shows that the proposed SRAM cell has provided the less and comparable area, high write speed, and good writability under process variations. Finally, the Monte Carlo Simulation of SRAM cells under 45 nm CMOS technology validates the efficiency of the 12T proposed cell.

Keywords Radiation-hardened SRAM · Static power · Dynamic power · Soft error resilience · Writability

1 Introduction

IN various aerospace electronic systems, the SRAMs are widely used for storing the values. The impact of process variation for sub-100 nm technology affects stability and other parameters of SRAM cells [1–3]. The main parameters to consider for SRAM cells in aerospace applications are the delay, power consumption, soft error rate, and the area [4–6]. The SRAM cells occupy a large area in the system on chip (SoC). Therefore, it is important to minimize the area and power cost of the cells. Researchers had

reported many SRAM cells like adiabatic 6T, 9T, and 12T to reduce the power consumption [2–8].

SRAMs in aerospace applications have restrictions that are not very reliable due to high potential particles [7]. The stored value in the delicate node may change when the transient voltage pulse is generated by the charge [9]. For extensive system integration, the complex systems, advanced electronics like microprocessors are also introduced in the aircraft [1]. The uncertainty of the system dependability may be increased due to more use of products. So, it requires to analyze the performance of electronic equipment [10].

The microprocessors are considered as the state of art, which requires soft error protection. The soft errors can sometimes disturb the functioning of the system [11]. Due to the high packing density, the memory and logic circuits are more attacked by soft errors. Especially, SRAM cell is more liable to suffer from soft errors due to a wide range of delicate part per bit. In the nanometer regime, soft errors in SRAMs are increasing due to the growth of technology [12, 13]. Error correction codes (ECC) are used to control the SRAM SER, but in ECC error detection and correction are required additional memory and the supporting circuits

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which consume more power, area, and delay [14]. In aerospace applications, the soft error stability with the RHBD process is necessary because of the above-listed reasons. It initiates a novel area-efficient, high stable, and low power radiation-hardened cell to handle the high radiation environment at a higher frequency [15–17].

From the last few years, several RHBD cells like 12T Dice, 12T We-Quatro, and 14T cell had been reported to provide radiation fault free cache memory [9, 18–21]. Velazco et al. proposed a 12T RHBD Dice (dual interlocked storage cell) [18]. In the cell, positive feedback is used by using two latch pairs to recover its original value. In a 12T We-Quatro cell [19], two access transistors are added on 10T-Quatro [20] to obtain good writability. The above-discussed RHBD cell-like Dice, We-Quatro, and boosted-Quatro [8] are consuming more power with less speed. Guo et al. presented the 10T RHBD SRAM cell [21] to solve a large area and more power consumption problem. It has the limitation of high write failure at high-frequency. So it is still challenge to design RHBD cell with balance of all the parameters at a higher frequency. A new radiation-hardened 12T SRAM cell has been proposed to achieve low power dissipation, high write speed, and high critical charge at a higher frequency.

This paper mainly organized as follows: A few conventional RHBD SRAM cells are explained in Sect. 2. The proposed 12T cell has been described with fault recovery and transient response analysis in Sect. 3. The proposed cell has been compared with conventional cells in terms of power, delay, stability, soft error resilience, and the area in Sect. 4. The statistical analysis of the cells has been discussed further in terms of power, stability, and write failure in Sect. 5. Section 6 concludes the paper.

2 Conventional RHBD SRAM cells

2.1 Dice 12T SRAM cell

The most commonly used RHBD cell is Dice cell as insensitive to radiation effect is depicted in Fig. 1. The twelve transistors are required to design a Dice cell, which makes two interlocked latch pairs to resort to the original value using positive feedback with the cost of its large area, power consumption, speed, and hold noise margin [18]. The 12T Dice cell has four output nodes to store values. Assume output values of Dice cell is “B” = ‘1’, “A” = ‘0’, “C” = ‘0’, and “D” = ‘1’. Consider the delicate node “B” is affected by radiation (high energy particles touch the node “B”) then immediately the value stored in the output node “B”(‘1’) is flipped to ‘0’. The P3 depends only on node “B” switched “OFF” temporarily. But the gate of the N5 is connected to node “B” as well as the N2. So the

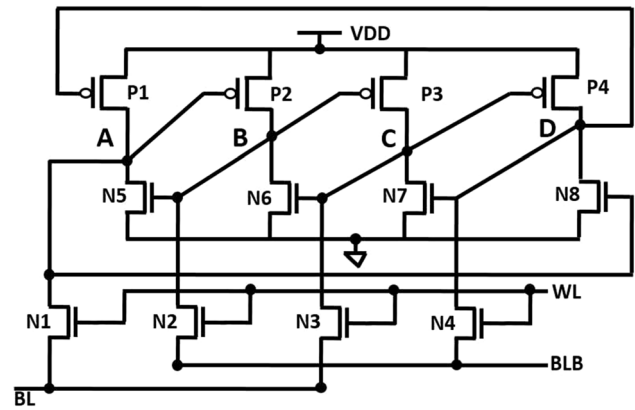


Fig. 1 Circuit diagram of the 12T DICE SRAM cell

lower voltage at the output node “B” does not affect the node “A”. Hence, the disruption is only present to the nodes “B” and “C”. Finally, the disturbance on “B” and “C” is further recovered by P2 and N7.

2.2 12T We-Quatro SRAM cell

The 12T We-Quatro SRAM Cell had been addressed by Trang et al. [19]. In this cell, “We” means writability enhanced. Quatro SRAM [20] suffers from the writability problem due to process variation. They have added two more access transistors to obtain proper writability to Quatro named as we-Quatro. The we-Quatro occupies the same area as Quatro [20]. The main problem of the 12T We-Quatro cell is its high power cost and more delay. Hence, We-Quatro is also less preferable for aerospace applications. In 12T We-Quatro, the output nodes “A”, “C” are connected through pass transistor to the bit line (BL), similarly the output nodes “B” and “D” are connected to the bit line bar (BLB) as shown in Fig. 2. However, in We-Quatro to write ‘0’ at the output node “C” which is holding ‘1’, then the transistor N8 pulls down the voltage at node “C”. Once node “C” pulls down to the

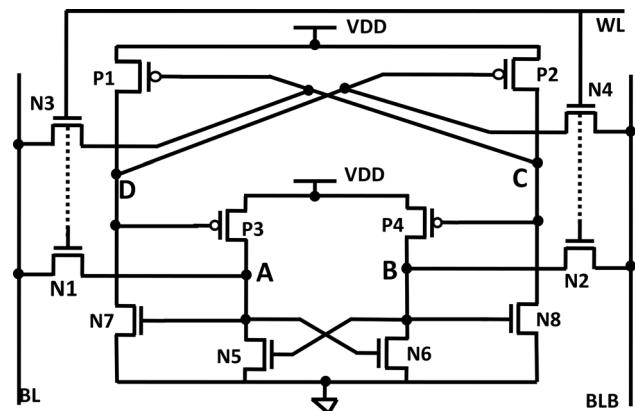


Fig. 2 Circuit diagram of the We-Quatro cell (12T)

ground then immediately nodes “B” and “D” strongly pull up to supply voltage. Considering the situation where ‘1’ stored in the cell. Now the opposite data ‘0’ needs to be written on the cell. Under this situation, the output nodes “B” and “D” are pulled up by P4, P1 respectively. At the same time “A”, and “C” are pulled down by N5, and N8 respectively. Hence the entire output node is simultaneously biased to the voltage expressing the written data, provides a better writability. The simulated response of the We-Quatro cell is indicated in Fig. 3.

2.3 10T SRAM cell

The main drawback of Dice and We-Quatro is its high power consumption with large area overheads. A 10T-RHBD SRAM cell address above problem, as shown in Fig. 4 is designed by Jing Guo et al. [21]. Due to the high delay of 10T cell [13], it shows write failure for high frequency (1 GHz) and 1 V supply voltage at 45 nm CMOS Technology impeding the application of 10T cell. The simulated response of the 10T-SRAM cell is shown in Fig. 5. From the response, it is observed that the 10T cell shows write failure at 1 GHz frequency. The output node “B” is not able to flip fully due to the weak pull-up strength of the “N2”. When the voltage at the output node “A” is lowered, it turns “OFF” the transistor “N4”, which turn “ON” the transistors “P1” and “P6” so the output node “B” is flipped to VDD this makes the writability problem of the 10T cell.

From Fig. 6 [22], it shows the write success of 6T cell. In the write mode of the 6T cell, the output node “A” pulls down through N1, which turns “ON” P2. This directly pulls up the node “B” to VDD through P2. Figure 4 shows the reason behind the write failure of the 10T cell. In 10T cell, the node “A” pulls down through N1. As the node “A” pulls down, the gate voltage of N4 is reduced, which makes the weaker pull-down strength of N4 compared to the pull-up strength of N2. Then the flipping occurs at the node “B”. Therefore, the weak pull-up strength of NMOS

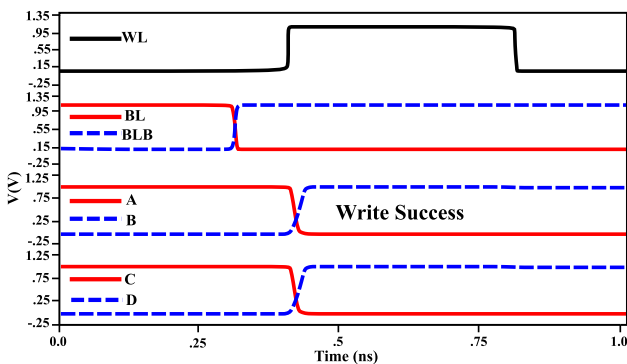


Fig. 3 Simulated response of the 12T We-Quatro cell

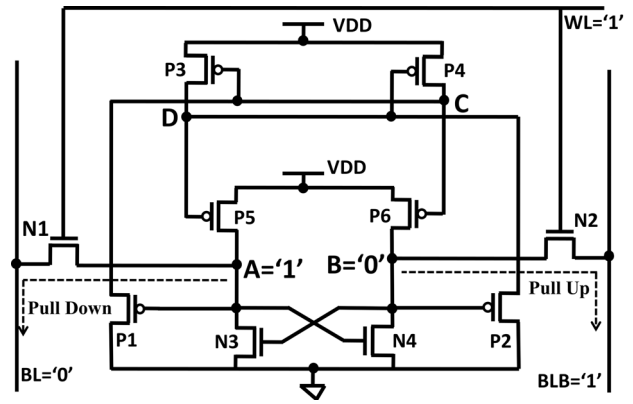


Fig. 4 Circuit diagram of the 10T cell

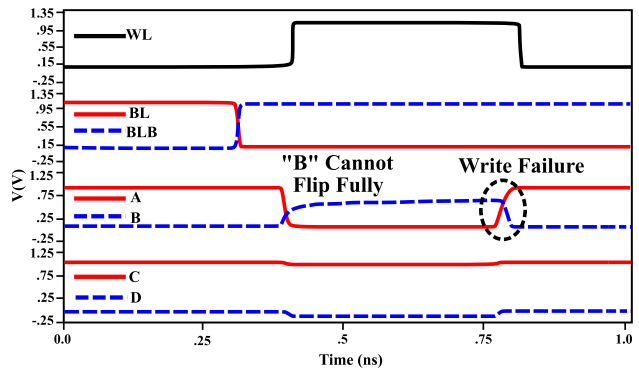


Fig. 5 Transient response of the 10T-SRAM cell, which show the write failure at 1 GHz frequency

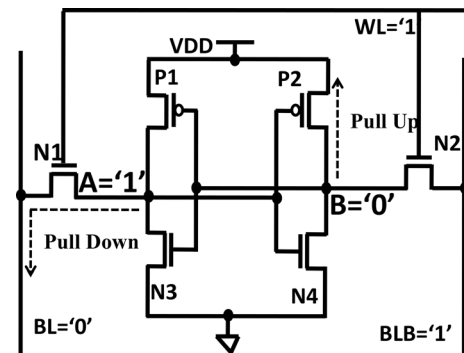


Fig. 6 The reason behind write success of 6T cell

(N2) instead of PMOS (strong pull-up) and high delay are the reason behind write failure of the 10T cell at a higher frequency.

3 Proposed RHBD 12T SRAM cell

In Sect. 2, conventional cells had been described. The main disadvantages of We-Quatro and Dice, they consume more power with high delay, and the 10T SRAM cell suffers

from write failure under high frequency, which is shown in Fig. 4. To address the above challenges, a 12T RHBD cell has been proposed as described in Sect. 3.

3.1 Circuit diagram and layout

The proposed cell, as shown in Fig. 7 consists of twelve transistors. As the 10T SRAM cell [21] is facing write failure at a higher frequency. So two extra transistors N3 and N4 have been added on the 10T cell in the proposed cell to avoid the write failure. The We-Quatro and Dice cell consist of twelve transistors, where four (P1–P4) PMOSs, and eight (N1–N8) NMOSs, respectively. As it has, the more number of NMOSs and due to the structure of design during reading and write mode, the maximum number of transistors is in active mode, and hence, it consumes more power. Therefore, to achieve high soft error and less power consumption, the proposed cell has been designed using more number of PMOSs with a different configuration of transistors. The power and area cost has been reduced, and the critical charge has been improved respectively due to the small size of transistors (all transistors are the same size except P3 and P4 (2.1×)) and more number of PMOSs. The write speed and write SNM has been improved due to added extra N3 and N4 access transistors. The larger size of P3, P4, and connection of the transistors are responsible for higher hold stability.

In retention mode, logic ‘0’ is applied to WL. Under this condition, as WL = ‘0’ all-access transistors N1–N4 will be “OFF”. Hence the stored value at the output node in the latch will be disconnected from bit lines and there will be no changes at the output. Similarly, the circuit is connected from the bit lines, when the logic signal is active high (‘1’) to WL is called active mode. During the read operation, the pre-charge circuit gives high voltage to both the BL = ‘1’ and BLB = ‘1’. If the proposed cell is holding high value, then there is no discharge of BL voltage. But BLB voltage will be discharged, and the stored output is decreased as

both the bit lines connected to the differential sense amplifier, which gives the digital output. Figure 8a depicts the read operation of the proposed cell. Now for a write operation, assume to write ‘1’ on the proposed cell which is holding the value ‘0’, then it needs to give BL = ‘1’ and BLB = ‘0’. Under this condition, as WL = ‘1’ transistors N1–N4 will be “ON”, the transistors N6, P2, P4, P5 will be “ON” so that the transistor P1, N5, P3, P6 will be “OFF” and the store output in the cell will change from value ‘0’ to ‘1’. Hence, the write operation is performed successfully. Figure 8b shows the perfect operation of the proposed cell.

3.2 Soft error recovery analysis (SER)

Suppose delicate node “B” of the proposed cell from Fig. 9 is affected by radiation (high energy particles touch the node “B”) then the value stored in the output “B” (‘1’) flipped immediately to ‘0’. The transistor N6, P1 will be switched “OFF” and “ON” respectively for a short period.

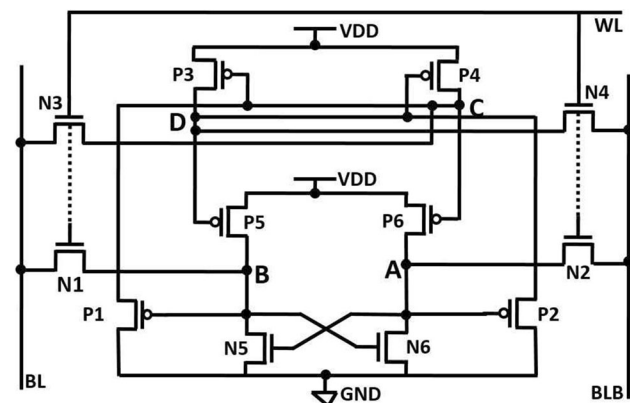
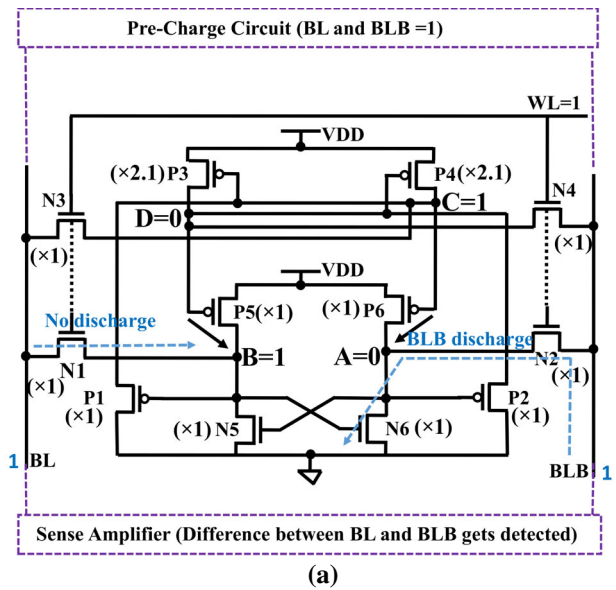
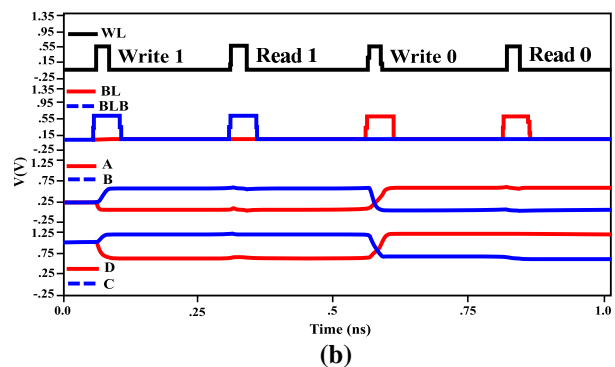


Fig. 7 Circuit diagram of the proposed 12T cell



(a)



(b)

Fig. 8 a Read operation b transient response shows perfect operation of the proposed cell

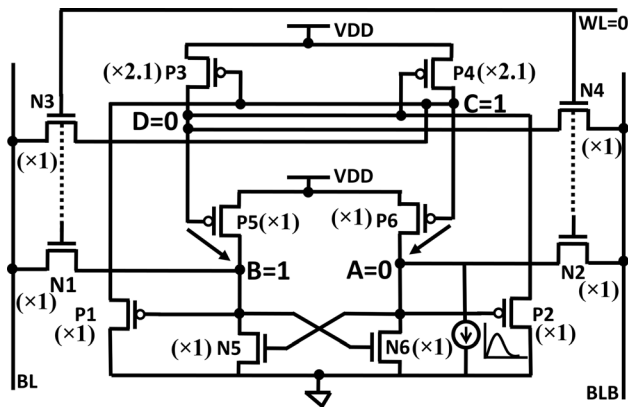


Fig. 9 Circuit diagram of the proposed 12T cell with sizes of the transistors for soft error recovery analysis

In the proposed cell, as the size of P4 is larger than the P1 (2.1×), the maximum voltage from supply drops across transistor P4 and the value at node “C” equal to ‘1’ (previous). However, the gate of transistor P3 is connected to node “C”. Hence P3 will be always “OFF”. Due to “OFF” transistor P3, the voltage across node “D” is unchanged (‘0’). The value (‘0’) at the node “D” makes the transistor P5 always “ON”. Finally, the initial voltage is rolled over to the node “B”, which is equal to ‘1’.

Similarly, when the output “A” (‘0’) is flipped to ‘1’ due to radiation effect, the transistor N5, P2 will be “ON” and “OFF” respectively for a short period. As the N5 is “ON”, the output “B” is switched from ‘1’ to ‘0’, and the N6, P1 will be switched “OFF” and “ON” respectively for a short period. The node “C” will be its initial state due to the size of transistors. The size of the P4 transistor is larger than the size of the P1 transistor (2.1× larger). Hence, the output node “D” remains unchanged. So, the P3 will be always “OFF”, and the P5 will be in always “ON”. Finally, the initial voltage is rolled over to the node “B”, which is equal to ‘1’. Now it will switch “ON” the N6 and the output “A” is flipped to its initial voltage (‘0’). Similarly, for other cases, the size of the transistor P3 is larger than P2 (2.1× larger).

3.3 Writability analysis

Initially, the output nodes “B” and “C” store the value ‘1’ and the output node “A” and “D” store the value ‘0’ by an assumption of the proposed cell. Now it has been written the opposite data during the write mode of the cell. The logic signal high (‘1’) has been applied to BLB and low (‘0’) to BL. Under this condition the access transistor N1 and N3 are pulled down by the node voltages at “B” and

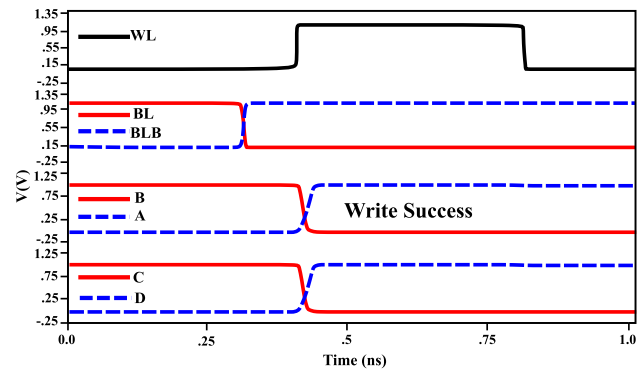


Fig. 10 Transient response of the proposed cell, which shows successfully, write operation of the cell at a high frequency (1 GHz)

“C”, similarly the access transistor N2 and N4 have been pulled up by the output nodes “A” and “D”. Figure 10 shows successfully write operation of the proposed cell at 1 GHz. In Fig. 5, the 10T cell is not able to write at a higher frequency. The 10T SRAM cell is not able to provide full VDD potential to the output nodes “A” and “B” due to the weak pull up of NMOS (N1 and N2). However, in the proposed cell, the extra added transistors N3 and N4 pulls down the node “C” and “D” respectively. The potential at “C” and “D” turn “ON” the P6, and P5 respectively generate the nodes “A” and “B” to full VDD. This type of feedback boosts the writability of the proposed cell.

When the logic ‘0’ will be written on the SRAM cell, which is holding ‘1’, then the node voltage across the output “B” (V_B) gets discharge bit line voltage to a particular voltage which depends on the access and pull-up transistor. Write failure of SRAM occurs whenever the V_B is not able to reduce below the trip voltage of the inverter within the high pulse width of the word line. The size of access and the pull-up transistor is major responsible for write failure of the SRAM cell. The weaker access and the stronger pull-up transistor slow down the discharge process. The process parameters variation changes the device strength, which increases the time required to write data on the SRAM. Hence, the proper size of transistors is not sufficient to reduce write failure. Now it has been observed that when the T_{write} (time required to discharge the “ V_B ” from supply voltage to the trip voltage of inverter) is greater than the $T_{wordline}$ (the high pulse width of the word line), then write failure are gotten so write failure probability ($P_{W.F.}$) of the SRAM cell is given in Eq. 1 [23].

$$P_{W.F.} = P(T_{write} > T_{word-line}) \tag{1}$$

4 Comparison analysis

4.1 Soft error resilience

The primary purpose of the SRAM cell in the aerospace application is to prevent radiation effects. An exponential current source model is used to verify the soft error resilience of the SRAM cells, which is explained and tested in the referred paper [24]. In the read and write mode, the output nodes are connected to bit-lines, so the SRAM cell hardly affected by radiation effects. Hence, the soft error analysis of SRAM cells is performed in hold mode. In hold mode bit lines are disconnected from output nodes because the word line is disabled. In the proposed cell, the output node “B” is one of the sensitive nodes. So, the exponential current source has been applied to the node “B”(high energy particles touch the node “B”), as shown in Fig. 11a. Now to calculate the threshold value ($I_{\text{threshold}}$) of peak current (I_{peak}), the I_{peak} of the exponential current source is increased till data flipping starts [24]. The recovery of the outputs for proposed cell due to high energy particles is shown in Fig. 11 (a) schematic and (b) simulated response. The capacitive effect and the larger size of transistor P3 and P4 ($2.1\times$ larger) balance the extra current due to high energy particles at respective output nodes and recovered the flipped output.

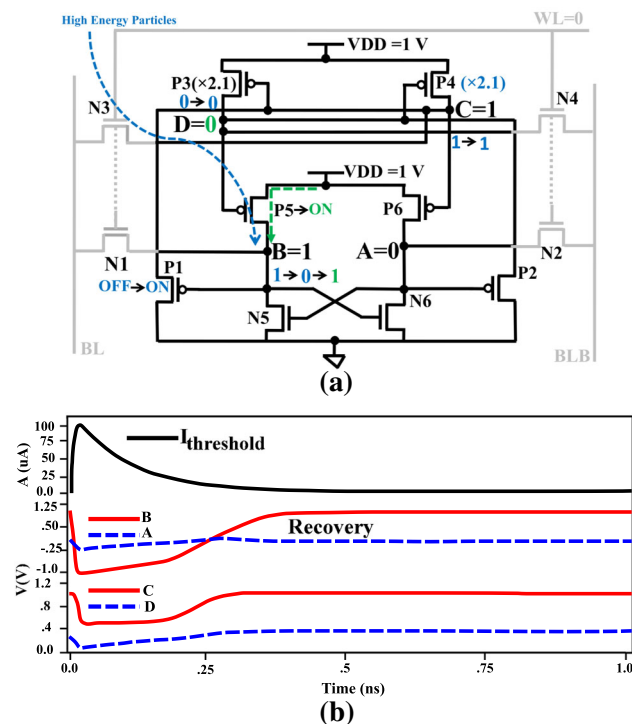


Fig. 11 a Schematic and b simulated response of the proposed cell to show the error controlled

Comparison of critical charge (Q_c) among the SRAM cells is shown in Table 1. From Eq. (2), the critical charge is a function of the backend parasitic capacitance (C_{node}), stabilization current from the PMOS transistors ($I_{P,ON}$), pulse duration (W_{pulse}) and supply voltage (V_{DD}) [25]. In the proposed cell, the number of PMOS transistors are more so $I_{P,ON}$ is high. Also, due to the size of P3 and P4 are larger than the size of P1 and P2 ($2.1\times$), the C_{node} is high which is also responsible for the high Q_c of the proposed cell.

$$Q_{\text{critical-charge}} = C_{\text{node}} \times V_{DD} + I_{P,ON} \times W_{\text{pulse}} \quad (2)$$

4.2 Power and delay comparison

In recent years, as more than 50% area occupied by SRAM based cache memory in the microprocessor [4]. Therefore, the optimized parameters of SRAM based memory are very important. Hence, the power dissipation, delay, and the area of the SRAM are crucial factors. The leakage current of each MOSFET in the SRAM cell is the main source of static and total power consumption determined by a gate and sub-threshold leakage current [27, 28]. When $V_{gs} < V_{th}$, the MOSFET will be “OFF” and it produces some amount of current is called sub-threshold current ($I_{\text{sub-threshold}}$), as given in Eq. 3 [26]. Here, I_0 is the reverse saturation current, V_{gs} is the gate-source voltage and V_{ds} is the drain-source voltage of MOSFET, η is the sub-threshold swing coefficient. V_{th} and V_T are the thresholds and thermal voltage of MOSFET respectively [23]. The fluctuation of electrical parameters during fabrication may change the threshold voltage that may affect the sub-threshold current, as indicated in Eq. (3) [28]. Similarly the gate leakage current contains the gate to the substrate, gate to channel and edge direct tunneling current. As the oxide thickness of the gate diminishes, the gate leakage current enhances exponentially. The combination of minority carriers near the edge of depletion and electron-hole pair generation in the depletion region of reverse-biased junction gives junction leakage current [28].

$$I_{\text{sub-threshold}} = I_0 \times e^{\frac{V_{gs}-V_{th}}{\eta V_T}} \times \left(1 - e^{\frac{-V_{ds}}{V_T}}\right) \quad (3)$$

The proposed 12T RHBD SRAM cell decreases the power dissipation and write delay of SRAM based cache memory. Table 1 shows the power, delay, stability, and area comparison for considered SRAM cells. The total power loss of cell is calculated by the average power losses during the write, read, and hold mode. In the read and write mode ($WL = '1'$) it dissipates dynamic power and in hold mode ($WL = '0'$) it dissipates static power. From Table 1, it concludes that the proposed cell is better than We-Quatro and Dice in terms of power and write delay. The static and

Table 1 Parameters comparison of SRAMs

SRAM cells	Proposed (12T)	We-Quatro (12T) [19]	Dice (12T) [18]	RHBD-14T [16]	6T [22]				
Total power (μ W)	0.981	2.025	1.36	1.23	0.978				
Static power (pW)	26.25	32.32	28.15	26.67	16.16				
Write delay (pS)	14.04	17.20	16.43	16.02	16.30				
Read delay (pS)	83.21	70.56	63.25	93.25	65.23				
Critical charge (fC)	12.15	9.22	6.25	24.15	0.948				
HSNM (mV)	361.0	242.0	81.0	405.2	328.2				
RSNM (mV)	151.0	160.0	173.0	122.1	118.2				
WSNM (mV)	198.0	175.0	224.0 </tr <tr> <td>Area (μm^2)</td> <td>4.298</td> <td>4.212</td> <td>4.507</td> <td>4.392</td> <td>1.725</td> </tr>	Area (μm^2)	4.298	4.212	4.507	4.392	1.725
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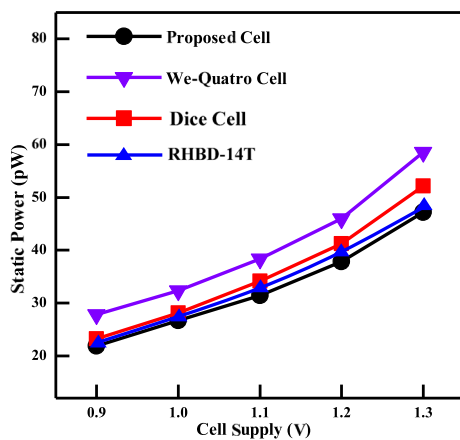


Fig. 12 Static power cost of the SRAMs at different supply voltage

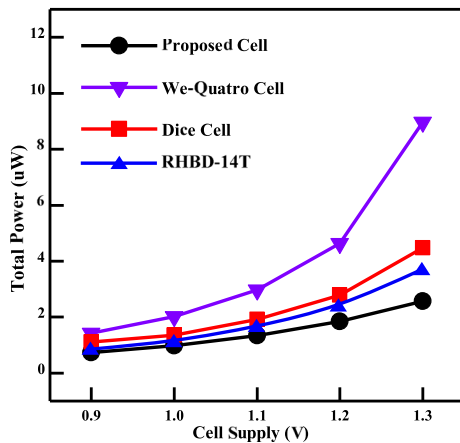


Fig. 13 Total power cost of the SRAMs at different supply voltage

total power cost comparison of the cells at various voltage are reported in Figs. 12 and 13 respectively. Due to the usability of PMOS transistors P1 and P2, it introduces the loss of threshold voltage in the output node “C” and “D”. The voltage in the output nodes “C” and “D” decreases or increases by the threshold voltage, respectively. Hence, it

requires more time to complete the read operation. Therefore, its read access time is more and the comparison is shown in Table 1.

4.3 Area comparison

Table 1 shows the area comparison for SRAM cells, which shows that the proposed cell occupies less area compared to Dice and We-quatro. Based on the layout design, the proposed cell area is equal to the 10T SRAM cell, because the extra added transistors N3 and N4 are placed at the blank space of 10T cell layout. Figure 14a and b shows the layout of the 12T proposed cell of Fig. 7 and the 10T cell of Fig. 4 respectively. The metal-1, metal-2 layers for wiring of the cell are hidden. Only active, N-well, and poly layers are shown in Fig. 14. For the proposed cell the size of transistors P3 and P4 is 2.1 times larger than P1 and P2 transistors respectively, as shown in Fig. 9. For the 12T Dice cell, all the transistors are the same size. For We-Quatro cell, all the pull-down transistors (N5, N6, N7, and N8) are double than all other transistors.

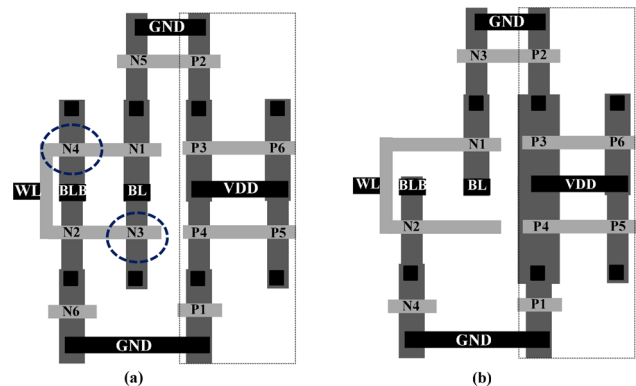


Fig. 14 The layout of the SRAM cells. **a** Proposed 12T cell of Fig. 6, **b** 10T cell [12] of Fig. 4

4.4 Stability comparison

Static Noise Margin (SNM) is the main parameter to define the stability of the cell [29, 30]. The maximum DC voltage is handled by the cell without disturbing the output called SNM. The butterfly curve is the most commonly used method to measure SNM [31–33]. The butterfly curve of considered cells for HSNM, WSNM, and RSNM are depicted in Fig. 15. The stability of the proposed cell is also checked using the pole-zero technique which is presented in Ref. [2]. It shows that all the poles of the proposed cell lies on the left half of the s plane and hence proposed cell have the correct logic function. Table 1 has reported that the proposed 12T RHBD SRAM has better hold noise margin (HSNM) compared to the We-Quatro and Dice cell due to the larger size of P3, P4, and longer feedback. The write noise margin (WSNM) is better than the We-Quatro, and less than Dice cell which can enhance by improving the size of access transistors. The strength of pull-down and driver transistors is responsible for the read noise margin (RSNM). Due to the presence of PMOS (P1 and P2) in the proposed cell, it gives less RSNM compared to other cells. The RSNM of the proposed cell can improve by enhancing the strength of driver transistors. The retention voltage of the proposed, We-Quatro, and Dice cells are 73.2 mV, 59.8 mV, and 58.3 mV respectively.

5 Statistical analysis of SRAM cells

5.1 Statistical estimation (mean (μ) and standard deviation (σ)) of power and stability in SRAM cells

The main contributor to the power dissipation is due to leakage current [34–41]. The leakage current is a

combination of the junction, gate, and the sub-threshold leakage current [39]. The $I_{sub-threshold}$ changes exponentially with the threshold voltage shows in the Eq. (3). Statistical analysis is an essential part before fabrication to know the variation of parameters, which results from the fluctuation of the threshold, channel length, and width because of process variations and mismatch.

The stability of cells also are checked under the 1000 MC Simulations to know the fluctuation of stability in different modes. The Stability comparison of the proposed cell is shown in Fig. 16. From Fig. 16, the minimum HSNM, RSNM, and WSNM are 300 mV, 124 mV, and 183 mV respectively. The 1000 MC Simulations of SRAM cell are performed under SS process and 85 °C temperature to know the fluctuation (mean (μ) and standard deviation (σ) in the power, and the stability of SRAM cells. Figures 17 and 18 depict the μ and σ of total and static power, respectively for the proposed cell. The 1000 MC

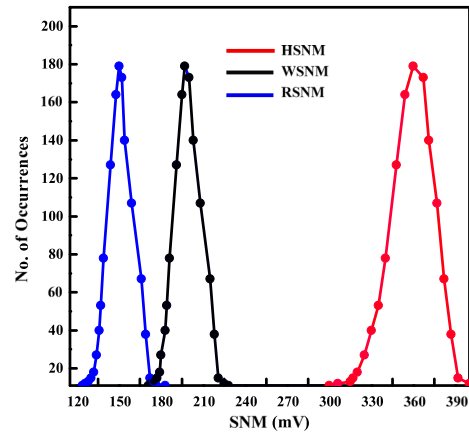


Fig. 16 Stability using 1000 Monte-Carlo Simulation for the proposed cell

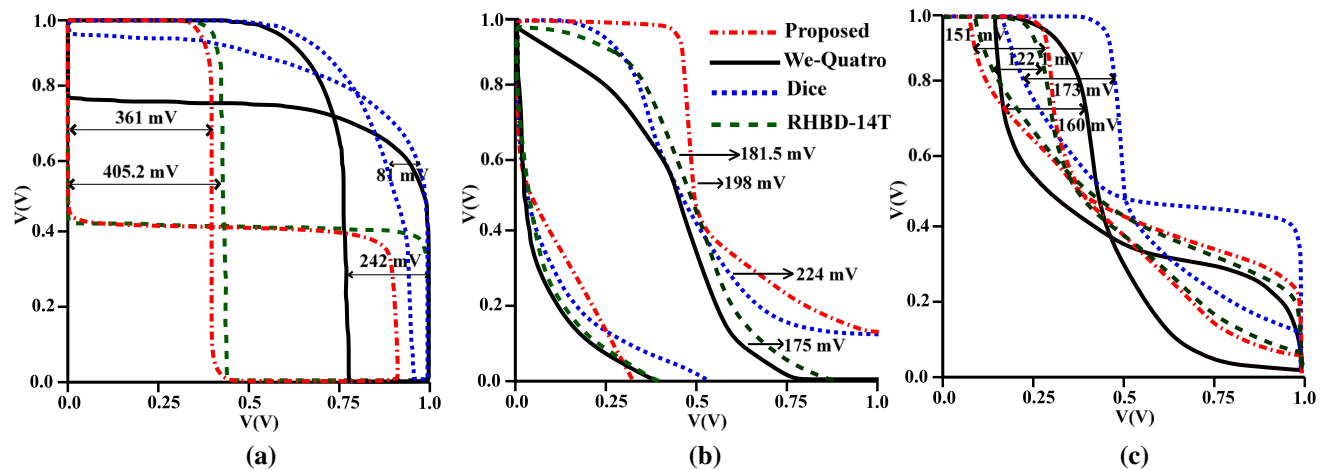


Fig. 15 Butterfly curve of the proposed cell for a HSNM, b WSNM, c RSNM

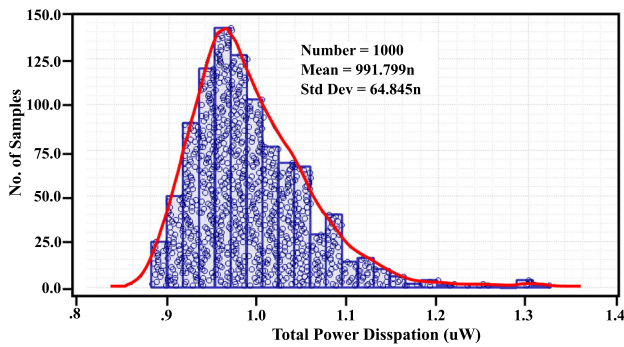


Fig. 17 Total power dissipation with lognormal distribution using 1000 Monte-Carlo (MC) Simulation of the proposed cell

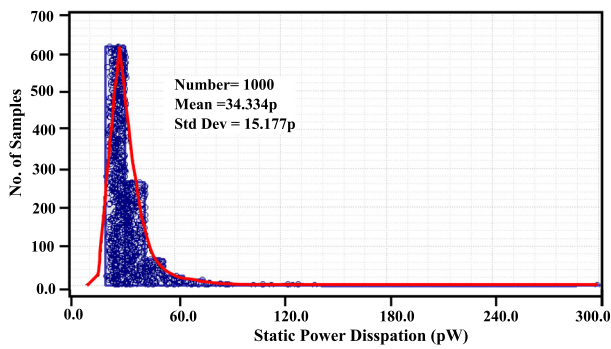


Fig. 18 Static power dissipation with lognormal distribution using 1000 MC Simulation of the proposed cell

Simulation of considered cells are also performed using the same model file and reported in Table 2. Similarly, the same MC Simulation has been performed and reported in Table 3 to know the fluctuation in the stability (SNM) of SRAMs.

5.2 Statistical estimation of the SRAM cells during write mode

The 1000 MC Simulation of cells has been performed in SS corner and 85 °C at a 2 GHz frequency with nominal supply voltage (1 V), to compare the writability of SRAM cells. Figure 19 shows the 10T-SRAM cell having a large number of write failures at a 2 GHz frequency. But the We-Quatro and the proposed cell have no write failure at the a 2 GHz frequency. So, two cases have been observed, to check more accurately the write failure of different cells. In the first case, the supply voltage VDD to 1.0 V at different frequencies, it has been observed that no write failures for We-Quatro and the proposed cell. A large number of write failures have been observed for a 10T-SRAM. In the second case, by scaling the supply voltage VDD to 0.6 V at different frequencies, it has been observed that no write failures for We-Quatro and the proposed cell and a large number of write failures have been observed for a 10T-SRAM. The writability comparison of different SRAM shows in Fig. 19 at different scenarios which proves that the writability of the proposed SRAM better than a 10T cell, comparable to the We-Quatro cell.

Table 2 Distribution of power cost using MC simulation of the SRAMs

SRAM Cells	No. of Samples	Total power		Static power	
		Mean (μ W)	SD (nW)	Mean (pW)	SD (pW)
Proposed-12T	1000	0.991	64.84	34.33	15.17
We-Quatro-12T [19]	1000	2.048	125.9	41.37	20.85
Dice-12T [18]	1000	1.390	101.3	36.37	17.34
RHBD-14T [16]	1000	1.261	98.23	35.12	16.21
6T Cell [22]	1000	0.988	128.9	25.12	13.23

Table 3 Distribution of stability using MC simulation of the SRAM Cells

SRAM Cells	No. of Samples	HSNM		RSNM		WSNM	
		Mean (mV)	Standard Deviation (mV)	Mean (mV)	Standard Deviation (mV)	Mean (mV)	Standard Deviation (mV)
Proposed-12T	1000	361	31.25	151	15.23	198	18.9
We-Quatro-12T [19]	1000	242	23.2	160	15.8	175	16.2
Dice-12T [18]	1000	81	0.79	173	17.1	224	23.1
RHBD-14T [16]	1000	405.1	38.23	122	12.3	181	17.8
6T Cell [22]	1000	328.1	29.21	118	11.9	165	15.8

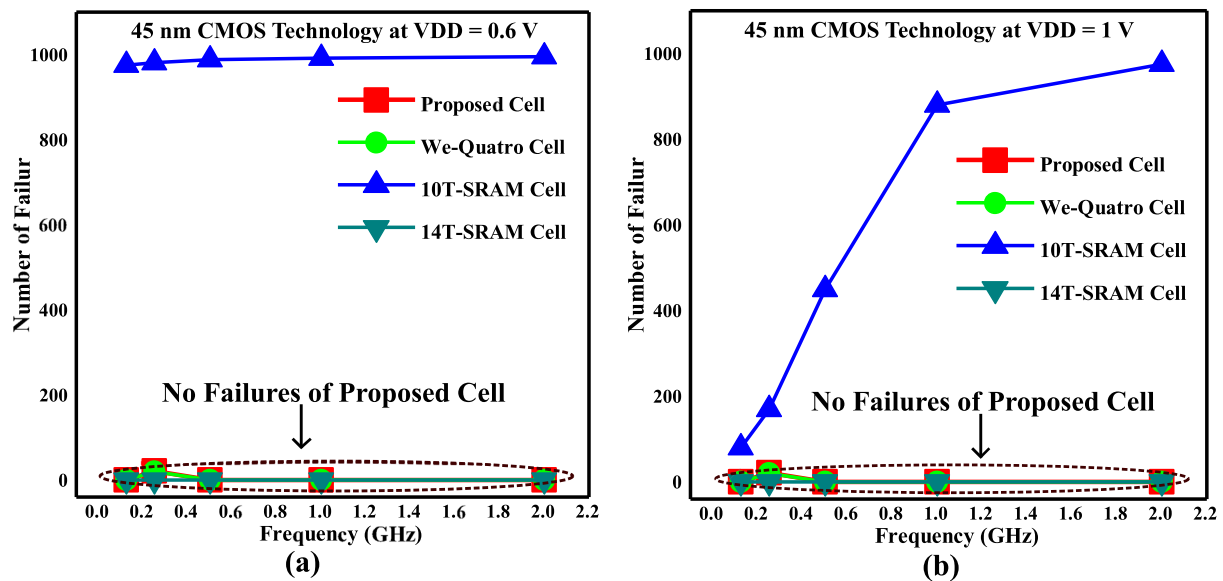


Fig. 19 1000 MC Simulation of SRAM cells to compare writability at various frequencies and **a** supply voltage = 0.6 V **b** supply voltage = 1.0 V

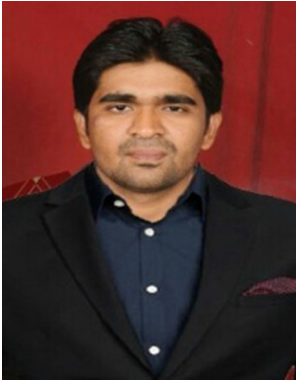
6 Conclusion

The proposed cell area is the same as the 10T RHBD cell and less compared to the 12T Dice and We-Quatro cell based on the layout design. Also, the critical charge for the soft error resilience, power, delay, and stability compared with other cells. The result presents that the proposed 12T SRAM cell consumes 51.56%, 27.88%, and 18.78%, 6.75% less total, and static power dissipation compared to 12T We-Quatro and 12T Dice cell, respectively. The critical charge is improved by 25.16% and 49.27% compared to We-Quatro and Dice, respectively. The write speed of the proposed cell is 18.37% and 14.54% more compared to We-Quatro (12T), and Dice (12T), respectively. The HSNM of the proposed cell is improved by 32.96% and 77.56% compared to We-Quatro and Dice, respectively. The WSNM of the proposed cell is increased by 11.6% and decreased by 12.7% compared to We-Quatro and Dice cell, respectively. The RSNM of the proposed cell is less and comparable to We-Quatro and Dice cell. Hence the proposed SRAM cell provides a good balance between power, stability, delay, and the area under high radiation environment at the high frequency, so it is an excellent choice for aerospace applications at higher-frequency.

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