Analog Integrated Circuits and Signal Processing (2021) 107:659–670
https://doi.org/10.1007/s10470-020-01760-4

An efficient, scalable, regular clocking scheme based on quantum dot cellular automata

Jayanta Pal[1] · Amit Kumar Pramanik[2] · Jyotirmoy Sil Sharma[1] · Apu Kumar Saha[3] · Bibhash Sen[4]

Received: 29 June 2020 / Revised: 28 July 2020 / Accepted: 30 November 2020 / Published online: 3 January 2021

Abstract

The present CMOS VLSI technology is facing some challenges like working in nano scale, device density, power dissipation, operating frequency, fast execution, which demands a proper alternative. Quantum dot Cellular Automata (QCA) is one of the feasible substitutes for the same. In QCA, clocking is the primary driving source of power, and the flow of information occurs with the effect of underlying clocking circuitry. But in most of the designs, the proper use of the underlying clocking circuit was circumvented and targeted on random, ineffective clocking, which is a concern of convolution in terms of buildability. On the other hand, wire crossing plays a very critical role in cell layout, as well as the underlying clocking circuit for QCA. In this regard, a proposal for an efficient clocking scheme is of paramount importance with a reduction in underlying wire crossing. This article presents an efficient, scalable clocking scheme with a regular clocking region, feedback path, and fabricatable with minimal underlying wire crossing structure. The reduction in wire crossing significantly decreases the trouble of assembling the circuit in practice. To advocate the superiority of the proposed clocking scheme, both the combinational and the sequential design has been investigated using the proposed clocking scheme. QCADesigner is used to comply with the functionality and compared for improvement with the design in previously available clocking schemes.

Keywords Regular clocking · Underlying wire crossing · Quantum-dot cellular automata · 2:1 MUX · SR Latch

1 Introduction

It is expected that CMOS technology will reach the fundamental physical limits in the near future [7] by its property like power dissipation and short-channel effects, which intern will degrade the performance in the nano-scale. So as to conquer these issues and to proceed with, the researcher has proposed many new technologies in recent past years like Quantum-dot Cellular Automata (QCA) [38, 44], Single Electron Device (SED) [41], Molecular Electronics [10], Resonant Tunneling Diodes (RTD)[18] to name a few. Among these feasible alternative approaches, QCA is more promising technology with the striking concept of quantum dots to the traditional CMOS technology [20]. This transistor-less paradigm capable of computing in nano-scale offering remarkable lead as high density, low power consumption, and performing at high speed with terahertz frequency [35, 40] and operates by the accommodation of electrons.

✉ Jayanta Pal
jayantapal@tripurauniv.in

Amit Kumar Pramanik
amit.pramanik21@gmail.com

Jyotirmoy Sil Sharma
mailme.jyotirmoy@gmail.com

Apu Kumar Saha
apusaha_nita@yahoo.co.in

Bibhash Sen
bibhash.sen@cse.nitdgp.ac.in

[1] Department of IT, Tripura University, Suryamaninagar, India

[2] Department of CSE, Dumka Engineering College, Jharkhand, India

[3] Department of Mathematics, NIT Agartala, Tripura, India

[4] Department of CSE, NIT Durgapur, West Bengal, India

A square-shaped QCA cell is made up of four dots with two electrons doped inside it. Majority voter gate [29] and inverter [13] are the basic components for QCA design. A polarized state of a cell is engendered via QCA wire. The signal transition occurs with the influence of the clocking signal, unlike the current flow as, in the case of CMOS [32].

The right and effective polarization of QCA cells are empowered by an external clock signals [21], through which the potential barriers can be controlled within the quantum dots. These clock zones are also defined by these clock signals. With these foundations, many circuits in sequential, as well as the combinational approach in QCA have been proposed so far [2, 23, 25, 31, 36, 37, 39]. Woefully, most of the cases, the proposed works have a diversion from the use of a regular clocking circuit.

Apart from that, the incorporation of the interconnect issue in any electronic device must be addressed. Generally, a wire-crossing can be implemented by passing one wire over the other [5, 28]. Clock phase-based wire crossing directly affects the cost of the circuit, because, with the increase of clock phase, the latency also increases. On the other hand, rotated cell-based crossing or multilayer based wire crossing results in a circuit with fabrication issue, as doping of rotated cell or incorporating a number of layers is still an area of concern in implementing the practical logic circuitry. Therefore, using a large number of wire-crossing leads to downscaling of the circuit and increasing the complexity of cost efficiency and fabrication. Thus, it is important to ensure the minimum amount of wire crossing in a coplanar architecture.

An appropriate clocking scheme has an important significance in developing the specification of logic design in QCA technology. Few clocking schemes for QCA had been reported in [6, 12, 19, 33, 45, 47]. The prior three are neither universal nor even complete in terms of efficiency, flexibility, and scalability. They do not even support the feedback path, which is not a suitable choice for sequential circuits. A clocking with the feedback path is realized in [45], with an increased number of cells, and the complexity of the circuit. It has been addressed by in [6] but, there exists wire crossing in it. The RES clocking scheme [12] emerged as an alternative utilizing coplanar wire crossing with three directional information flow facility. As the clock zone "3" does not relay a regular underlying metal wire, it incorporates more underlying metal wire crossings, thus increasing the fabrication overhead. Optimized 2-D clock in proposed in [47], incorporating these issues with no metal wire crossing. However, the cost of wires increases extensively with the expansion of the clocking or realizing the larger circuitry.

All these matters of contention have motivated us to think and design a new Efficient, Scalable & Regular (ESR) clocking scheme with reliability, scalability, and, more importantly, with a reduced number or elimination of underlying wire crossing. This paper presents a novel clocking scheme and also capable of realizing QCA circuits as efficiently as the earlier schemes. The proposed clocking scheme is fabricable using fabrication technologies, which can convert the circuit to realistic and practical. The research contributions in this work include the followings:

- A new clocking scheme is proposed for the QCA logic circuit.
- The proposed clocking scheme enables optimum underlying wire crossing to reduce the fabrication complexity.
- It permits the development of QCA circuits with a feedback path facility.
- The scalability and performance analysis of the proposed clocking scheme is presented, which outperforms all the existing schemes.
- Both combinational and sequential design is simulated using the proposed ESR clocking scheme.
- QCADesigner tool has verified the functionality of the design.

This research primarily focuses on proposing a new ESR clocking and realize combinational and sequential design using the same. The rest of the paper is organized in the following manner; Sect. 2 discusses the basics of QCA. In Sect. 3, a literature review of different existing underlying clocking schemes has been made. The Proposed clocking is being illustrated in Sect. 4. Section 5 deals with the performance analysis of the proposed design using the proposed ESR clocking, and lastly, concluded in Sect. 6.

2 QCA basic elements

The fundamental structure of QCA cell is illustrated in Fig. 1(a), it is a square-shaped block unit and consists of four different dot regularly distributed in the corners. A pair of electrons resides within it, due to the coulombic force of repulsion it takes diagonal position [19]. They represent the digital logic bit (1 or 0) by cell polarization ($+1$ or -1) depending on cell arrangement in either diagonal. Figure 1 captures the concepts in a frame. The Majority gate (Fig. 1(c) plays a dominant role in designing QCA circuits [11, 27]. The functional logic is expressed as $Output(F) = P.Q + Q.R + R.P$ which is usually represented as $Maj(P, Q, R)$ with 3 inputs P, Q and R. With the help of this gate and the polarization property of QCA cell, the basic logic gate like OR & AND can be realized by applying $+1$ & -1 respectively in one of the inputs [4, 24]. The wire in QCA comprises of array of cells to propagate

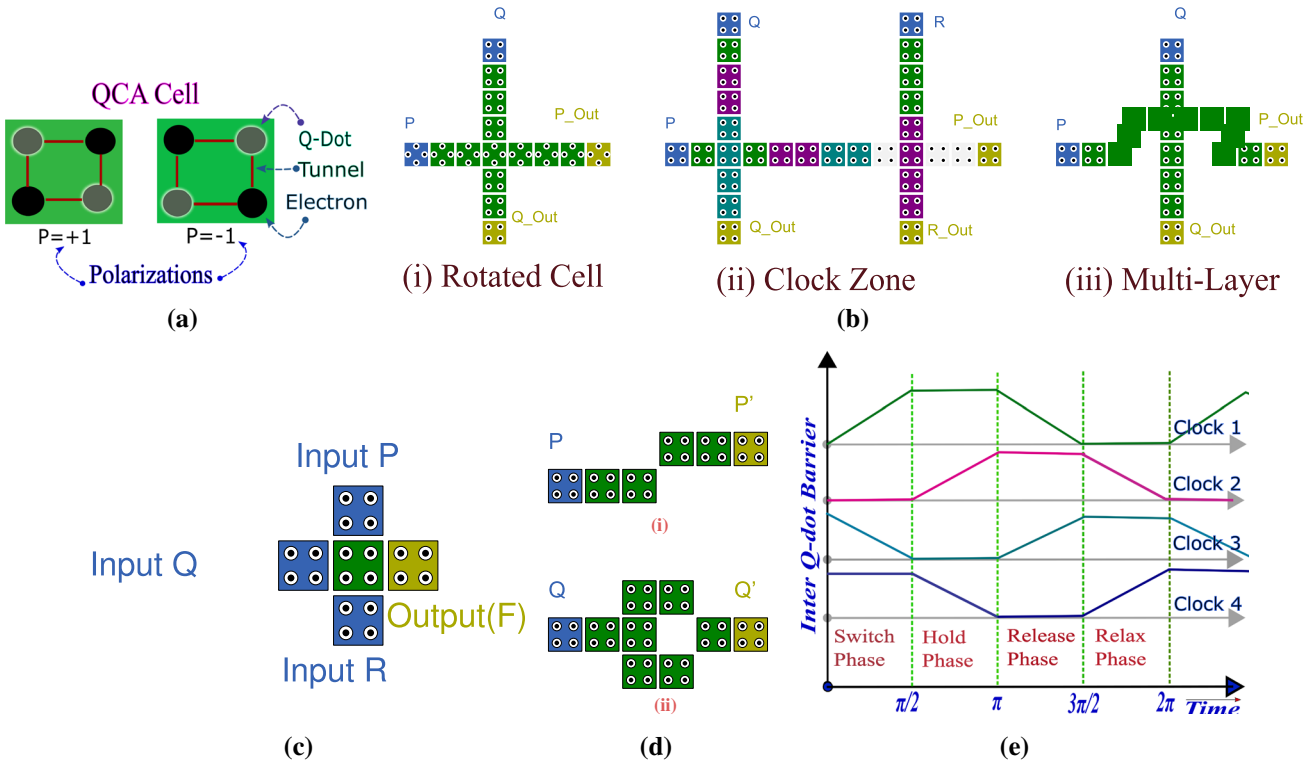


Fig. 1 Basic structural components of QCA

the value from input to output or the intermediate circuitry. The inverters for the opposite polarization of input cell can be realized with cell arranged as Fig. 1(d). **Wire-Crossing**: While fabricating, the interconnection of QCA wires needs special care for a better stabilized circuit. The coplanar approach, as depicted in Fig. 1(b-i) (Rotated Cell based crossing) & Fig. 1(b-ii) (Clock zone based crossing) and Multi-layer (Fig. 1b-iii) approach are commonly used crossover methods. The coplanar approach uses two different types of QCA cells for crossing. In contrast, the Multi-layer approach is implemented with more than one cell layer like multiple metal layers, as in the case of traditional IC.

Clocking To control the flow of data and to supply power to automation in the QCA clock is used, which intern controls the flow of information. The clocking is realized by controlling the potential barrier, which generates four operating phases [43]. Figure 1(e) demonstrates the clocking concept and different zones with separate colors. The barriers between dots start rising in the locking stage, followed by a locked stage, where the situation occurs when barriers are fully raised, which restricts the electron move between dots. In the relaxing stage, the tunneling barriers start lowering and finally completely lowered in a relaxed stage where electrons can move freely at this stage [1, 42]. Alternatively, these phases are known as the Switch phase, Hold phase, Release and Relax phase, respectively [34].

3 Related work

Present status of Wire crossing Coplanar wire crossing consists 90^0 and 45^0 orientated cell in opposite directional wire (Fig. 1b-i), may lead to cell misalignment resulting in cross-coupling and ultimately decreases the robustness of the circuit [3]. The second mechanism (Multi-layer, Fig. 1b-iii) yields in a costly circuit as creating layers while fabrication in QCA is an issue till date [8]. Wire crossing can also be implemented utilizing the clock zones (Fig. 1(b)-ii), where the switch, and release phase is crossed and the cells in the hold and relax phase are crossed, without any polarization effect [9]. It utilizes all four phases, which also increases the clocking count and gradually increases the QCA cost of a circuit, too [22]. Considering all these points, it is utmost required to minimize the number of wire crossing (if not possible to eliminate) to design a robust, cost-effective, and fabricatable QCA circuit.

Present status of Clocking scheme On the other hand, clocking has an expandable role in realizing the QCA circuits with unique benefits like restoration of lost signal and attenuation. In the present scenario of QCA, most of

the work emphasizes cell count in a clock zone, which lacks any established rules. It typically doesn't legitimize their choice and also disregards the clocking circuit implementation, which is responsible for generating the clock regions. The tunneling barrier between the quantum dots are induced or prompted by the electric field, which generates the clocking in QCA. The commonly known approach, where Carbon Nanotubes [26] or the metal wire are buried underneath the layers of QCA cell (see Fig. 3), to realize the underlying clocking circuits is proposed in [14]. This section discusses the different clocking schemes available in QCA.

One-Dimensional Clocking Scheme The concept of QCA clocking was first proposed by [19] with a uni-dimensional placement of the clocking zones, also known as the One-Dimensional Clocking Scheme. Having this base, a later study in [14, 17] suggested it should be a regular, bounded shape and uniform as well. As depicted in Fig. 2(a), it divides the clock zones along with the horizontal axis only. Thus, the enlargement of QCA wire in any sophisticated design along with the vertical axis keeps them in the same zone. Whereas, the vertical line could make a significant contribution to the circuit. Though the clocking demands can be fulfilled, it prevents the execution of feedback paths.

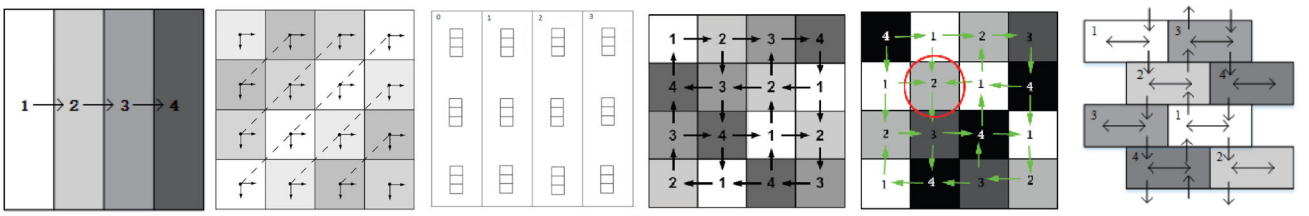
Two-Dimensional Clocking Scheme Different problems like wire length difference, non uniform clock zone width, the difference in cell number between zones, and importantly feedback path and un-utilized area have been reported in [30] proposing Trapezoidal and the Universal clocking scheme. But neither the scheme was revealed, nor the zones were equal in shape and size. Hence, a formal proposal for two-dimensional clocking schemes reported in [45] with bi-directional input and output facility. The most encouraging 2DDWave scheme is based on a grid of rectangular clock zones having the same size (Fig. 2b). The thermodynamic effects due to the large QCA wire length have been able to be avoided. However, the implementation of a sequential circuit remains an issue due to the uncertainty of realizing the feedback path.

Regular Cell based Clocking Scheme A new clocking scheme is proposed in [33] based on one-dimensional technique primarily aims in avoiding the use rotated cell in wire crossing as in case of 2DDWave, instead using regular cells only for the flawless flow of information as shown in Fig. 2(c). Here, the circuit is divided into many regular clock zones for each clock phase in a uni-directional way, as in 1-Dimensional clocking. But the same issue of feedback path remains along with the QCA cost, as the clock zone increases multiple times.

USE Clocking Scheme A Universal, Scalable, and Efficient (USE) clocking scheme facilitates the effective implementation of feedback, proposed in [6]. The clock zones with immediate effect of data propagation are kept together (like clock zone 0 propagates data to zone 1, zone 2 propagates to zone 3 and so on), as shown in Fig. 2(d). There are four grids with a loop facility automatically maintaining the clock zones. It also maintains the opposite directional transformation of information in the adjacent rows and columns. An electric field generation circuitry is proposed for the regular clock zones where metal wires are buried diagonally under the layer. It is to be noted that, it integrates underlying metal wire crossing for the circuit realization. Additionally, in this scheme, multi-layer cross over is entertained for circuit synthesis, which is not a proper or suitable method for fabrication.

RES Clocking Scheme The Robust, Efficient and Scalable (RES) clocking scheme is proposed in [12]. It utilizes only coplanar wire crossing eliminating the cons of USE clocking. Unnecessary white spaces created for opposite directional cell placement to achieve routing purpose as in case of USE have been taken care of by fixing the cell below the top left corner to clock zone 1 as shown with a red marker in Fig. 2(e). Three directional flow of information has been considered as an added benefit. In achieving the advantages described above, this scheme lacks in generating a uniform underlying layout for the particular clock zone 3. It is responsible for unnecessary wire crossing under the QCA layer, and at the same time, the complexity of fabrication also increases.

Optimized 2-D Clocking Scheme A new tile structured timing scheme is proposed in [47], which is capable of realizing all functionalities of existing clocking. The optimized 2-D clocking scheme, as shown in Fig. 2(f), resolves



(a) 1D Clocking [19] **(b)** 2D Clocking [45] **(c)** Regular Cell based clocking [33] **(d)** USE clocking [6] **(e)** RES Clocking [12] **(f)** Optimized 2-D Clocking [47]

Fig. 2 Different existing Regular Clocking Schemes based on QCA

the trouble of underlying metal wire crossing. According to the proposed structure, it acquires a rectangular shape clock zone having a 2:1 aspect ratio. Importantly, it indicates a clocking circuitry with no wire crossing. However, a shift in the blocks (clock zone) in the consecutive row makes it practically difficult to fabricate. It facilitates bi-directional information propagation only in each block or zone. Moreover, the wiring cost (the number of wires) gets doubled with the addition of every single row.

Compiling these clocking schemes, it can be concluded that, underlying metal wire crossing is a matter of concern for fabrication. The wiring cost should also be considered and at the same time. The clocking scheme must be well defined as two-dimensional clocking, uniform, and flexible like USE, robust and scalable similar to RES and optimized in metal wire crossing like Optimized 2-D clock for the design of cost effective circuits with feedback. The next section proposes ESR clocking scheme complying with these demands.

4 Proposed ESR clocking scheme

In this section, a novel timing scheme for the nanotechnology based QCA circuit is proposed. The proposed clocking scheme bears a resemblance to the drawbacks of 2DDWave, Regular Cell based clocking, USE & RES clocking with a significant reduction in underlying metal wire crossing.

As suggested in RES [12], just having side by side opposite direction may lead to unnecessary white spaces in the circuit. So, the transmission directions in the proposed scheme are not always opposite to each other. The placement of clock zones are regular and uniform with the interacting zones together like USE [6]. The interacting zones are kept adjacent to each other (As an example, clock 2 interacts with clock 3, clock 4 interacts with clock 1 and so on). It can be noticed that the upper two rows are arranged like 2DDWave with bi-directional inputs and outputs. However, the feedback loop can be realized in the bottom rows, which is suitable for the sequential circuit. A square zone based proposed Efficient, Scalable & Regular (ESR) clocking scheme is depicted in Fig. 4. The proposed clocking circuitry used to electric field generation for the clock zones indicating the metal wire orientation and wire crossing (shown in Fig. 5). The proposed clocking scheme provides a homogeneous electric field with the metal wire distributed over a single clocking zone. The clock generator proposed here can be realized using the fabrication technique used CMOS technology[15].

It (proposed ESR clocking) allows a straight line, a zig-zag line and a feedback loop with a minimum metal wire crossing. Both directional feedback (clockwise or anti-clockwise) can also be utilized, which is vital for sequential circuit and memory design lowering the burden as shown in Fig. 6(a). According to the area or size of the circuit, the proposed clocking scheme can be expanded as and when required, as referred in Fig. 6(b) with an outline of the overview of clocking circuitry on expansion. It is observed that clock zone '1' and clock zone '3' are configured a zig-zag like a pattern; thus, it can also be named as Zig-Zag clocking scheme. All the clock zones follow a predefined direction of information flow and also with an existence of a feedback path. Additionally, with the advent of zig-zag direction, this scheme also allows three-directional input as well as output, which improves the fan-out of the circuit. If the zig-zag pattern of clock zone '3' is noticed, then it can be observed that, when it makes a cross over with clock zone 4, it facilitates a three dimensional input from clock 3 to clock 4. While making a cross over with clock 2, it has the three-dimensional output from clock 2 to clock 3. Similarly, clock zone 1 creates three-dimensional input and output on the cross over with clock zone 2 and clock zone 4, respectively.

It is worth mention that the proposed clocking scheme takes all advantages of previously known timing schemes and introduces a new scheme combining them with a minimal metal wire crossing. However, considering the optimization of wire crossing and complexity of buildabilty/fabrication it is required to eliminate the underlying metal wire crossing. The optimized 2-D timing scheme with the structure of a tile, as proposed in [47], deals with this issue. But, the metal wire complexity also increases as the number of wires gets doubled for each row expanded for the realization of a large or complex circuit. Considering the optimization of wire crossing, and at the same time, the wiring complexity, an alternative wire orientation is at this moment proposed in Fig. 7. It can be observed that the underlying metal wire crossings are eliminated with optimization in wire complexity. The diagonal orientation of metal wire reduces the increase in the number of wires with the extension of grids according to the circuit area.

5 Performance analysis and discussion

In this section, the comparative study of the proposed scheme with the previously known better schemes of clocking in terms of metal wire crossing is discussed. The basic combinational and sequential circuit using this scheme is implemented to prove the acceptability and applicability of proposed scheme and also compared with metrics of the circuits using Two dimensional (2-DDWave), Universal, Scalable and Efficient (USE), Robust, Efficient and Scalable (RES) and Optimized 2-D (Tiles) timing scheme for the same design.

5.1 Structural comparison

To permit metal wire crossing, an extra metal layer has to be utilized and to generate uniform electric field, the implementation of metal pad is required in a third layer below each clock zone (see Fig. 3).

So, to reduce the fabrication overhead, metal wire crossing needs to be reduced in number. With this technique along with diagonal orientation of wire to minimize complexity, the clocking circuitry for USE, RES, and Optimized 2-D clocking (Tiles) are shown in Fig. 8. The underlying metal wire crossing for corresponding schemes are marked as red circles. Besides the advantages of ESR clocking, the reduction in the metal wire crossing perceptible as compared to USE, RES or Optimized 2-D in the circuitry to generate the electric fields, which yields a lower complexity and cost-effective circuit design.

Table 1 shows the comparison table based on the 4×4 structural grid. It can be noticed in this table that, 2DDWave clocking scheme may be implemented with no wire crossing, but it fails in providing feedback path. However, it can generate feedback with a long-distance wire by placing six (6) rotated grid of cells as reported in [45], which produces an extensive number of underlying wire crossing, and also the fabrication constraint remains very high. It also shows that the metal wire crossing reduced to two (2) as compared to six (6) in the case of USE and four (4) as in RES. Considering the wire orientation as Fig. 8(c), the proposed ESR clock also reduces wire crossing as compared to three (3) in Optimized 2-D (Tiles) scheme. Along with these, it provides three-dimensional input and output as compared to input at one point in RES. This facility is not available in the case of 2DDWave, USE, or Optimized 2-D clocking scheme. Moreover, the alternate orientation for wire, as proposed in Fig. 7, optimizes the underlying meta wire crossing as it succeeds in eliminating the same.

Table 1 Structural Comparison with 4×4 grid

Clocking	Feedback	Wire Crossing	Multi-direction
2DWave [45]	Partially[a]	0[b]	No
USE [6]	Yes	6	No
RES [12]	Yes	4	Yes
Optimized 2-D [47]	Yes	3[c]	No
Proposed (Fig. 5)	Yes	2	Yes
Proposed (Fig. 7)	Yes	0	Yes

[a]Normally does not facilitate. It is costly to implement

[b]ncreases extensively while realizing feedback loop

[c]Considering wire orientation as shown in Fig. 8

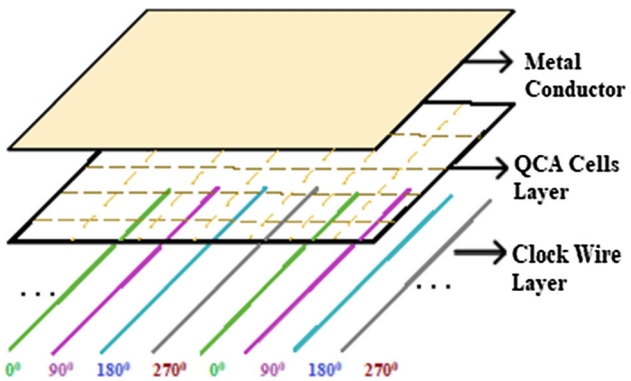


Fig. 3 Schematic view of QCA Underlying Clocking

5.2 Circuit realization

To comply with the applicability of the proposed ESR clocking scheme, both combinational and sequential circuits are designed. A 2:1 Multiplexer which plays an an important role in boolean function recognition & circuit designs and the SR-Latch, the basic in the sequential circuit are compared to its counter design using 2DDWave clocking, USE clocking, and RES clocking scheme. All results are based on simulations with the QCADesigner [46] tool version 2.0.3 in the coherence vector simulation engine mode.

5.2.1 2:1 Multiplexer

A 2-to-1 multiplexer is presented following the design principle of the proposed ESR clocking scheme with the schematic, as shown in Fig. 9.

QCADesigner based implementation of the 2-1 multiplexer circuit using the proposed clock scheme is displayed in Fig. 10(a). The simulated waveform of the proposed 2-1 multiplexer, as depicted in 10(b), verifies the output and operations of the design.

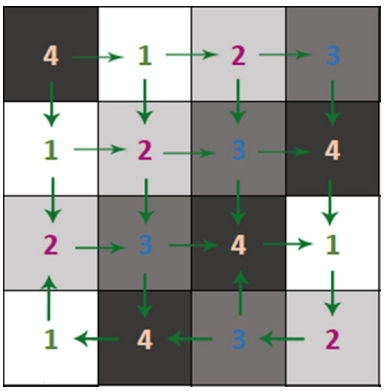


Fig. 4 Clock zone arrangement for the proposed ESR scheme

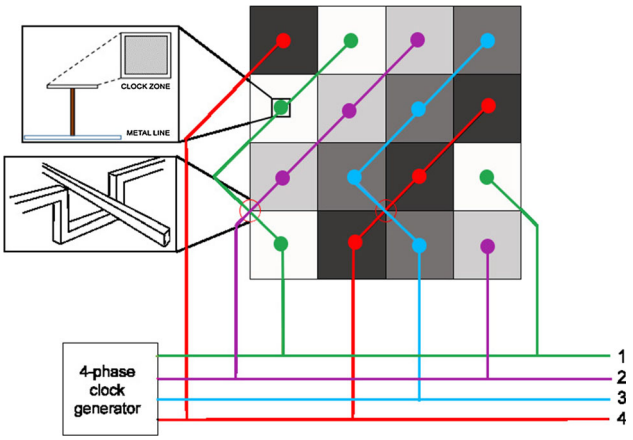
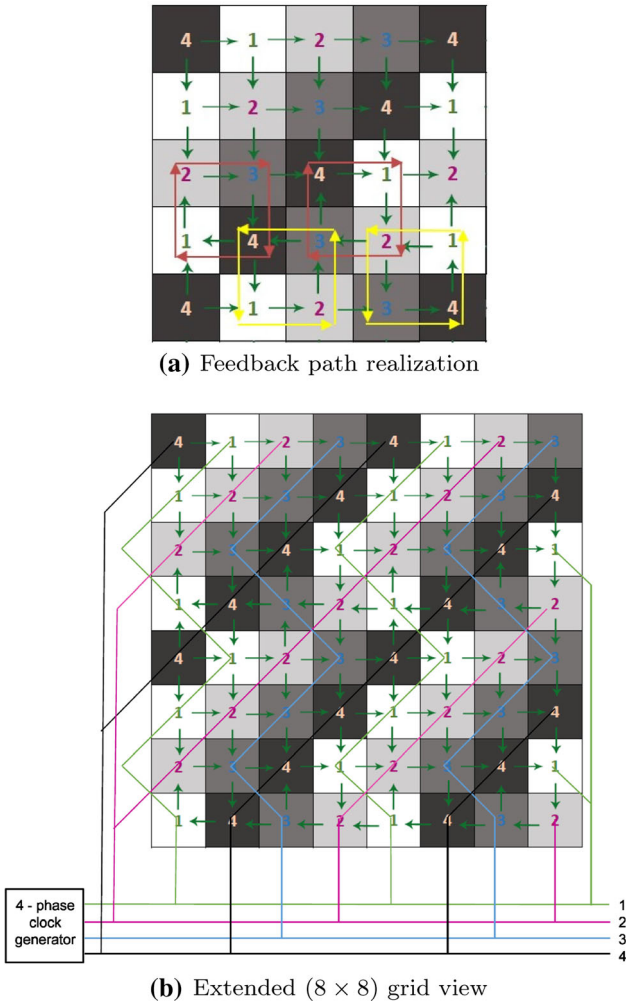


Fig. 5 Clocking circuitry of proposed ESR clocking scheme



(a) Feedback path realization

(b) Extended (8×8) grid view

Fig. 6 Expandability & Scalability of the proposed ESR clocking scheme

5.2.2 SR Latch

The sequential circuit (SR Latch) is designed with the proposed ESR clocking scheme to comply with the realization of the feedback path. The schematic diagram for the SR Latch can be found in Fig. 11, as discussed in[12, 16].

Figure 12(a) depicts the clock zones for SR-Latch using proposed ESR clocking, and the simulation results are highlighted in Fig. 12(b). The simulation waveform confirms the sequence of order as hold, reset, set and hold; with the input vectors S = 0000 1111; R = 0101 0101 and the output Q = X011 1011. This affirms the exact functionality of the SR latch.

The proposed circuits are compared with the counterpart designs in 2-DDWave [45], USE [6], RES [12] & Optimized 2-D (Tiles) [47] clocking scheme in respect to the metrics like Cell count, Area, and latency. The comparative analysis is presented in Table 2. A significant improvement is observed for all parameters. In this table, the last row considers the linear wire orientation in each row of Tiles clocking scheme as presented in [47] and the alternative

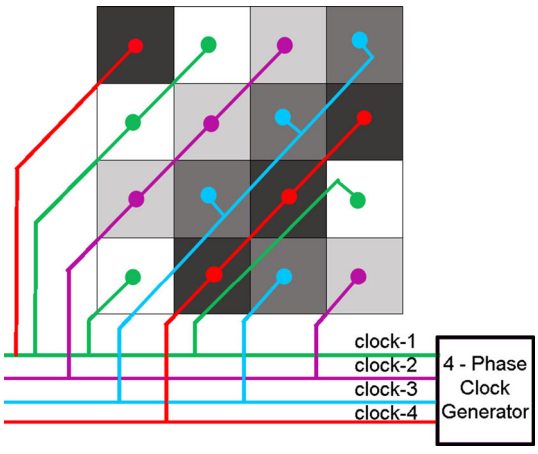


Fig. 7 Alternate metal wire orientation for ESR, eliminating underlying wire crossing

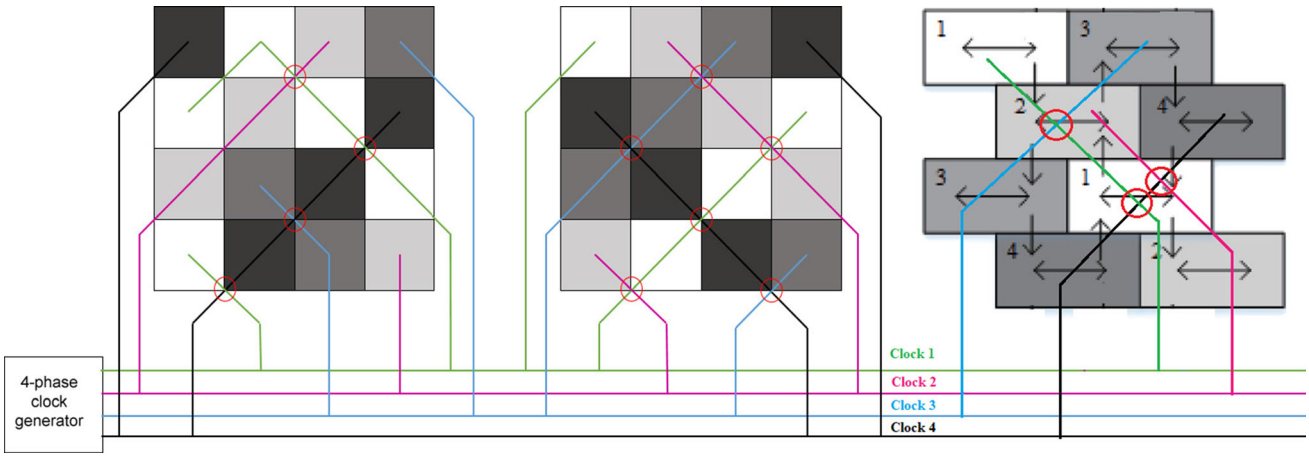


Fig. 8 Underlying Metal Crossing in RES, USE and Optimized 2-D Clocking respectively

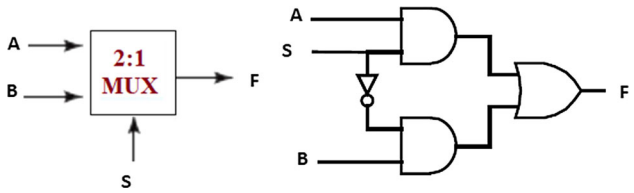
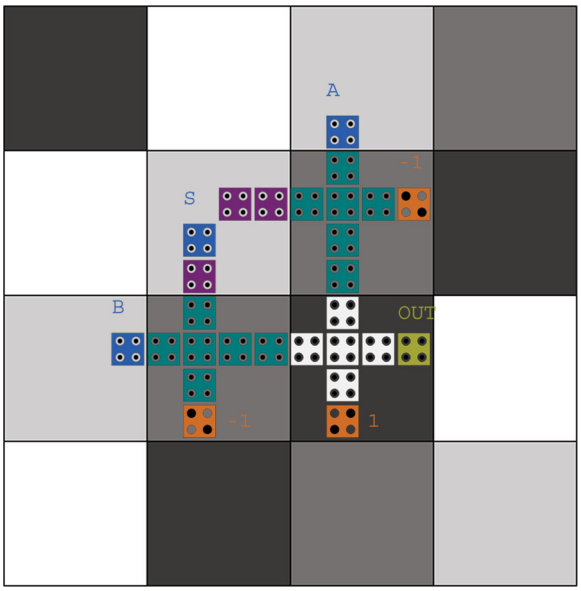


Fig. 9 The schematic diagram for 2:1 MUX implementation

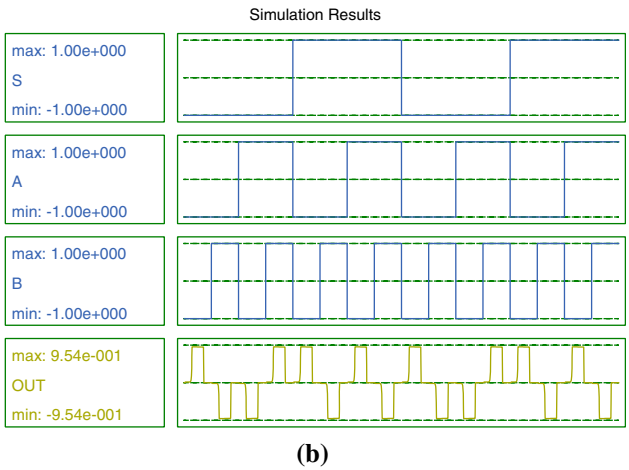
wire orientation of the proposed ESR clocking scheme. All the analytical results verify the superiority and flexibility of the proposed clocking scheme.

6 Conclusion

In this paper, an Efficient, Scalable & Regular (ESR) clocking scheme is established, which reduces wire-crossing drastically in the underlying clocking circuit. In the comparison of the 4×4 grid of the clocking layout, it outperform the existing clocking schemes achieving 50% and above fewer wire-crossings. At the same time, the alternate approach for wire layout delivers optimum performance eliminating the wire crossing in underlying metal wire. It also enables feedback paths with small loops incurring less area and can apply current integrated circuit fabrication technologies to realize efficient clocking circuitry. Case studies presented in this paper advocates the prominence of an area reduction of factors 3 to 5 and delay decrease by up to factor 3 in comparison with an existing advanced clocking scheme. Besides, it's worth noting to mention that the single timing region of the clock phase under our proposed timing scheme is larger than the region



(a)



(b)

Fig. 10 2:1 Multiplexer **a** Cell Layout using the proposed ESR and **b** Simulated Output

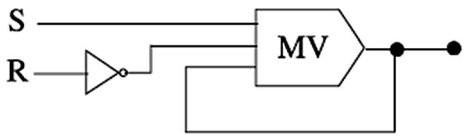


Fig. 11 The schematic diagram for SR Latch implementation

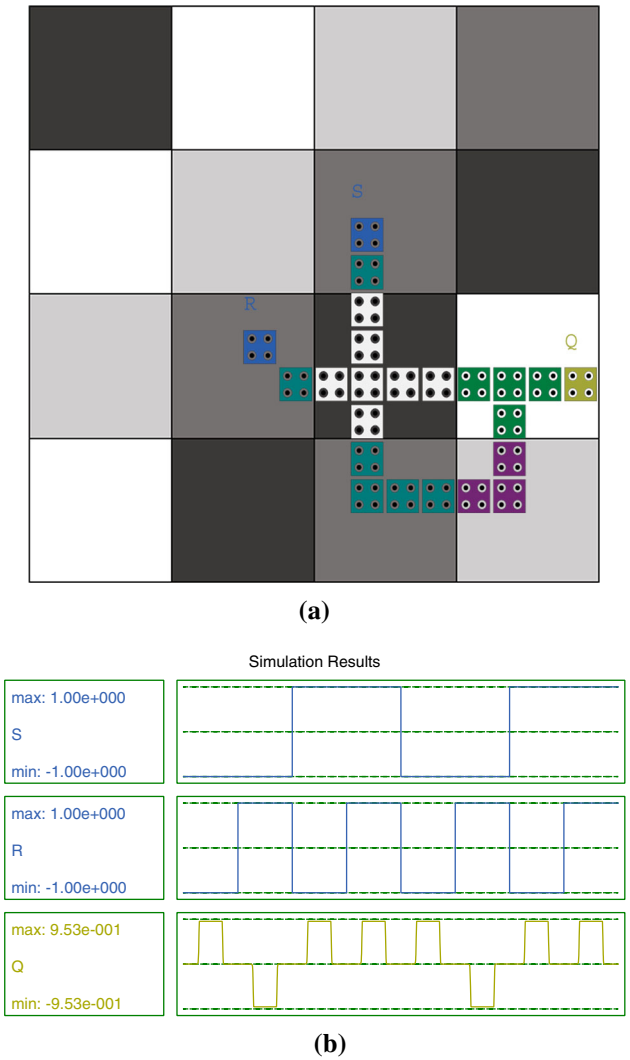


Fig. 12 SR Latch **a** Cell Layout using the proposed ESR and **b** Simulated Output

under other timing schemes for a particular circuit, which also eradicates the need for excessive clock zone. Thus, the proposed scheme simplifies the development of placement and routing algorithms for QCA technology by its all-round flexibility.

In future works, algorithms for automatic placement and routing of future QCA standard cells using the proposed clocking scheme can be developed.

Table 2 Performance Comparison of ESR clocking scheme

Metrics	2:1 Multiplexer						SR Latch					
	2DWave [45]	USE [6]	RES [12]	Tiles [47]	ESR	Gain	2DWave [45]	USE [6]	RES [12]	Tiles [47]	ESR	Gain
Cell Count	129	84	48	94	27	43.75%	168	47	35	45	23	34.28%
Area (nm^2)	34844	132924	82362	119042	41451	65.17%	627200	82044	64964	64268	39555	37.83%
Latency (Clock Zones)	8	6	4	6	3	25%	8	6	4	4	4	Same
Grid Block Used	6X5	4X3	3X4	4X4	3X3	1 Row/Col	8X4	3X4	3X3	4X4	3X3	Same
Metal Wire Crossing (Fig. 5)	0	3	0	3	0	Optimum	4	3	3	2	1	50%
Metal Wire Crossing (Fig. 7)	0	3	0	0	0	Optimum	4	3	3	0	0	Optimum

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

References

1. Agrawal, P., Sinha, S., & Wairya, S. (2016). Quantum dot cellular automata based parity generator and detector: A review. *International Journal of Electronics and Communication Engineering*, *5*, 3.
2. AlKaldy, E., Majeed, A. H., Bin Zainal, M. S., & Bin Md Nor, D. (2020). Optimum multiplexer design in quantum-dot cellular automata. *Indonesian Journal of Electrical Engineering and Computer Science*, *17*(1), 148–155.
3. Bhanja, S., Ottavi, M., Lombardi, F., & Pontarelli, S. (2007). Qca circuits for robust coplanar crossing. *Journal of Electronic Testing*, *23*(2–3), 193–210.
4. Bhowmik, D., Saha, A.K., & Dutta, P. (2016). A novel design to obtain fault tolerant majority gate for five input majority gate by quantum cellular automata. In *2016 International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE)*, (pp. 429–433). IEEE.
5. Bhowmik, D., Saha, A.K., Dutta, P., & Nandi, S. (2017). Implementation of basic and universal gates in a single circuit based on quantum-dot cellular automata using multi-layer crossbar wire. In *IOP Conference Series: Materials Science and Engineering*, (vol. 225, p. 012172). IOP Publishing.
6. Campos, C. A. T., Marciano, A. L., Neto, O. P. V., & Torres, F. S. (2015). Use: A universal, scalable, and efficient clocking scheme for qca. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *35*(3), 513–517.
7. Compano, R., Molenkamp, L., & Paul, D. (2000). *Roadmap for nanoelectronics*. Future and Emerging Technologies: European Commission IST programme.
8. Crocker, M., Niemier, M., Hu, X. S., & Lieberman, M. (2008). Molecular qca design with chemically reasonable constraints. *ACM Journal on Emerging Technologies. Computing Systems (JETC)*, *4*(2), 1–21.
9. Devadoss, R., Paul, K., & Balakrishnan, M.(2010). Clocking-based coplanar wire crossing scheme for qca. In *2010 23rd International Conference on VLSI Design*, (pp. 339–344). IEEE.
10. Elke, S., & Carlos, C. J. (2017). *Molecular electronics: an introduction to theory and experiment* (Vol. 15). Singapore: World Scientific.
11. Goswami, M., Mohit, K., & Sen, B. (2017). Cost effective realization of xor logic in qca. In *2017 7th International Symposium on Embedded Computing and System Design (ISED)*, (pp. 1–5). IEEE
12. Goswami, M., Mondal, A., Mahalat, M. H., Sen, B., & Sikdar, B. K. (2019). An efficient clocking scheme for quantum-dot cellular automata. *International Journal of Electronics Letters, 8*(1), 1–14.
13. Goswami, M., Roychoudhury, M., Sarkar, J., Sen, B., & Sikdar, B. K. (2019). An efficient inverter logic in quantum-dot cellular automata for emerging nanocircuits. *Arabian Journal for Science and Engineering, 45*(4), 1–12.
14. Hennessy, K., & Lent, C. S. (2001). Clocking of molecular quantum-dot cellular automata. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, *19*(5), 1752–1755.
15. Hennessy, K., & Lent, C. S. (2001). Clocking of molecular quantum-dot cellular automata. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, *19*(5), 1752–1755. https://doi.org/10.1116/1.1394729..
16. Huang, J., Momenzadeh, M., & Lombardi, F. (2007). Design of sequential circuits by quantum-dot cellular automata. *Microelectronics Journal*, *38*(4–5), 525–537.
17. Janez, M., Pecar, P., & Mraz, M. (2012). Layout design of manufacturable quantum-dot cellular automata. *Microelectronics Journal*, *43*(7), 501–513.
18. Kanaya, H., Shibayama, H., Sogabe, R., Suzuki, S., & Asada, M. (2012). Fundamental oscillation up to 131 thz in resonant tunneling diodes with thin well and barriers. *Applied Physics Express*, *5*(12), 124101.
19. Lent, C. S., & Tougaw, P. D. (1997). A device architecture for computing with quantum dots. *Proceedings of the IEEE*, *85*(4), 541–557.
20. Lent, C. S., Tougaw, P. D., & Porod, W. (1993). Bistable saturation in coupled quantum dots for quantum cellular automata. *Applied Physics Letters*, *62*(7), 714–716.
21. Lent, C. S., Tougaw, P. D., Porod, W., & Bernstein, G. H. (1993). Quantum cellularautomata. *Nanotechnology*, *4*(1), 49.
22. Liu, W., Lu, L., O'Neill, M., & Swartzlander, E. E. (2014). A first step toward cost functions for quantum-dot cellular automata designs. *IEEE Transactions on Nanotechnology*, *13*(3), 476–487.
23. Majeed, A. H., AlKaldy, E., & Albermany, S. (2019). An energy-efficient ram cell based on novel majority gate in qca technology. *SN Applied Sciences*, *1*(11), 1354.
24. Majeed, A. H., AlKaldy, E., Zainal, M., & Nor, D. (2019). A new 5-input majority gate without adjacent inputs crosstalk effect in qca technology. *Indonesian Journal of Electrical Engineering and Computer Science*, *14*(3), 1159–1164.
25. Majeed, A. H., Alkaldy, E., bin Zainal, M. S., Nor, B. M., et al. (2019). Synchronous counter design using novel level sensitive t-ff in qca technology. *Journal of Low Power Electronics and Applications*, *9*(3), 27.
26. Moaiyeri, M. H., Nasiri, M., & Khastoo, N. (2016). An efficient ternary serial adder based on carbon nanotube fets. *Engineering Science and Technology, an International Journal*, *19*(1), 271–278.
27. Mukhopadhyay, D., & Dutta, P. (2012). Quantum cellular automata based novel unit reversible multiplexer. *Advanced Science Letters*, *16*(1), 163–168.
28. Nath, R. K., Sen, B., & Sikdar, B. K. (2017). Optimal synthesis of qca logic circuit eliminating wire-crossings. *IET Circuits, Devices & Systems*, *11*(3), 201–208.
29. Navi, K., Sayedsalehi, S., Farazkish, R., & Azghadi, M. R. (2010). Five-input majority gate, a new device for quantum-dot cellular automata. *Journal of Computational and Theoretical Nanoscience*, *7*(8), 1546–1553.
30. Niemier, M.T. (2000). Designing digital systems in quantum cellular automata. Ph.D. thesis, University of Notre Dame.
31. Pal, J., Bhattacharjee, S., Saha, A.K., & Dutta, P. (2019). Study on temperature stability and fault tolerance of adder in quantum-dot cellular automata. In *2019 5th International Conference on Signal Processing, Computing and Control (ISPCC)*, (pp. 69–74). IEEE.
32. Pal, J., Dutta, P., & Saha, A.K. (2018). Realization of basic gates using universal gates using quantum-dot cellular automata. In *Proceedings of the International Conference on Computing and Communication Systems*, (pp. 541–549). Springer.
33. Rani, S., & Sasamal, T. N. (2017). A new clocking scheme for quantum-dot cellular automata based designs with single or regular cells. *Energy Procedia*, *117*, 466–473.
34. Sen, B., Anand, A.S., Adak, T., & Sikdar, B.K. (2011). Thresholding using quantum-dot cellular automata. In *2011 International Conference on Innovations in Information Technology*, (pp. 356–360). IEEE.

35. Sen, B., Dalui, M., & Sikdar, B.K. (2010). Introducing universal qca logic gate for synthesizing symmetric functions with minimum wire-crossings. In *Proceedings of the International Conference and Workshop on Emerging Trends in Technology*, (pp. 828–833).
36. Sen, B., Dutta, M., Banik, D., Singh, D.K., & Sikdar, B.K. (2012). Design of fault tolerant reversible arithmetic logic unit in qca. In *2012 International Symposium on Electronic System Design (ISED)*, (pp. 241–245). IEEE.
37. Sen, B., Dutta, M., Goswami, M., & Sikdar, B. K. (2014). Modular design of testable reversible alu by qca multiplexer with increase in programmability. *Microelectronics Journal*, *45*(11), 1522–1532.
38. Sen, B., Dutta, M., & Sikdar, B. K. (2014). Efficient design of parity preserving logic in quantum-dot cellular automata targeting enhanced scalability in testing. *Microelectronics Journal*, *45*(2), 239–248.
39. Sen, B., Goswami, M., Some, S., & Sikdar, B.K. (2013). Design of sequential circuits in multilayer qca structure. In *2013 International Symposium on Electronic System Design*, (pp. 21–25). IEEE.
40. Sen, B., Sahu, Y., Mukherjee, R., Nath, R. K., & Sikdar, B. K. (2016). On the reliability of majority logic structure in quantum-dot cellular automata. *Microelectronics Journal*, *47*, 7–18.
41. Shih, S.M., Su, W.F., Lin, Y.J., Wu, C.S., & Chen, C.D. (2003). *Single electron device US Patent 6,586,787*.
42. Shin, S. H., Lee, G. J., & Yoo, K. Y. (2015). Design of exclusive-or logic gate on quantum-dot cellular automata. *International Journal of Control and Automation*, *8*(2), 95–104.
43. Tóth, G., & Lent, C. S. (1999). Quasiadiabatic switching for metal-island quantum-dot cellular automata. *Journal of Applied Physics*, *85*(5), 2977–2984.
44. Tougaw, P. D., & Lent, C. S. (1994). Logical devices implemented using quantum cellular automata. *Journal of Applied physics*, *75*(3), 1818–1825.
45. Vankamamidi, V., Ottavi, M., & Lombardi, F. (2007). Two-dimensional schemes for clocking/timing of qca circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *27*(1), 34–44.
46. Walus, K., Dysart, T. J., Jullien, G. A., & Budiman, R. A. (2004). Qcadesigner: a rapid design and simulation tool for quantum-dot cellular automata. *IEEE Transactions on Nanotechnology*, *3*(1), 26–31. https://doi.org/10.1109/TNANO.2003.820815.
47. Wang, L., Xie, G., Zhu, R., & Yu, C. (2019). An optimized clocking scheme for nanoscale quantum-dot cellular automata circuit. In *2019 IEEE 14th International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*, (pp. 336–341).

Jayanta Pal completed the B.Tech. degree in Computer Science and Engineering from IEM, Kolkata, India, in 2009, and the M.Tech. degree in Computer Science and Engineering from Tripura University, Tripura, India, in 2011 and pursuing Ph.D. degree from Department of Computer Science & Engineering, NIT Agartala, Tripura, India. Currently, he is working in the post of Assistant Professor at the Department of Information Technology, Tripura University, Tripura, India. His current research interests include Quantum-dot Cellular Automata, Fault-tolerant Architectures for emerging devices in Nano-Scale and Quantum Computing.

Amit Kumar Pramanik completed the B.Tech. degree in Information Technology from RCCIIT, Kolkata, WB, India, in 2011, ME degree in Computer Science & Engineering from IIEST, Shibpur, WB, India, in 2014 and pursuing Ph.D. degree from Department of Computer Science & Engineering, NIT Durgapur, WB, India. Currently, he is working in the post of Assistant Professor at the Department of Computer Science and Engineering at Dumka Engineering College, Jharkhand, India. His current research interests include Quantum-dot Cellular Automata and Quantum Computing.

Jyotirmoy Sil Sharma has completed the BCA (Bachelor of Computer Application) degree from Tripura University, Tripura, India, in the year 2017, and presently pursuing his master's in the course of MCA (Masters in Computer Application) from Tripura University, Tripura, India. His current research interests include Quantum-dot Cellular Automata (QCA) and Nanotechnology.

Apu Kumar Saha received the B. Sc. degree in Mathematics Honours and M. Sc (Mathematics) from Tripura University in 1996 and 1998 respectively and Ph.D. degree from National Institute of Technology Agartala, India, in 2012. He is currently an Associate Professor at the Department of Mathematics in NIT Agartala, Tripura, India. His current research interests include Evolutionary Optimization Techniques, Swarm intelligence, MCDM, Quantum-dot Cellular Automata etc.

Bibhash Sen (M'12) received the B.Tech. degree in Computer Science and Engineering from NERIST, Nirjuli, India, in 2002, and the M.E. and Ph.D. degrees in Computer Science and Engineering from IIEST, Shibpur, India, in 2007 and 2015, respectively. He is currently an Associate Professor at the Department of Computer Science and Engineering, NIT Durgapur, Durgapur, India. His current research interests include Hardware Security, Security System for Wireless Sensing, Hardware Trojan, Quantum-dot Cellular Automata, Reversible Logic, and Fault-tolerant Architectures for emerging Nano devices.